IN THE UNITED STATES DISTRICT COURT
FOR THE SOUTHERN DISTRICT OF NEW YORK

CIF Licensing, L.L.C., Mitsubishi Electric Corporation, Samsung Electronics Co., Ltd., Thomson Licensing, The Trustees of Columbia University in the City of New York, U.S. Philips Corporation, and Koninklijke Philips Electronics, N.V.,	:	
Plaintiffs,	:	C.A. No. 08 CV 01700 (KMK) **JURY TRIAL DEMANDED**
- against -	:	
ATI Technologies, Inc.,	:	
Defendant.	:	

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiffs CIF Licensing, L.L.C., d/b/a GE Licensing ("GE"), Mitsubishi Electric Corporation (alternatively named Mitsubishi Denki Kabushiki Kaisha) ("Mitsubishi"), Samsung Electronics Co., Ltd. ("Samsung"), Thomson Licensing, ("Thomson"), The Trustees of Columbia University in the City of New York ("Columbia"), U.S. Philips Corporation ("U.S. Philips"), and Koninklijke Philips Electronics, N.V. ("KPENV") (collectively "Philips"), (collectively "Plaintiffs") by their undersigned attorneys, for their complaint against defendant ATI Technologies, Inc. ("ATI" or "Defendant") allege as follows:

SUMMARY OF CLAIMS

1. This is a patent infringement action brought against Defendant by GE, Mitsubishi, Samsung, Thomson, Columbia, and Philips, because of Defendant's infringement of Plaintiffs' patents which are all essential to the practice of the world-wide video compression standard known as MPEG-2. Plaintiffs are owners of a number of patents essential to the MPEG-2 standard as implemented in numerous devices manufactured and sold by Defendant. Among other applications, the MPEG-2 standard is used by devices manufactured and sold by Defendant and by others in the playing of stored or transmitted video information.

2. MPEG-2 is a compression technology that can be used for digital video signals, i.e., moving picture signals in movies or television. To produce an MPEG-2 compliant signal or bitstream, a digital video signal is compressed/encoded to remove redundant or visually insignificant information. The encoding/compression reduces the amount of information needed to represent the video signal so that it can be stored in a smaller storage area or transmitted in a lower capacity communication channel. Alternatively, MPEG-2 enables storage or transmission of more or higher fidelity video signals. For example, without compression, a 133 minute long movie would require over 25 DVD discs for storage. Using MPEG-2, a good quality 133 minute long movie can be stored on a single DVD disc. In the case of terrestrial broadcast, MPEG-2 enables transmission of a high definition television ("HDTV") signal of 1920 x 1080 pixel resolution on the same frequency channel that currently carries a standard definition television signal of 720 x 480 pixel resolution. MPEG-2 also enables transmission of at least four standard definition television signals in the same frequency channel that currently carries one standard definition television signal.

3. MPEG-2 is currently employed in and makes possible the storage, playing, transmission and reproduction of full-length films on DVD discs, digital terrestrial broadcast television, digital satellite television broadcasts, and digital cable television. Numerous consumer products thereby use software and/or hardware to encode and/or decode video in compliance with the MPEG-2 standard, including but not limited to video telecommunications equipment; disc players or recorders, including DVD players and recorders, personal video recorders, and digital video recorders; television sets; personal computers; camcorders; cameras; video receivers, including internet protocol televisions ("IPTV"), terrestrial, satellite and cable receivers, set top boxes, converters, or descramblers; and video game consoles/video game equipment ("MPEG-2 Products"). Consumer spending of MPEG-2 Products in the United States amounts to billions of dollars per year.

4. Use of the patents in suit is essential to the practice of the MPEG-2 technology.

5. Defendant manufactures, offers to sell, sells, uses, and imports a number of products with MPEG-2 functionality. ATI's website refers to a number of "GPU" cards ("Defendant's Cards") and "TV tuners" ("Defendant's Tuners") that encode/compress video according to the MPEG-2 standard, decode/decompress video according to the MPEG-2 standard, and/or accelerate MPEG-2 decoding/decompressing and/or MPEG-2 encoding/compression. Defendant's Cards are also referred to in the industry as "graphics accelerators," "graphics adapters," and "graphics cards." Defendant's Tuners are also referred to in the industry as "TV Tuners" and "video input adapters." Both of these types of devices are

typically installed into a desktop computer or laptop computer, or connected to an external port of a desktop computer or laptop computer.

6. Defendant is infringing the patents in suit, by, among other things, offering for sale and selling in the United States and in this judicial district Defendant's Cards and Defendant's Tuners, which employ the MPEG-2 patented technology.

7. According to Defendant's website, Defendant's Cards utilize the MPEG-2 standard. For example, the ATI X1300 GPU performs accelerated MPEG-2 decoding and transcoding, where transcoding is a combination of decoding and encoding. The website also indicates that the ATI X1300 GPU performs motion compensation, DCT, iDCT and 3:2 pulldown, all of which are steps performed while encoding/compressing video or decoding/decompressing video according to the MPEG-2 standard. (Exhibit ("Exh.") 1). Defendant's website also advertises other GPU products including, but not limited to: Radeon 9550, Radeon 1050, Radeon X1300, Radeon X1550, Radeon X1600, Radeon X1650, Radeon X1800, Radeon X1900, Radeon X1950, Radeon HD 2400, Radeon HD 2600, Radeon HD 2900, and Radeon HD 3800.

8. According to Defendant's website, Defendant's Tuners utilize the MPEG-2 Standard. For example, the ATI TV Wonder 650 Series TV tuner includes a hardware MPEG-2 encoder. Defendant's website explains that this device is capable of encoding or compressing a video signal according to the MPEG-2 standard. (Exh. 2, available at http://ati.amd.com/products/theater650pro/ATITheater650WhitePaper.pdf). Other TV tuner products include: ATI TV Wonder 600 Series, ATI TV Wonder 550 Series and ATI TV Wonder 200 Series products.

9. For many years, Defendant has had an opportunity to license the patents in suit by either licensing one or more such patents directly from the individual Plaintiffs or, in the alternative, by taking a license from MPEG LA, L.L.C. ("MPEG LA"), which offers a non-discriminatory patent portfolio license under many patents essential to the practice of MPEG-2 technology, including all patents in suit. (Exh. 3).

10. MPEG LA was established in 1996 to provide the marketplace with non-discriminatory access to as many of the patents which are essential to MPEG-2 technology as possible. MPEG LA is a non-exclusive licensee of each of the patents in suit as well as numerous other patents essential to the practice of the MPEG-2 technology. MPEG LA has the authority to offer a non-exclusive sublicense to the approximately 150 MPEG-2 patent families offered in the MPEG-2 Patent Portfolio License throughout the world — including the patents in suit — on non-discriminatory and reasonable terms. Approximately 1,300 licensees located throughout the world have executed the standard MPEG-2 Patent Portfolio License offered by MPEG LA. MPEG LA's licensing program began after the United States Department of Justice reviewed the circumstances surrounding the formation of MPEG LA and its standard MPEG-2 Patent Portfolio License, among other things, and issued a favorable Business Review Letter.

11. Each Plaintiff is committed to license the patents in suit on reasonable terms. As an alternative, Defendant, and indeed any potential licensee, can get a license from MPEG LA as a convenience to the licensee. The MPEG LA license adds an alternative choice to the marketplace, in addition to, not instead of, bilateral licenses with each of the licensors, including the Plaintiffs herein.

12. Competitors of Defendant, such as Hauppauge Computer Works, and NVIDIA Corporation and Pinnacle Systems, have executed the MPEG LA license which Defendant has declined to execute.

13. Notwithstanding the fact that Defendant was aware that its products used patents owned by Plaintiffs, Defendant has refused to enter into any license with Plaintiffs.

JURISDICTION AND VENUE

14. This is an action for patent infringement under Title 35 of the United States Code. This Court has subject matter jurisdiction under 28 U.S.C. § 1338.

15. Upon information and belief, ATI has its principal place of business in Ontario, Canada. ATI through its own acts and/or through the acts of its affiliated corporations, acting as its agents or alter egos, has purposefully sold infringing products through regular distribution channels knowing such products would be used, offered for sale and/or sold in this judicial district.

16. Venue is proper in this district pursuant to 28 U.S.C. §§ 1391(b), (c), and (d), and § 1400(b).

THE PARTIES

17. Plaintiff CIF Licensing, L.L.C. is a limited liability company organized and existing under the laws of the State of Delaware, having its principal place of business in Princeton, New Jersey.

18. Plaintiff Mitsubishi is a corporation of Japan, having its principal place of business in Tokyo, Japan.

19. Plaintiff Samsung is a corporation of Korea, having its principal place of business in Seoul, Korea.

20. Plaintiff Thomson is a corporation of France, having a principal place of business in Boulogne-Billancourt Cedex, France.

21. Plaintiff Columbia is a not-for-profit corporation of New York, having its principal place of business in New York, New York.

22. Plaintiff U.S. Philips is a Delaware corporation having its principal place of business in Briarcliff Manor, New York.

23. Plaintiff KPENV is a corporation of Netherlands, having its principal place of business in Amsterdam, The Netherlands.

24. Upon information and belief, Defendant ATI is a corporation of Canada, having its principal place of business in Markham, Ontario, Canada.

DEFENDANT'S INFRINGEMENT

25. Defendant manufactures, imports, offers for sale and/or sells within the United States and in this district MPEG-2 Products, including the Defendant's Tuners and Defendant's Cards.

26. Defendant's MPEG-2 Products are purposely shipped by Defendant through an established distribution channel and are knowingly sold, among other places, within this judicial district.

27. The manufacture, importation, use, offer for sale, and/or sale of Defendant's MPEG-2 Products — which do any one or more of the following: decode, encode,

or accelerate the decoding or encoding of digital video signals using patented MPEG-2 methods and devices — directly and/or indirectly infringe the patents in suit.

28. Defendant has published and continues to regularly publish advertisements and product descriptions on the Internet and in newspapers and magazines stating that its products are MPEG-2 compatible and/or capable of MPEG-2 encoding or decoding. (Exhs. 1, 2).

29. Defendant contributorily infringes the patents in suit by importing, selling, offering for sale, and/or selling Defendant's MPEG-2 Products in this judicial district and elsewhere, knowing that such MPEG-2 Products are especially made and/or especially adapted for use in an infringement of the patents in suit.

30. Defendant actively induces the infringement of the patents in suit by offering for sale, selling, encouraging, and instructing others to use Defendant's MPEG-2 Products knowing that the use of these products to, among other things, decode, encode, or accelerate the decoding or encoding MPEG-2 video signals, causes others to infringe the patents in suit.

31. Defendant's infringing actions were without the consent or authority of Plaintiffs. Defendant does not now have and has never possessed a license under any of the patents in suit.

32. This is an exceptional case, and, accordingly, Plaintiffs are entitled to enhanced damages and their attorney's fees pursuant to 35 U.S.C. §§ 284 and 285.

33. Plaintiffs, and each of them, have suffered irreparable injury for which there is no adequate remedy at law as a result of Defendant's infringement of the patents in suit.

Pursuant to 35 U.S.C. § 283, Plaintiffs are entitled to an injunction against further infringement by an order preventing Defendant from selling any of Defendant's MPEG-2 Products in the United States.

FIRST CAUSE OF ACTION

34. The allegations contained in paragraphs 1 through 33 above are repeated and realleged as if fully set forth herein.

35. CIF Licensing, L.L.C. is the legal owner by assignment of United States Letters Patent No. 5091782 ("the '782 Patent") (Exh. 4).

36. Defendant has infringed and is infringing the '782 Patent by making, using, offering to sell, or selling MPEG-2 Products within the United States or importing into the United States MPEG-2 Products, in violation of 35 U.S.C. §§ 271(a)-(c).

37. Unless enjoined, Defendant will continue to infringe the '782 Patent.

SECOND CAUSE OF ACTION

38. The allegations contained in paragraphs 1 through 33 above are repeated and realleged as if fully set forth herein.

39. Mitsubishi is the legal owner by assignment of United States Letters Patent No. 5072295 ("the '295 Patent") (Exh. 5).

40. Defendant has infringed and is infringing the '295 Patent by making, using, offering to sell, or selling MPEG-2 Products within the United States or importing into the United States MPEG-2 Products, in violation of 35 U.S.C. §§ 271(a)-(c).

41. Unless enjoined, Defendant will continue to infringe the '295 Patent.

THIRD CAUSE OF ACTION

42. The allegations contained in paragraphs 1 through 33 above are repeated and realleged as if fully set forth herein.

43. Mitsubishi is the legal owner by assignment of United States Letters Patent No. 5990960 ("the '960 Patent") (Exh. 6).

44. Defendant has infringed and is infringing the '960 Patent by making, using, offering to sell, or selling MPEG-2 Products within the United States or importing into the United States MPEG-2 Products, in violation of 35 U.S.C. §§ 271(a)-(c).

45. Unless enjoined, Defendant will continue to infringe the '960 Patent.

FOURTH CAUSE OF ACTION

46. The allegations contained in paragraphs 1 through 33 above are repeated and realleged as if fully set forth herein.

47. Mitsubishi is the legal owner by assignment of United States Letters Patent No. 6097759 ("the '759 Patent") (Exh. 7).

48. Defendant has infringed and is infringing the '759 Patent by making, using, offering to sell, or selling MPEG-2 Products within the United States or importing into the United States MPEG-2 Products, in violation of 35 U.S.C. §§ 271(a)-(c).

49. Unless enjoined, Defendant will continue to infringe the '759 Patent.

FIFTH CAUSE OF ACTION

50. The allegations contained in paragraphs 1 through 33 above are repeated and realleged as if fully set forth herein.

51. Samsung is the legal owner by assignment of United States Letters Patent No. 5654706 ("the '706 Patent") (Exh. 8).

52. Defendant has infringed and is infringing the '706 Patent by making, using, offering to sell, or selling MPEG-2 Products within the United States or importing into the United States MPEG-2 Products, in violation of 35 U.S.C. §§ 271(a)-(c).

53. Unless enjoined, Defendant will continue to infringe the '706 Patent.

SIXTH CAUSE OF ACTION

54. The allegations contained in paragraphs 1 through 33 above are repeated and realleged as if fully set forth herein.

55. Samsung is the legal owner by assignment of United States Letters Patent No. 6680975 ("the '975 Patent") (Exh. 9).

56. Defendant has infringed and is infringing the '975 Patent by making, using, offering to sell, or selling MPEG-2 Products within the United States or importing into the United States MPEG-2 Products, in violation of 35 U.S.C. §§ 271(a)-(c).

57. Unless enjoined, Defendant will continue to infringe the '975 Patent.

SEVENTH CAUSE OF ACTION

58. The allegations contained in paragraphs 1 through 33 above are repeated and realleged as if fully set forth herein.

59. Thomson is the legal owner by assignment of United States Letters Patent No. 7020204 ("the '204 Patent") (Exh. 10).

60. Defendant has infringed and is infringing the '204 Patent by making, using, offering to sell, or selling MPEG-2 Products within the United States or importing into the United States MPEG-2 Products, in violation of 35 U.S.C. §§ 271(a)-(c).

61. Unless enjoined, Defendant will continue to infringe the '204 Patent.

EIGHTH CAUSE OF ACTION

62. The allegations contained in paragraphs 1 through 33 above are repeated and realleged as if fully set forth herein.

63. Thomson is the legal owner by assignment of United States Letters Patent No. 5422676 ("the '676 Patent") (Exh. 11).

64. Defendant has infringed and is infringing the '676 Patent by making, using, offering to sell, or selling MPEG-2 Products within the United States or importing into the United States MPEG-2 Products, in violation of 35 U.S.C. §§ 271(a)-(c).

65. Unless enjoined, Defendant will continue to infringe the '676 Patent.

NINTH CAUSE OF ACTION

66. The allegations contained in paragraphs 1 through 33 above are repeated and realleged as if fully set forth herein.

67. Columbia is the legal owner by assignment of United States Letters Patent No. Reissue 35093 ("the '093 Patent") (Exh. 12).

68. Defendant has infringed and is infringing the '093 Patent by making, using, offering to sell, or selling MPEG-2 Products within the United States or importing into the United States MPEG-2 Products, in violation of 35 U.S.C. §§ 271(a)-(c).

69. Unless enjoined, Defendant will continue to infringe the '093 Patent.

TENTH CAUSE OF ACTION

70. The allegations contained in paragraphs 1 through 33 above are repeated and realleged as if fully set forth herein.

71. U.S. Philips is the legal owner by assignment of United States Letters Patent No. 5844867 ("the '867 Patent"), while KPENV is the exclusive licensee of the '867 Patent in the field of products that comply with the MPEG-2 Standard. (Exh. 13).

72. Defendant has infringed and is infringing the '867 Patent by making, using, offering to sell, or selling MPEG-2 Products within the United States or importing into the United States MPEG-2 Products, in violation of 35 U.S.C. §§ 271(a)-(c).

73. Unless enjoined, Defendant will continue to infringe the '867 Patent.

ELEVENTH CAUSE OF ACTION

74. The allegations contained in paragraphs 1 through 33 above are repeated and realleged as if fully set forth herein.

75. KPENV is the legal owner by assignment of United States Letters Patent No. 5606539 ("the '539 Patent") (Exh. 14).

76. Defendant has infringed and is infringing the '539 Patent by making, using, offering to sell, or selling MPEG-2 Products within the United States or importing into the United States MPEG-2 Products, in violation of 35 U.S.C. §§ 271(a)-(c).

77. Unless enjoined, Defendant will continue to infringe the '539 Patent.

WHEREFORE, Plaintiffs demand judgment as follows:

1. Adjudging, finding, and declaring that Defendant is infringing the patents in suit.

2. Permanently enjoining Defendant, its officers, agents, servants, employees, and attorneys, and those persons in active concert or participation with it, from infringing the patents in suit.

3. Awarding the respective Plaintiffs an accounting and damages against Defendant in a sum to be determined at trial, together with interest and costs as fixed by the Court; all of these damages to be enhanced in amount up to treble the amount of compensatory damages, as provided by 35 U.S.C. § 284.

4. Awarding Plaintiffs their reasonable attorneys' fees, costs, and disbursements in this action pursuant to 35 U.S.C. § 285.

5. Granting Plaintiffs such other and further relief as is just and proper.

JURY DEMAND

Plaintiffs hereby demand a trial by jury of all issues that may be so tried.

SULLIVAN & CROMWELL LLP

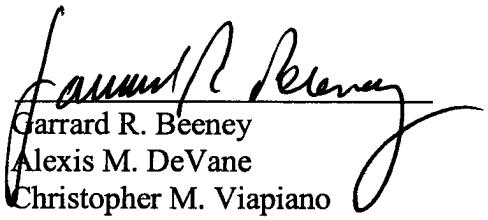
By: 
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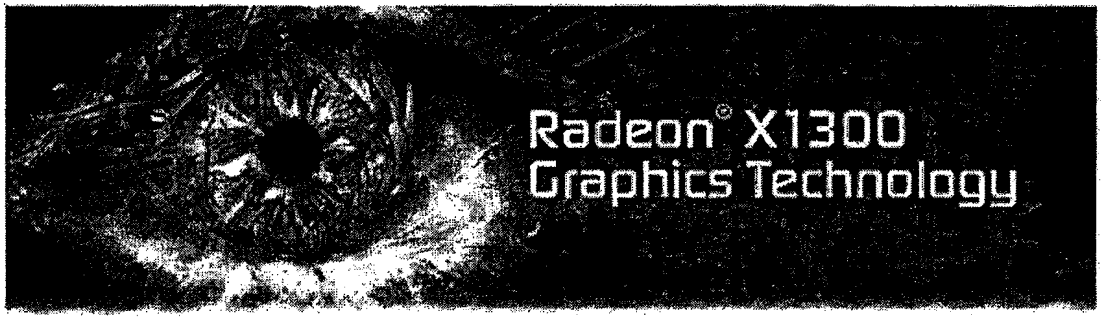
Exhibit 1



Specifications

Features

- 105 million transistors on 90nm fabrication process
- Four pixel shader processors
- Two vertex shader processors
- 128-bit 4-channel DDR/DDR2/GDDR3 memory interface
  - 32-bit/1-channel, 64-bit/2-channel, and 128-bit/4-channel configurations
- Native PCI Express x16 bus interface
  - AGP 8x configurations also supported with external bridge chip
- Dynamic Voltage Control

High Performance Memory Controller

- Fully associative texture, color, and Z/stencil cache designs
- Hierarchical Z-buffer with Early Z test
- Lossless Z Compression (up to 48:1)
- Fast Z-Buffer Clear

- Z/stencil xache optimized for real-time shadow rendering

Ultra-Threaded Shader Engine

- Support for Microsoft® DirectX® 9.0 Shader Model 3.0 programmable vertex and pixel shaders in hardware
- Full speed 128-bit floating point processing for all shader operations
- Up to 128 simultaneous pixel threads
- Dedicated branch execution units for high performance dynamic branching and flow control
- Dedicated texture address units for improved efficiency
- 3Dc+ texture compression
  - High quality 4:1 compression for normal maps and two-channel data formats
  - High quality 2:1 compression for luminance maps and single-channel data formats
- Multiple Render Target (MRT) support
- Render to vertex buffer support
- Complete feature set also supported in OpenGL® 2.0

Advanced Image Quality Features

- 64-bit floating point HDR rendering supported throughout the pipeline
  - Includes support for blending and multi-sample anti-aliasing
- 32-bit integer HDR (10:10:10:2) format supported throughout the pipeline
  - Includes support for blending and multi-sample anti-aliasing
- 2x/4x/6x Anti-Aliasing modes
  - Multi-sample algorithm with gamma correction, programmable sparse sample patterns, and centroid sampling
  - New Adaptive Anti-Aliasing feature with Performance and Quality modes
  - Temporal Anti-Aliasing mode
  - Lossless Color Compression (up to 6:1) at all resolutions, including widescreen HDTV resolutions
- 2x/4x/8x/16x Anisotropic Filtering modes
  - Up to 128-tap texture filtering
  - Adaptive algorithm with Performance and Quality options
- High resolution texture support (up to 4k x 4k)

Avivo™ Video and Display Platform

- High performance programmable video processor
  - Accelerated MPEG-2, MPEG-4, DivX, WMV9, VC-1, and H.264 decoding and transcoding
  - DXVA support
  - De-blocking and noise reduction filtering
  - Motion compensation, IDCT, DCT and color space conversion
  - Vector adaptive per-pixel de-interlacing

- 3:2 pulldown (frame rate conversion)
- Seamless integration of pixel shaders with video in real time
- HDR tone mapping acceleration
  - Maps any input format to 10 bit per channel output
- Flexible display support
  - Dual integrated DVI transmitters (one dual-link + one single-link)
    - DVI 1.0 compliant / HDMI interoperable and HDCP ready*
  - Dual integrated 10 bit per channel 400 MHz DACs
  - 16 bit per channel floating point HDR and 10 bit per channel DVI output
  - Programmable piecewise linear gamma correction, color correction, and color space conversion (10 bits per color)
  - Complete, independent color controls and video overlays for each display
  - High quality pre- and post-scaling engines, with underscan support for all outputs
  - Content-adaptive de-flicker filtering for interlaced displays
  - Xilleon™ TV encoder for high quality analog output
  - YPrPb component output for direct drive of HDTV displays**
  - Spatial/temporal dithering enables 10-bit color quality on 8-bit and 6-bit displays
  - Fast, glitch-free mode switching
  - VGA mode support on all outputs
  - Drive two displays simultaneously with independent resolutions and refresh rates
- Compatible with ATI TV/Video encoder products, including Theater 550

* AMD's ATI Radeon™ X and Radeon™ 9550 series of GPUs are capable of processing HDCP signals ("HDCP ready"), however not all ATI Radeon graphics cards are HDCP ready. Please check the applicable ATI Radeon graphics card specification to determine if a particular ATI Radeon graphics card is HDCP ready. Some third parties manufacture graphics cards containing ATI Radeon GPUs -- you can inquire of them which models, if any, are HDCP ready. In addition, playing HDCP content requires additional HDCP ready components, including but not limited to an HDCP ready monitor, disc drive, multimedia application and computer operating system.

**with optional HDTV adapter available from ATI Online Store

CrossFire™

- Multi-GPU technology
  - Inter-GPU communication over PCI Express (no interlink hardware required)
- Four modes of operation:
  - Alternate Frame Rendering (maximum performance)
  - Supertiling (optimal load-balancing)
  - Scissor (compatibility)
  - Super AA 8x/10x/12x/14x (maximum image quality)

HyperMemory™ 2***

- 2nd generation virtual memory management technology
  - Improved PCI Express transfer efficiency
- Supports rendering to system memory as well as local graphics memory

Windows® Logo Program compliant
ATI Catalyst™ Software Suite

*** HyperMemory2 is an optional feature that may not be implemented in some board configurations. HyperMemory is the cumulative total of local and system memory used by the Graphics Processing Unit (GPU) intended for use in the processing and creation of 3D and other images. The amount of HyperMemory is determined by the amount of local memory and available system memory.

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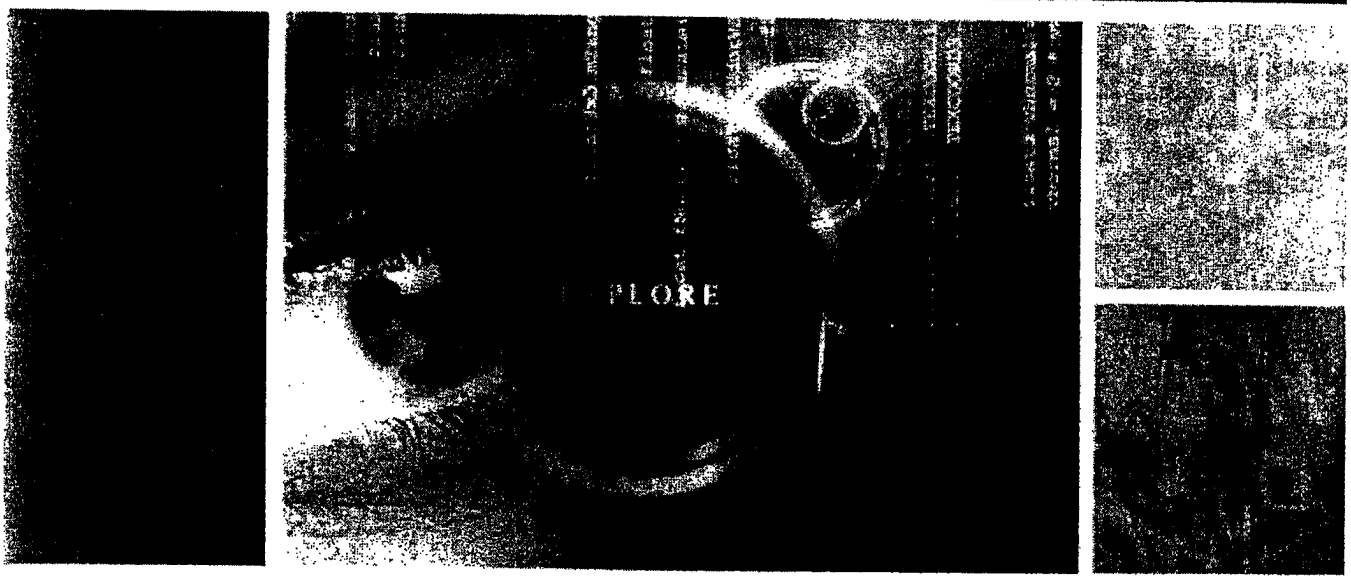
Exhibit 2



ATI Theater™ 650 Pro:
Bringing TV to the PC

Perfecting Analog and Digital TV Worldwide

Introduction: A Media PC Revolution

After years of build-up, the media PC revolution has begun. Driven by such trends as the worldwide migration to digital over-the-air television broadcasting and the imminent arrival of next-generation HD optical discs, consumers are demanding solutions which deliver the immersive experiences promised by these new technologies. The media PC in particular is seen as a key enabler and is well-placed to become the hub of the home entertainment network. Key to this vision is the delivery of high quality television on the PC. From using your computer as a television to recording TV shows, the idea of turning a personal computer into an intelligent TV watching/recording device is attracting millions of users worldwide.

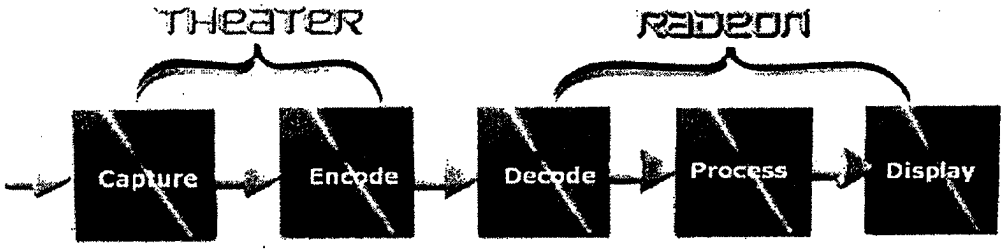


Fig.1 - The video pipeline and the role of the video capture card

Delivering broadcast television signals to the viewer, regardless of the platform, involves the steps outlined in the diagram above (the "video pipeline"), progressing from image capture through to eventual display. To achieve high quality video, the sequential nature of the video pipeline requires that high quality be maintained throughout every stage of the pipeline (for a comprehensive review of the entire video pipeline, refer to the whitepaper "Avivo and the Video Pipeline"). The purpose of the present whitepaper is to highlight some of the key requirements of a high quality video capture/encode solution.

Video Capture & Encode Challenges

A great video experience starts with high-quality video capture. The key processing steps involved in capturing and encoding video are as follows:

- TV tuning / video input
- Intermediate frequency (IF) demodulation
- Video decoding
- Video preprocessing / noise reduction
- MPEG encoding
- Bridge to system

Let's now examine each of these processing stages in turn and explore the key issues and challenges for producing high-quality video

TV Tuning / Video Input

Capturing analog and/or digital video signals (and in the case of analog signals, converting them to digital representations) is the first step required to view video on a PC. This is done through a video input device or a TV tuner. In the case of a TV tuner, the hardware must be tuned to a desired frequency to receive a desired television station.

Analog television is today the predominant broadcast method, for which there are three major transmission standards worldwide:

- NTSC (National Television System Committee)
  - used in North America, Japan, Korea, Taiwan, and parts of Latin America
- PAL (Phase Alternation Line)
  - used in most parts of Europe (France is the notable exception)
- SECAM (Sequential Color with Memory)
  - used in France, Russia, and parts of the Middle East

Increasingly, however, digital television is becoming more prevalent, driven in many cases by government-mandated deadlines for accommodation/switchover to high-definition digital broadcast. For instance, in the US all new TV devices are required to have the capability of receiving broadcast digital signals by March 1, 2007. Major television digital transmission standards worldwide are:

- ATSC (Advanced Television System Committee)
  - used in North America, Japan, Korea, Taiwan, and parts of Latin America
- DVB-T (Digital Video Broadcasting - Terrestrial)
  - used in Europe
- ISDB-T (Integrated Services Digital Broadcasting - Terrestrial)
  - used in Japan

To accommodate the many broadcast standards and variants thereof, TV manufacturers typically require multiple designs with different receivers for each standard, increasing the cost and complexity of multi-standard TV receivers. Increasingly, manufacturers are choosing so-called hybrid tuners (tuners which support both analog and digital formats in the same system) in an effort to reduce costs and improve system flexibility. The actual TV tuner, the 'can' or 'chip' used in a TV tuner card, can greatly affect the resultant video quality.

IF Demodulation

Once a particular TV channel frequency is tuned, the signal must be converted from radio frequency to an intermediate frequency (IF) and then demodulated down to baseband frequency. A high quality TV reception device should pay special attention to the IF demodulation stage of the pipeline, as it will greatly affect the quality of the resultant video.

A high-quality IF demodulator should use digital processing rather than analog. Since PCs are inherently digital systems, the analog television signal must be converted into digital form. Doing this as early in the pipeline as possible reduces chances of signal degradation and allows greater control over the quality of the video. Performing IF demodulation digitally therefore has advantages over low-end solutions which utilize TV tuner modules that have built-in analog IF demodulation (mainly to save cost) and therefore delay the analog-to-digital (A/D) conversion process to the (downstream) video decoding stage. A good digital IF demodulator will ensure that the A/D conversion and demodulation operations are performed at high resolution to maintain a high level of accuracy and robustness of the video signal.

Video Decoding

After the IF demodulation stage, baseband video must be decoded from its broadcast format to a standard format that is recognized by an MPEG encoder. This is one of the most critical stages in the video pipeline – a low quality video decoder will irreparably destroy the video quality. Key requirements for a high quality video decoder include:

- Internal data paths should be sufficiently wide to maintain signal resolution and detail throughout
- High quality comb filtering for precise separation of video components from the composite video stream without artifacts

With respect to the last point, comb filtering is an integral part of the decoding process for composite analog video and is required for separation of the luminance (Y) and chrominance (C) components of the video signal. Note that video captured from an S-Video or Component Video source does not require comb filtering as the Y and C components are already separate.

High quality video decoders have the ability to apply either 2D (two-dimensional, e.g., within a single field/frame) or 3D (three-dimensional, e.g., across multiple fields/frames) filtering to the video stream depending on whether motion exists within the frame.

When there is significant motion in the frame, a multiple-line (3-5 lines are typical) 2D comb filter should be used. The filter in this case looks only at data within a single frame of video to determine the best representation of the content and ensure sharp images without motion artifacts.

If little or no motion is detected in the content, a 3D comb filter will provide much better results by utilizing data from adjacent frames as well as intra-frame data. Still or slow-moving scenes with details such as parallel lines will look much sharper and have far fewer flickering artifacts than if only a 2D comb filter were applied. Sometimes in a product feature specification a manufacturer will advertise a '3-line digital comb filter' - this should not be confused with a 3D filter, as it is in fact a 2D comb filter and will therefore not provide optimal quality for still images.

Given that quality 2D and 3D filters exist within the decoder, the key to ensuring high quality comb filtering is the ability of the processor to detect the presence of motion and therefore select in an intelligent way the appropriate filtering technique – 2D, 3D, or combinations thereof. Advanced chips employ per-pixel adaptive algorithms which will ensure that the best method is used for each and every pixel within a given frame. This will result in the sharpest possible video quality, with the best color representation.

Video Preprocessing / Noise Reduction

Most analog video available in the home contains a significant amount of noise. Even modern digital television that is received from a digital set-top box and imported to the PC over an S-Video connection will contain many visual imperfections. Thus, before video is compressed on the user's PC, noise reduction processing should be employed to clean up as much of this noise as possible. This is a delicate and often sophisticated process – applying too aggressive an algorithm can result in loss of detail and image smearing, whereas too mild an algorithm may yield little to no perceived quality improvements. Many algorithms can be adjusted from high (aggressive) to low (mild) noise reduction settings and can therefore be tuned to best match the requirements of the source content at hand.

A good de-noise algorithm not only provides better video quality but also improves video encoder compression efficiency. Video encoders seek to identify redundancies in an image or video stream and discard extraneous data so as to minimize the amount of data which must be encoded and stored. Since noise is a random artifact, its presence can trick the encoder into thinking that what it is seeing is unique and therefore important for preservation, resulting in reduced compression efficiency. Good noise reduction techniques prior to video encoding will result in more highly compressed bit streams, reducing data storage requirements and effectively increasing disk storage capacity.

Video Encoding

MPEG-2 is the video compression standard that is used on DVD discs and home personal video recorder devices. This standardization makes it the compression algorithm of choice for video capture and playback on the PC. Video recorded directly into MPEG-2 can be immediately exported to a DVD or shared across networks.

MPEG-2 encoding is very computationally intensive and requires advanced motion prediction algorithms in order to compress raw video coming in at 160Mbps (megabits per second) bit-rates down to 4-8Mbps, while maintaining the same resolution and minimizing visible artifacts. Although it is possible to achieve MPEG-2 compression purely in software, the complexity of the task consumes significant CPU resources. This can be a problem when the CPU is simultaneously required to perform other (perhaps higher priority) tasks, and the result can be dropped frames or other undesirable video quality artifacts. High system power consumption is another effect of having the CPU heavily and continuously occupied with video encoding.

Bridge to System - Moving Video to Host Storage (Hard Disk/RAM)

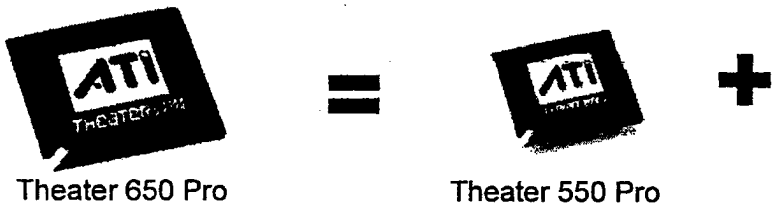
Once video is compressed to MPEG-2 format it must be written to disk, either a local hard disk, a local optical disk or a network disk. Current PC architecture requires that video data

from add-in TV tuner boards be sent across either internal buses such as PCI or PCI Express, or over USB to be written to disk or host buffer. PCI Express is the bus of choice due to its lower cost and much higher bandwidth relative to PCI or USB. It is extremely important that the bus and disk/buffer have sufficient bandwidth to keep up with the streaming video, otherwise frame drops may occur and degrade the perceived video quality.

It is clear from the above that there are a number of challenges to implementing high quality video capture on a PC platform. In the following section, we shall introduce the new Theater 650 Pro integrated circuit and explore how this product addresses the challenges.

Theater 650 Pro and the ATI Avivo™ advantage for video capture

The Theater 650 Pro is ATI's next generation solution for unprecedented home-theater quality TV on your PC. As a successor to the highly successful Theater 550 Pro and the latest addition to ATI's exclusive Avivo™ platform, the Theater 650 Pro delivers superior features and performance for video capture and digital encoding, at unparalleled levels of integration.



Exceptional Digital TV | High-quality analog TV | Windows Vista™ Premium Logo | Worldwide support | Programmable encoder

As a leading supplier of video processing components to both PC and consumer electronics markets, ATI offers a unique combination of capabilities and expertise unmatched in the industry. For the Theater 650 Pro this translates into a comprehensive and tightly-integrated feature set encompassing the entire front end of the video pipeline:

- IF demodulation
- Analog and digital video capture and encode
- Complete worldwide TV standards support
- Sophisticated video preprocessing
- MPEG encoding
- Advanced bus interfaces

We'll now examine in more detail some of the key features and benefits of the Theater 650 Pro and see how they contribute to a superior video experience for media PC applications.

Worldwide support for both analog and digital broadcast formats

The Theater 650 Pro supports all major analog television standards (NTSC/PAL/SECAM) and both ATSC and DVB-T digital HD broadcast standards, and is thus optimized to support the creation of hybrid tuner solutions using both an analog and a digital tuner on a single board.

Intermediate-Frequency (IF) Demodulation

Digital IF demodulation of standard-definition (NTSC/PAL/SECAM) analog signals is carried out within the Theater 650 Pro chip, which as described earlier provides advantages over alternative solutions which implement IF demodulation within the tuner. The Theater 650 Pro is able to separate audio and video (A/V) signals in the digital domain with near-perfect precision with only a single analog-to-digital converter (ADC), virtually eliminating any cross-talk (undesirable interference) between A/V carriers.

For capture of digital HD (ATSC and DVB-T) signal formats, the Theater 650 Pro can be seamlessly paired with external tuner/demodulator solutions such as the ATI Theater 314, recently tapped as the best performing ATSC demodulator in FCC testing.

High-Resolution Video Decoder with 12-bit ADC

Translating the demodulated analog broadcast signal into the digital realm is the job of the video decoder. Theater 650 Pro integrates high performance analog-to-digital converters (ADCs) with 12-bit per channel resolution, which offers precise video capture with more realistic color and without the visible banding or color artifacts associated with the lower-resolution 8- or 10-bit ADCs employed in competing solutions.

Advanced Motion-Adaptive 3D Comb Filter

The Theater 650 Pro employs a high-performance 3D motion-adaptive comb filter for separating the luma (Y) and chroma (C) components from a composite video stream, delivering quality levels typically found only in high-end television receivers. The filter combines a 5-line 2D comb filter, a temporal (3D) frame comb filter, a comb filter blender, and a pixel-based motion detection engine for exceptional image sharpness and detail for both still and moving images.

The key to the exceptional performance of the Theater 650 filter is a sophisticated algorithm for detecting, on a per-pixel basis, the presence of motion within the scene and adjusting the filtering technique accordingly. When no motion is detected between two adjacent frames, the filter will engage both the 2D and frame comb filters, utilizing the resultant inter- and intra-frame data to provide sharp images with minimal flicker artifacts. When motion is detected, the 2D filter alone is used to avoid motion artifacts such as blurring. In cases where motion detection is less reliable (such as when noise is present in the video) both the 2D and frame comb filters will be engaged and their outputs blended, resulting in an output image that is more pleasing than if either 2D or 3D filtering were applied alone.

Fig.2 below illustrates the performance advantage of the Theater 650 Pro 3D filtering relative to competing solutions. Note that with Theater 650 Pro fine detail is preserved resulting in a clearer, sharper image.

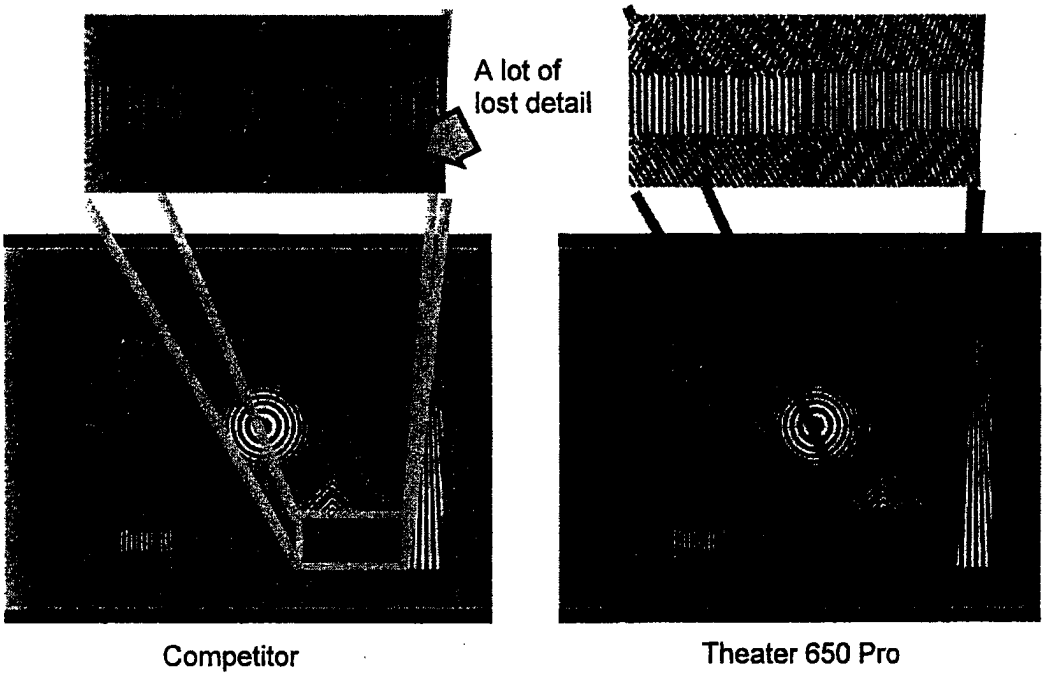
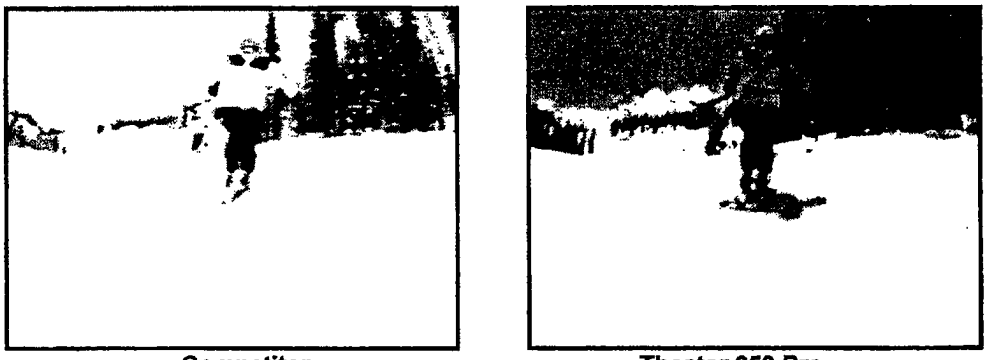


Fig.2 – Comparative 3D comb filter performance on reference test pattern

Automatic Gain Control (AGC)

The purpose of AGC is to smooth out the incoming video in case there are fluctuations in signal strength, brightness, or intensity of an image. When an AGC is implemented properly, the user should not notice any major changes in brightness when changing channels or when there is a sudden change in the color on the screen. The Theater 650 Pro employs an advanced AGC algorithm which provides superior signal control relative to competitive solutions resulting in clearer more vibrant images, as illustrated in Fig.3 below.



Competitor Theater 650 Pro

Fig.3 – AGC performance for Theater 650 Pro vs. competition

Hardware-based MPEG-2 Encoding

The Theater 650 Pro performs full on-chip MPEG-2 encoding of both video and audio in dedicated hardware, significantly reducing the impact of this computationally-intensive operation on the system CPU. Also, by combining the audio encoding process on the same hardware as the video, perfect synchronization is achieved on every recording.

Noise Reduction

Noise in the video signal, aside from impacting image quality, has the effect of reducing the coding efficiency of the MPEG encoder. The Theater 650 Pro contains dedicated hardware to identify and minimize noise prior to encode, and as a result will effectively increase disk storage density by up to 20% or more. In practical terms this means that, with noise reduction enabled, 2 hours of MPEG-2 content (i.e., DVD movie) can be stored as opposed to approximately 1 hr 40 minutes of content if no noise reduction is applied prior to encoding (see Fig.4 below).

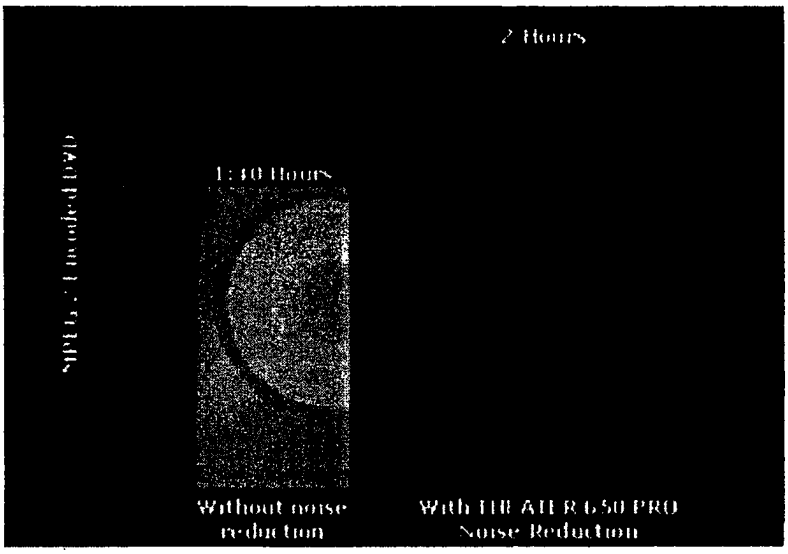


Fig.4 – MPEG-2 Storage Density with and without noise reduction

Conclusion

The growing popularity of media PCs as a platform for TV viewing is creating a demand for better video processing and a more satisfying TV experience overall. As we have shown, PC manufacturers confront numerous problems due to a multitude of TV standards worldwide (both analog and digital), stiff technical challenges in signal tuning, demodulation, and decoding, and the often conflicting requirements for maintaining high signal quality throughout the pipeline at reasonable cost.

Leveraging the extensive experience gained by ATI in both the PC and consumer electronics industries, the Theater 650 Pro provides the solutions manufacturers need for bringing high quality TV to the PC. Industry-leading video quality is achieved with innovations in motion-adaptive 3D comb filtering, digital IF demodulation, noise reduction, and high-resolution video decoding. Comprehensive support for hybrid tuners and worldwide TV standards provides manufacturers and users maximum flexibility and cost savings. Additional value is provided with features such as PCI Express bus and Microsoft Windows Vista Premium logo support.

As video becomes an ever more important part of the PC experience, high-quality processing throughout the video pipeline becomes critical. The Theater 650 Pro from ATI is engineered to meet this challenge and ensures a high-fidelity TV experience on the PC.

Exhibit 3

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MPEG LA®

VIA FACSIMILE

April 23, 2004

Mr. Richard A. Brait
General Counsel
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, ON L3T 7X6
Canada

Dear Mr. Brait,

MPEG LA has previously been in touch with ATI Technologies Inc. concerning the use of MPEG-2 technology in ATI's products. Unfortunately, we have not heard from anyone at ATI in a very long time and ATI's MPEG-2 products remain unlicensed. Therefore, as I understand that you are the new General Counsel at ATI, I hope you will able to assist me.

In that regard, I would like to re-open the lines of communication in order begin a constructive discussion regarding ATI's need for the MPEG-2 Patent Portfolio License. Therefore, please let me know how you wish to proceed. I will be glad to discuss this matter via telephone, fax, email or in person. Simply let me know what is most convenient for you.

We at MPEG LA stand ready to assist ATI in meeting its MPEG-2 intellectual property obligations and I personally look forward to your reply setting forth the next steps.

Best regards,

John Hanshaw
Licensing Associate, MPEG LA
jhanshaw@mpegla.com

Exhibit 4

US005091782A

United States Patent [19]

Krause et al.

[11] Patent Number: 5,091,782

[45] Date of Patent: Feb. 25, 1992

[54] APPARATUS AND METHOD FOR ADAPTIVELY COMPRESSING SUCCESSIVE BLOCKS OF DIGITAL VIDEO

[75] Inventors: Edward A. Krause, San Diego; Woo H. Paik, Encinitas, both of Calif.

[73] Assignee: General Instrument Corporation, Hatboro, Pa.

[21] Appl. No.: 507,258

[22] Filed: Apr. 9, 1990

[51] Int. Cl.[5] H04N 7/12; H04N 7/18

[52] U.S. Cl. 358/135; 358/136; 358/105; 382/56

[58] Field of Search 358/133, 135, 136, 105; 382/56

[56] References Cited

U.S. PATENT DOCUMENTS

3,439,753	4/1969	Mounts et al.	325/38
4,546,386	10/1985	Matsumoto et al.	358/136
4,651,206	3/1987	Ohki	358/136
4,707,738	11/1987	Ferre et al.	358/135
4,802,006	1/1989	Iinuma et al.	358/135
4,816,906	3/1989	Kummerfeldt et al.	358/136
4,827,340	5/1989	Pirsch	358/136
4,837,618	6/1989	Hatori et al.	358/135
4,862,264	8/1989	Wells et al.	358/138
4,887,156	12/1989	Ohki	358/133
4,897,720	1/1990	Wu et al.	358/136
4,933,759	6/1990	Van der Meer et al.	358/105
4,962,465	7/1990	Ohta	358/133
4,984,076	1/1991	Watanabe et al.	358/133

FOREIGN PATENT DOCUMENTS

0105604	4/1984	European Pat. Off. .
0237989	9/1987	European Pat. Off. .

OTHER PUBLICATIONS

"Scene Adaptive Coder", Chen and Pratt, *IEEE Transactions on Communications*, vol. COM-32, No. 3, Mar. 1984.

"Fixed and Adaptive Predictors for Hybrid Predictive/Transform Coding", Ericsson, *IEEE Transactions on Communications*, vol. COM-33, No. 12, Dec. 1985.

"A Motion-Compensated Interframe Coding Scheme for Television Pictures", Ninomiya and Ohtsuka, *IEEE Transactions on Communications*, vol. COM-30, No. 1, Jan. 1982.

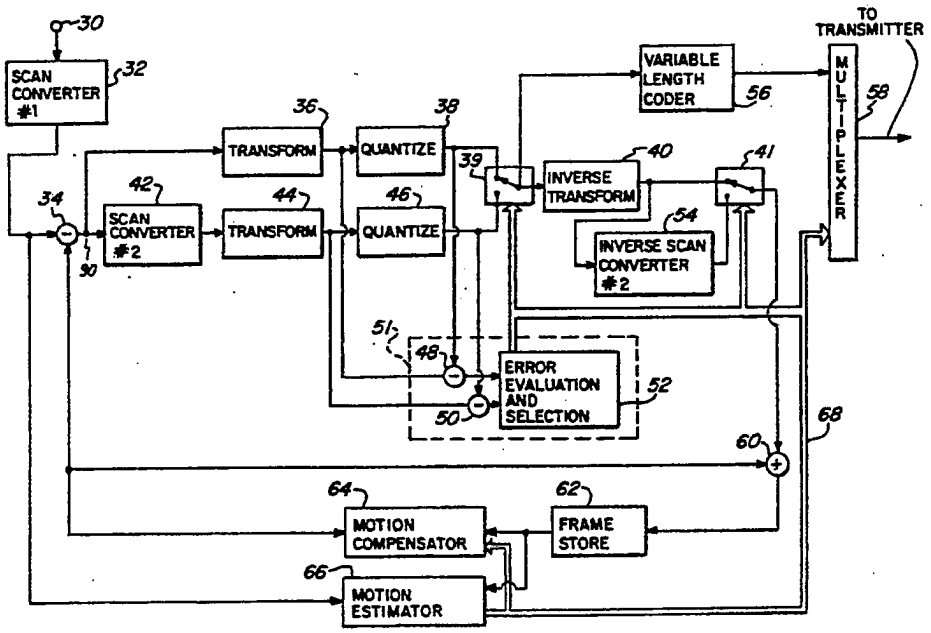
Primary Examiner—John K. Peng

Attorney, Agent, or Firm—Barry R. Lipsitz

[57] ABSTRACT

The compression of successive blocks of digital data is optimized by selecting between different compression algorithms or different data formats on a block-by-block basis. In one application, digitized interlaced video signals are processed for transmission in a compressed form. A set of pixel data presented in a field format is compressed to provide a first compressed video signal. The set of pixel data is also presented in a frame format and compressed to provide a second compressed video signal. Errors are evaluated in the first and second compressed video signals. The compressed video signal having the least error is selected for further processing. The technique is repeated for successive sets of pixel data and the selected signals are encoded to identify them as field formatted or frame formatted signals. The encoded selected signals are then combined to provide a compressed video signal data stream for transmission. Apparatus for receiving and decoding the signals is also disclosed.

33 Claims, 8 Drawing Sheets



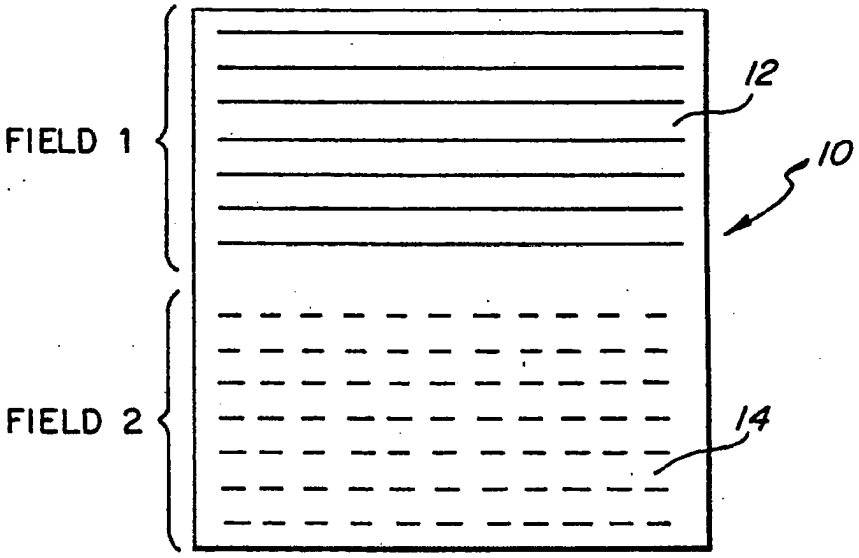


FIG. 1

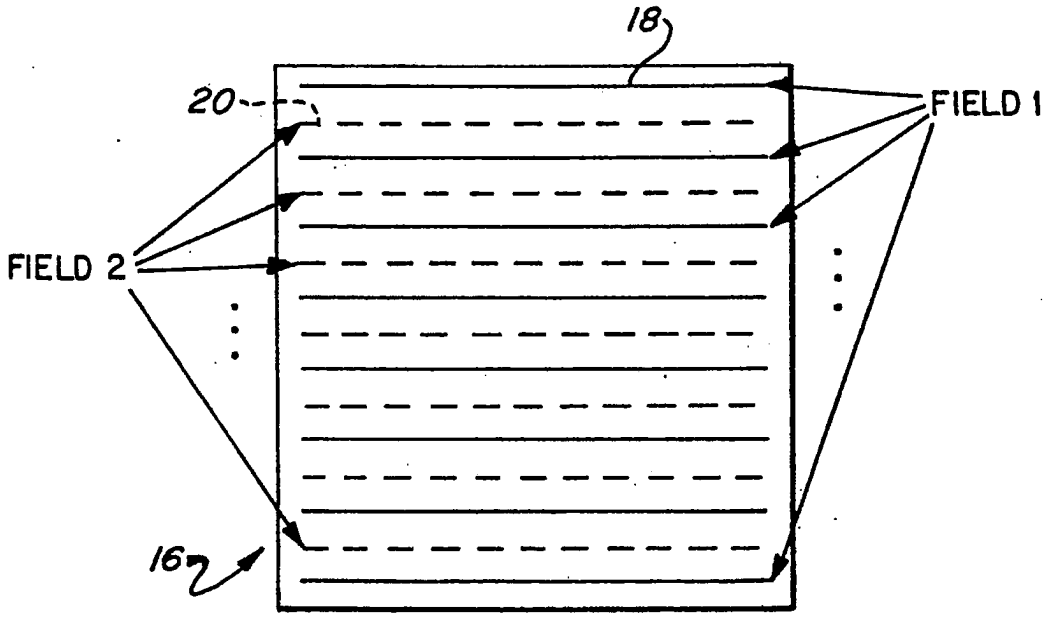


FIG. 2

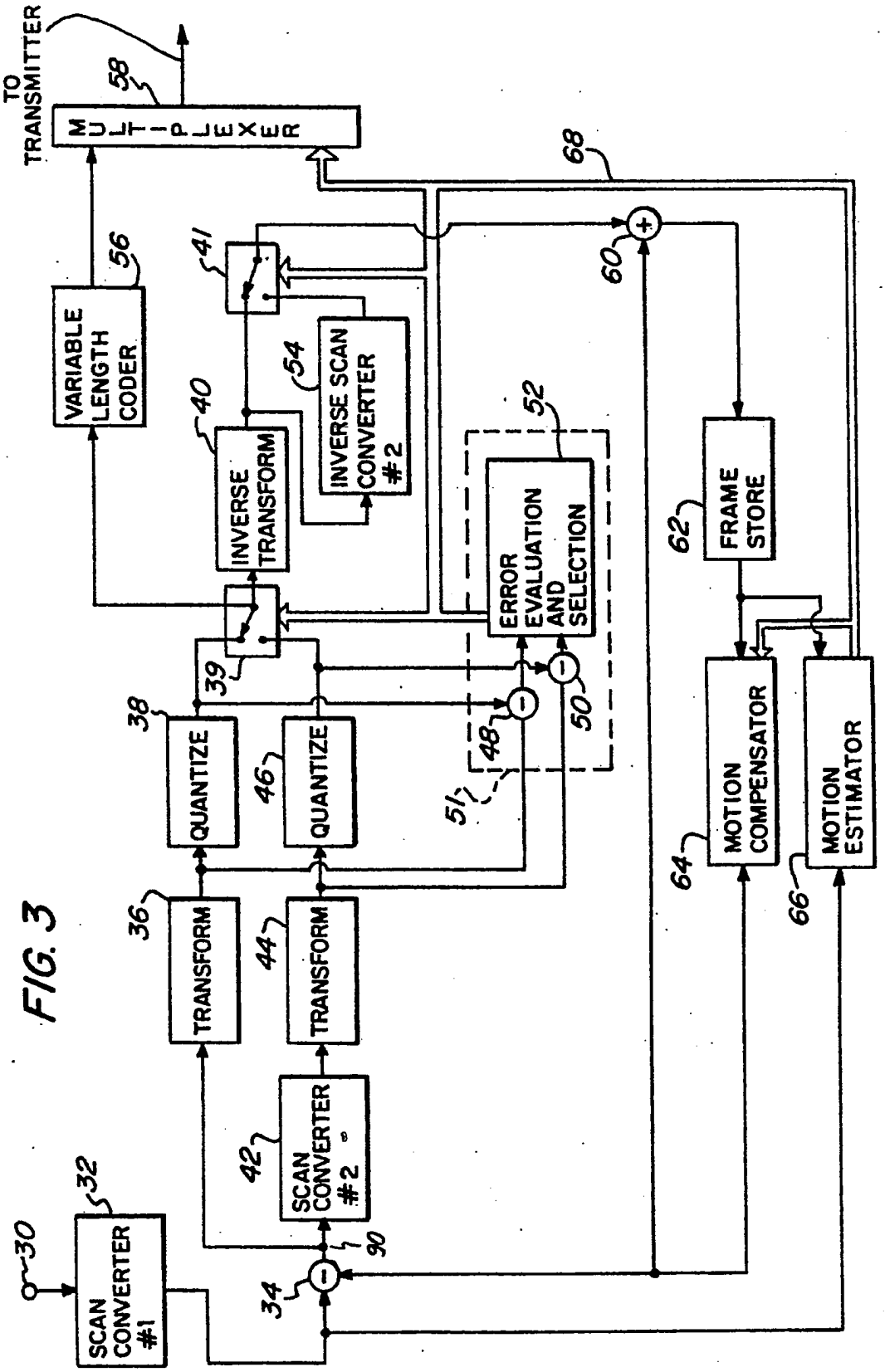


FIG. 3

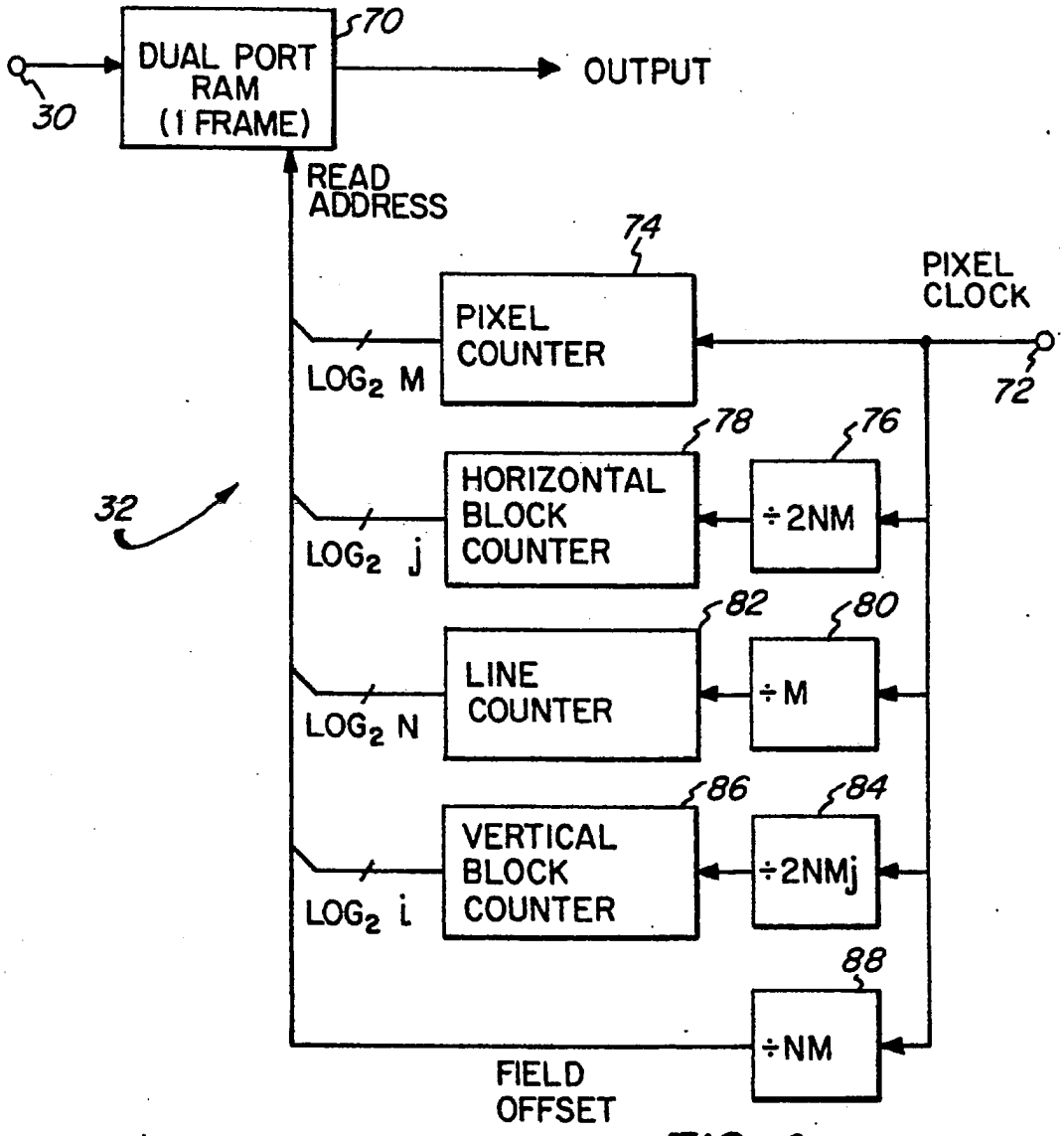


FIG. 4a

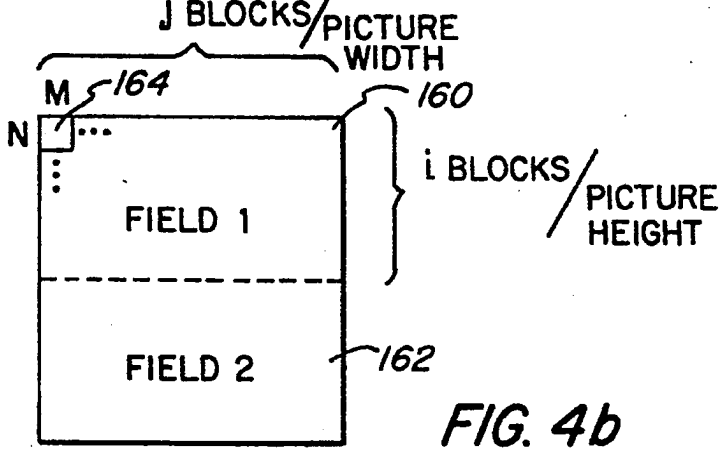


FIG. 4b

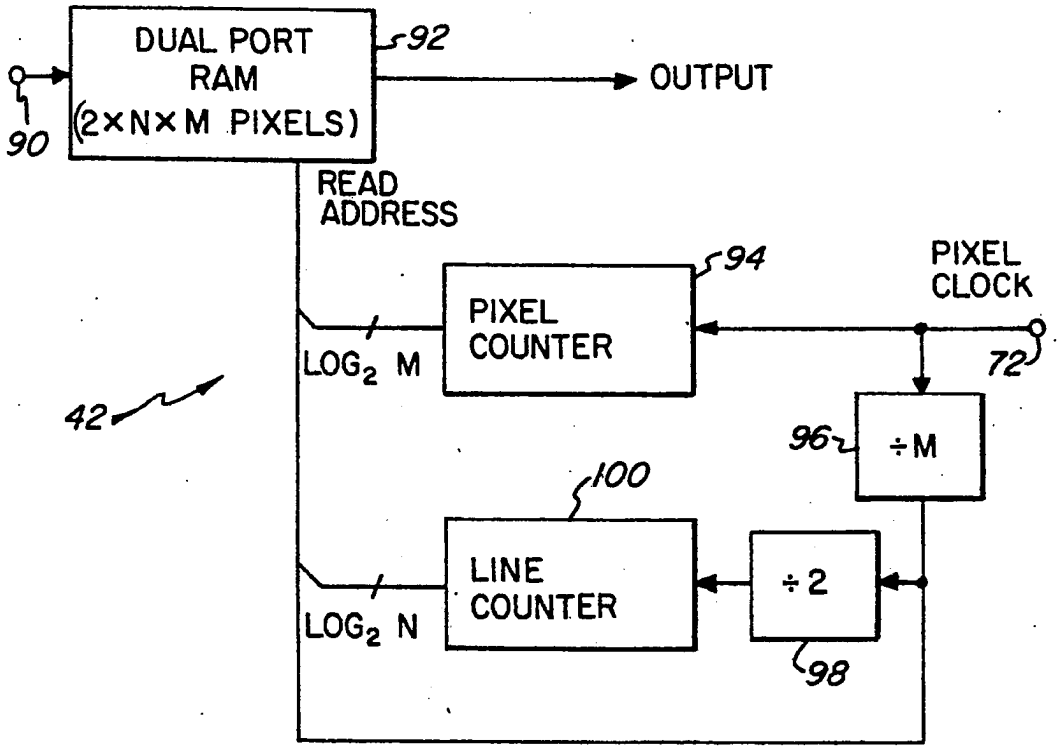


FIG. 5a

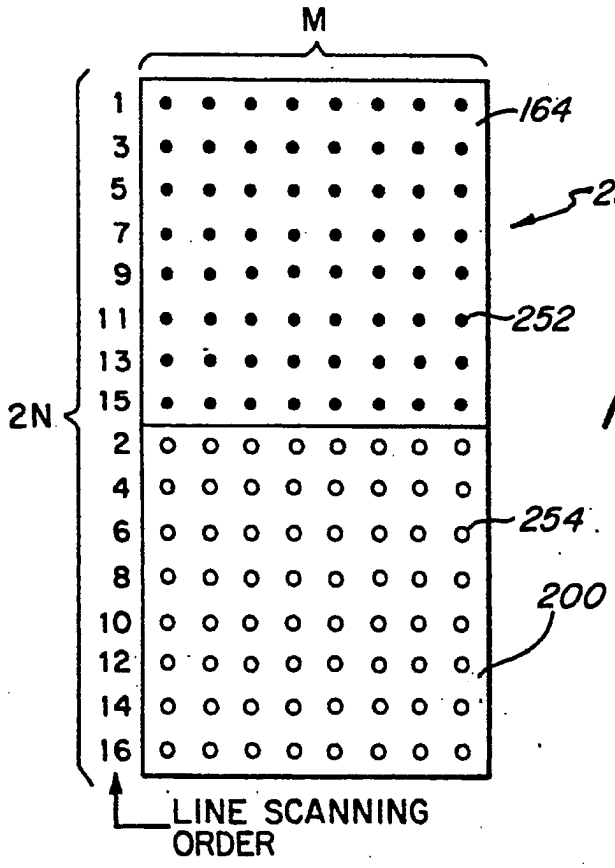


FIG. 5b

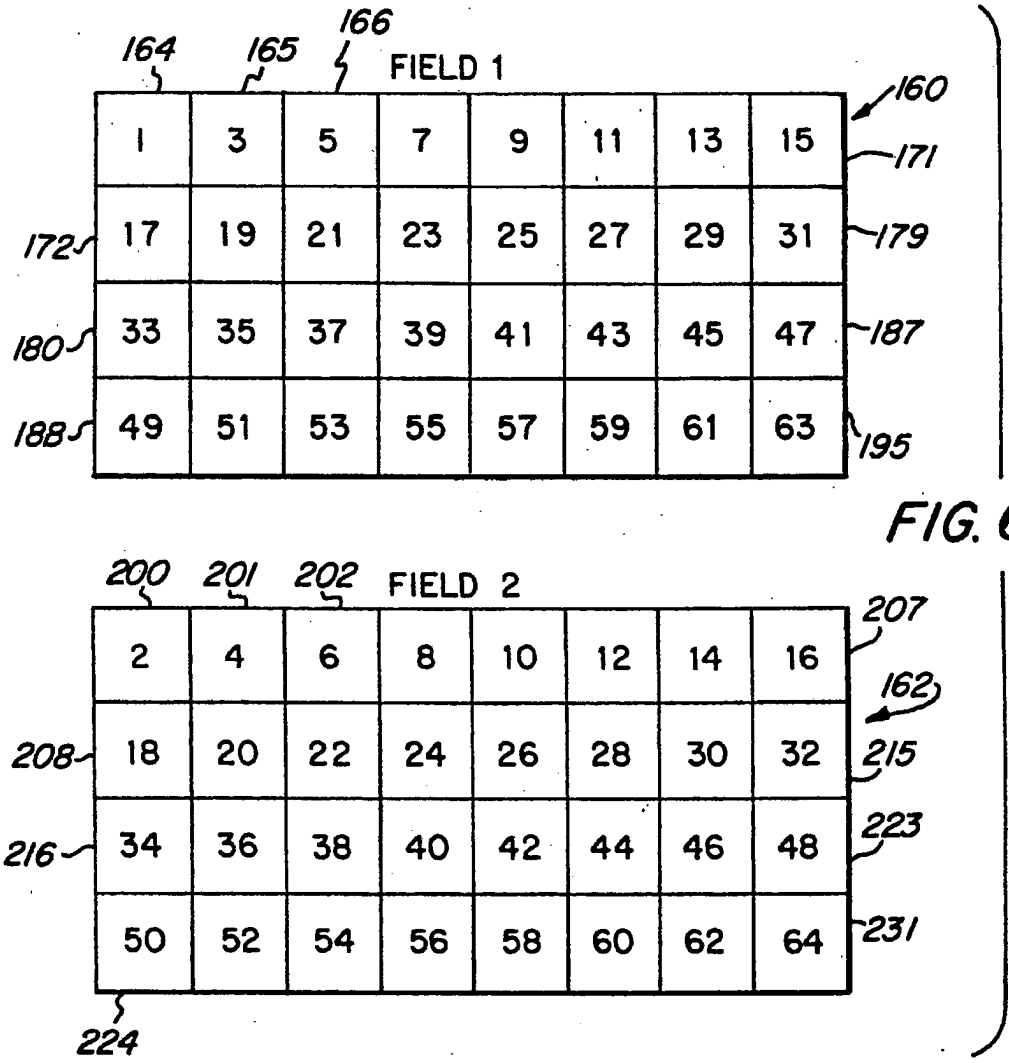


FIG. 6

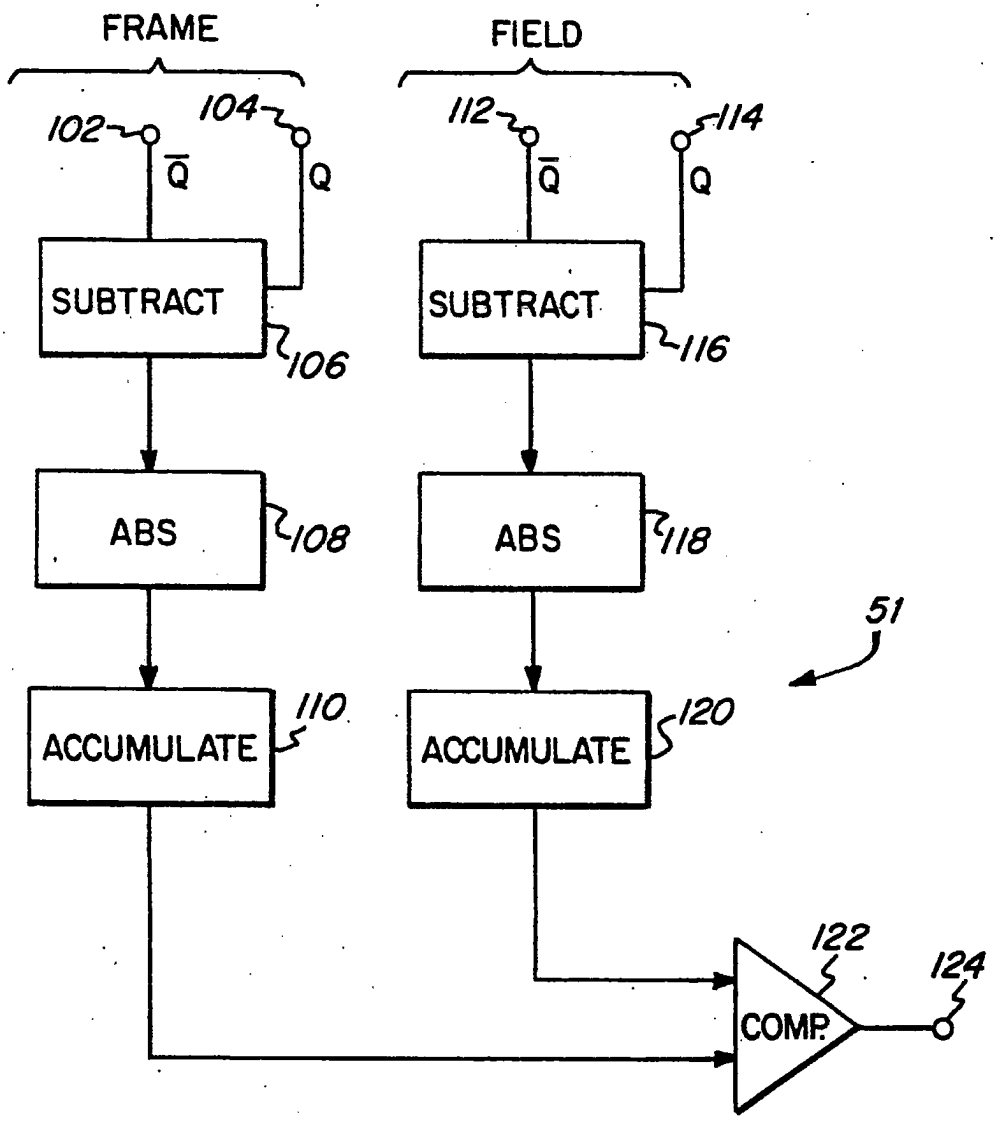


FIG. 7

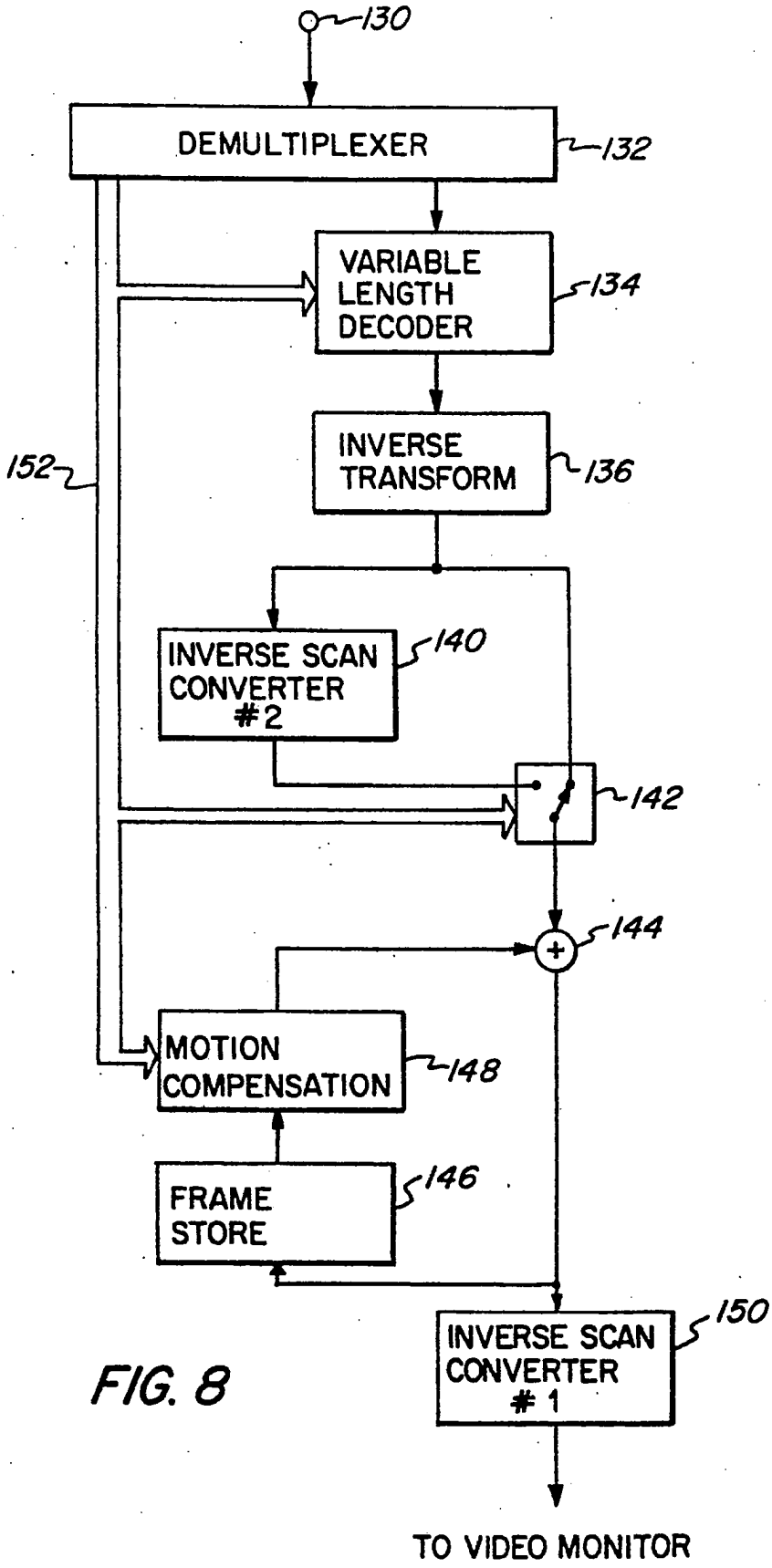


FIG. 8

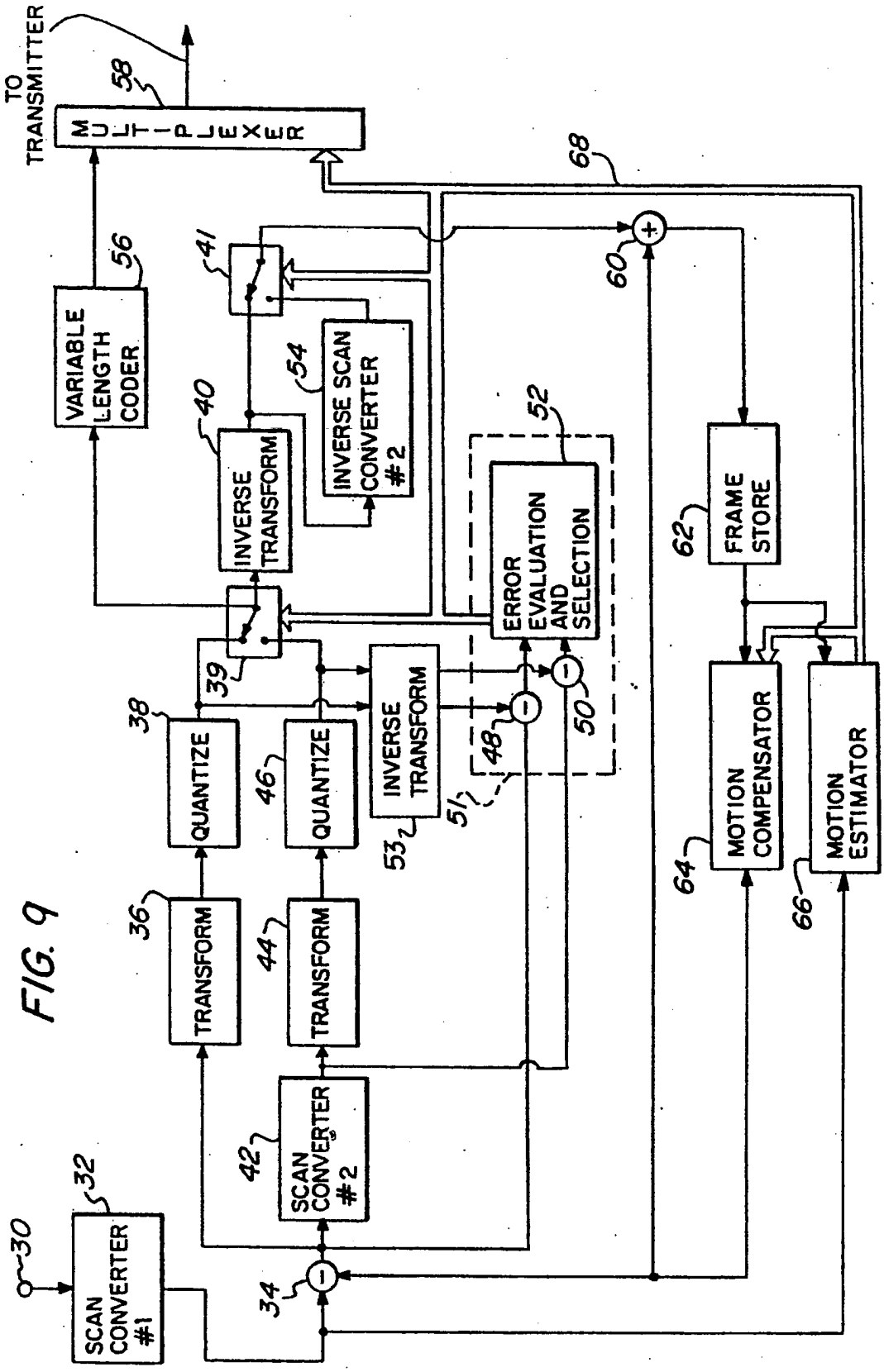


FIG. 9

APPARATUS AND METHOD FOR ADAPTIVELY COMPRESSING SUCCESSIVE BLOCKS OF DIGITAL VIDEO

BACKGROUND OF THE INVENTION

The present invention relates to the compression of digital video, and more particularly to a method and apparatus for processing digitized interlaced video signals for transmission in a compressed form.

Television signals are conventionally transmitted in analog form according to various standards adopted by particular countries. For example, the United States has adopted the standards of the National Television System Committee ("NTSC") while most European countries have adopted either PAL (Phase Alternating Line) or SECAM standards.

Digital transmission of television signals can deliver video and audio services of much higher quality than analog techniques. Digital transmission schemes are particularly advantageous for signals that are broadcast by satellite to cable television affiliates and/or directly to home satellite television receivers. It is expected that digital television transmitter and receiver systems will replace existing analog systems just as digital compact discs have largely replaced analog phonograph records in the audio industry.

A substantial amount of digital data must be transmitted in any digital television system. This is particularly true where high definition television ("HDTV") is provided. In a digital television system where signals are transmitted by satellite, the television signals can be transmitted using a quadrature phase shift keyed ("QPSK") modulated data stream. A subscriber to the system receives the QPSK data stream via a receiver/descrambler which provides video, audio, and data to the subscriber. In order to most efficiently use the available radio frequency spectrum, it is advantageous to compress the digital television signals to minimize the amount of data that must be transmitted.

Video compression techniques have been used in the past for video teleconferencing and other specialized applications. Such systems are capable of very high compression ratios, but generally exhibit limited spatial resolution and poor motion rendition. This is usually a result of initial constraints imposed on the frame rate and on the horizontal and vertical sampling rates of the system. A video "frame" can be likened to one of a sequence of snapshots that together provide a moving picture. Each frame is sampled in both the horizontal and vertical direction to obtain all of the picture information contained therein.

Video compression systems are currently under development for digital transmission of existing television signals and future high definition television signals. Such television signals are significantly more complex than teleconferencing signals and are much more difficult to compress. The performance of digital compression systems in television applications is highly scene dependent. In order to succeed, a compression algorithm should be able to adapt to specific conditions to increase compressibility and to mask invariable errors in a manner that will not be perceivable to a human viewer.

Highly detailed moving objects in a television picture present the greatest challenge to a compression system. The most powerful compression systems currently available (i.e., those that achieve the greatest reduction in the amount of data necessary to define television pictures) utilize interframe processing in order to take advantage of the temporal correlation between successive frames. However, frame-to-frame correlation is reduced when there is movement. This requires more complicated processing to maintain a high degree of performance.

Video compression is further complicated with television signals since interlaced scanning is used to define a television picture. Each frame of a television picture comprises a plurality of horizontal lines (e.g., 525 lines in a standard NTSC television signal) which together form a picture. The horizontal lines are divided into even and odd fields, wherein the even lines (lines **2, 4, 6,** . . .) form the even field and the odd lines (lines **1, 3, 5,** . . .) form the odd field. The even and odd fields are scanned in an alternating order to interleave the even and odd lines and provide the picture information in a proper sequence. The use of interlaced scanning complicates the compression of television signals as compared to previous teleconferencing applications, in which the compression was not performed on an interlaced signal.

A digitized interlaced television signal can be compressed in various formats. In one format, referred to herein as the "field format", each frame is separated into its two fields which are processed independently. In another format, referred to as the "frame format", the two fields are processed as a single frame by interleaving the lines of corresponding even and odd fields. Neither option is entirely satisfactory for video compression. Frame processing works better than field processing when there is little or no motion. Since each frame has twice the number of lines or samples than a field for a given picture height, there will be more correlation between samples and hence, compressibility is increased. To achieve the same accuracy as frame processing, field processing requires a higher bit rate. Thus, for equal bit rates frame processing achieves greater accuracy.

Frame processing enjoys similar advantages over field processing if horizontally moving features have little horizontal detail or if vertically moving features have little vertical detail. In regions where there is little detail of any sort, frame processing often works better than field processing no matter how rapidly changes occur.

In detailed moving areas, it is generally more efficient to compress field formatted data. In such cases, frame processing suffers from spurious high vertical frequencies introduced by the interleaving of the even and odd fields. This reduces the correlation between lines and therefore the effectiveness of the compression algorithm.

It would be advantageous to provide a compression system that combines the advantages of frame processing where there is little or no motion with the advantages of field processing in detailed moving areas. It would be further advantageous to provide such a system that permits video signals to be compressed and then reconstructed without any degradation in motion rendition.

It would also be advantageous to provide a general purpose compression system for optimizing the compression of digital data by combining different compression techniques or data formats to obtain peak performance under different conditions. The present inven-

tion provides a method and apparatus for achieving such advantages.

SUMMARY OF THE INVENTION

In accordance with the present invention, apparatus is provided for optimizing the compression of successive blocks of digital video. The video blocks are compressed in a first data path to provide a first compressed signal and in a second data path to provide a second compressed signal. Errors in the first and second compressed signals are evaluated, and the compressed signal having the least error is selected for each video block. The selected signals are then combined to provide a compressed digital data stream.

Each selected signal is encoded with data indicative of the data path in which the signal originated. Receiver apparatus for decoding the compressed digital data stream comprises means for detecting the encoded data from each selected signal to identify whether the signal originated in the first or second data path. Means responsive to the detecting means decompresses the selected signals from the first data path in a corresponding first decompression path. Similarly, signals selected from the second data path are decompressed in a corresponding second decompression path. The first and second data paths can use different compression algorithms. Alternately, the same compression algorithm can be applied in each path to data that is provided to the paths in different formats. In either case, the first and second decompression paths will use decompression algorithms or data formats that correspond to those of the respective first and second data paths.

In a preferred embodiment, the apparatus and method of the present invention process digitized interlaced video signals for transmission in a compressed form. The transmitted compressed signals are decoded at a receiver for reconstruction of the original interlaced video signals.

A digitized interlaced video signal is divided at the transmitter into blocks of pixel data. The blocks are formatted into a field format and compressed to provide a first compressed video signal. The blocks are also formatted in a frame format and compressed to provide a second compressed video signal. Errors in the first and second compressed video signals are evaluated, and the compressed video signal having the least error is selected for each block. The selected signals are encoded to identify them as field formatted or frame formatted signals. The encoded signals are combined to provide a compressed video signal data stream for transmission.

Motion compensation can be provided to increase the compression efficiency. With motion compensation, pixel data for a current video frame contained in the digitized interlaced signal is predicted from pixel data of a previous frame. The predicted pixel data is subtracted from the actual pixel data for the current frame to provide an abbreviated set of pixel data for use in producing the first and second compressed video signals. The selected signals are encoded with motion vector data generated during the prediction step.

At a receiver, the combined and coded signals are decoded. Field formatted signals are processed in a decoder path adapted for field processing of data. Frame formatted signals are processed in a decoder path adapted for frame processing of data. The appropriate decompressed data (field processed or frame processed) for each data block is then combined.

Motion vector data is retrieved at the receiver from encoded selected signals representing a current video frame. Data representing a previous video frame is stored. Prediction signals are computed from the retrieved motion vector data and the stored data. The prediction signals are added to the decompressed signals, and the resultant signals are formatted to reconstruct the original digitized interlaced video signal.

Field formatting of data at the transmitter can be accomplished by dividing the digitized interlace video signal into even and odd blocks of pixel data corresponding to even and odd fields of a video frame. The even and odd blocks are then provided to a first compressing means in an alternating order defining the field format. Frame formatted data can be provided by grouping the blocks into corresponding odd/even block pairs, and scanning the odd and even lines of pixel data from each pair in an alternating order. The resultant interleaved lines of frame formatted data from successive block pairs are provided to a second compressing means.

One compression algorithm that may be used in connection with the present invention is the Discrete Cosine Transform ("DCT"), in which case the first and second compressing means produce and quantize respective first and second arrays of transform coefficients for the pixel data. The error evaluating means determine the error between the quantized transform coefficients and the unquantized transform coefficients of each array. The error may be computed from the difference between each coefficient in an array before and after quantization, and selection between field processed and frame processed data can be made by comparing the sum of the absolute value of all the coefficient differences in the first array to the sum of the absolute value of all the coefficient differences in the second array. The array having the least total error is chosen for transmission.

The error evaluating means can alternatively operate in the pixel domain, by inverse transforming the first and second arrays to recover the pixel data. In this case, the error for the respective field and frame processing paths is determined by comparing the pixel data recovered from each array to the original set of pixel data presented to the compression means.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is an illustration depicting a video frame separated into odd and even fields for field processing of pixel data;

FIG. **2** is a diagram illustrating a video frame having interleaved even and odd lines for frame processing of pixel data;

FIG. **3** is a block diagram of data compression apparatus for use at a transmitter in accordance with the present invention;

FIG. **4***a* is a block diagram of circuitry that can be used to perform the function of scan converter #1 of FIG. **3**;

FIG. **4***b* is a diagram illustrating the format of pixel data blocks output from scan converter #1;

FIG. **5***a* is a block diagram of circuitry that can be used to perform the function of scan converter #2 of FIG. **3**;

FIG. **5***b* is a diagram illustrating the format of an odd/even pair of pixel data blocks provided by scan converter #2;

FIG. 6 is a diagram illustrating the order of individual pixel data blocks within the fields of a video frame;

FIG. 7 is a block diagram of error evaluation and selection circuitry that can be used in the apparatus of FIG. 3; and

FIG. 8 is a block diagram of decoder apparatus for use at a receiver to decompress transmitted digital data and reconstruct a digitized interlaced video signal.

FIG. 9 is a block diagram of data compression apparatus similar to that shown in FIG. 3, but using an alternate error evaluation scheme.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 illustrates a single video frame 10 separated into its two component fields. Field 1 designated by reference numeral 12 comprises the odd lines of the video frame. Field 2 represented by reference numeral 14 comprises the even lines of the video frame. In prior art analog television systems, each even and odd line of the video frame is defined by an analog signal modulated with image information. Sequential lines from the even and odd fields are interleaved to provide an intelligible video picture.

An interlaced video frame 16 is depicted in FIG. 2. Odd lines 18 from Field 1 are interleaved with even lines 20 from Field 2. The even and odd lines must be interleaved in this fashion in order for a proper picture to be displayed on a television screen.

The present invention concerns digitally transmitted data. In digital television systems, each line of a video frame is defined by a sequence of digital data bits referred to as "pixels". A large amount of data is required to define each video frame of a television signal. For example, 7.4 megabits of data is required to provide one video frame at NTSC resolution. This assumes a 640 pixel by 480 line display is used with 8 bits of intensity value for each of the primary colors red, green, and blue. High definition television requires substantially more data to provide each video frame. In order to manage this amount of data, particularly for HDTV applications, the data must be compressed. As noted above, different data formatting and/or compression techniques can be more efficient than others at different times during the transmission of a digital data stream. For example, field processing of video data in a format as shown in FIG. 1 is generally preferred in detailed moving areas. Frame processing, as depicted by the format of FIG. 2, generally works better than field processing when there is little or no motion. The present invention provides a system that optimizes the compression of digital television data by switching between field processing and frame processing as appropriate.

In accordance with the present invention, a standard digitized interlaced television signal is input at terminal 30 of the data compression apparatus shown in FIG. 3. The process of digitizing video signals is well known in the art. A plurality of separate digitized signals may be provided for the various components, such as luminance and chrominance, of a video signal. When the present invention is used in conjunction with multiple luminance and chrominance components, it is most important that the luminance portion of the video signal take advantage of the adaptive field and frame processing.

An image defined by the interlaced video signal is decomposed by a first scan converter 32 into blocks of a size appropriate for data compression. Any of the various data compression techniques well known in the art can be used in accordance with the present invention. The most popular compression technique is known as the Discrete Cosine Transform ("DCT"). This technique is described in Chen and Pratt, "Scene Adaptive Coder", *IEEE Transactions on Communications*, Vol. COM-32, No. 3, March 1984, which is incorporated herein by reference. The following description explains the invention using an 8×8 pixel block size together with the DCT compression technique.

In order to minimize complexity and memory requirements for the compression and subsequent decompression apparatus of the present invention, scan converter 32 groups the even and odd fields of each video frame into pairs. The scan converter then alternately outputs the same block from one field and then the other. This function can be implemented using the components illustrated in the block diagram of FIG. 4*a*.

The digitized interlaced video signal input at terminal 30 is formatted to provide all of the lines from the odd field (Field 1) followed by all of the lines of the even field (Field 2). This is depicted in FIG. 4*b*, which illustrates Field 1 (160) followed by Field 2 (162). The function of scan converter 32 is to divide Fields 1 and 2 into a plurality of corresponding blocks. Each block is M pixels wide by N pixels high. It takes j such blocks to cover the width of the picture and i blocks to cover the height of each field. Having established this format, scan converter 32 then outputs the blocks in alternating odd/even order, as illustrated in FIG. 6.

FIG. 6 is a detailed representation of the odd and even fields 160, 162 of FIG. 4*b* after the image has been decomposed by scan converter 32 into individual blocks of pixel data. Field 1 comprises odd blocks of pixel data and Field 2 comprises even blocks of pixel data. In the embodiment illustrated, each 8×8 block contains 64 pixels. The first block of data output from scan converter 32 for each field pair is block 164. Next, block 200 is output, followed by blocks 165, 201, 166, 202, etc. After block 231 is output from scan converter 32, the next two fields (representing the next video frame) are processed and read out in the same manner. The formatting of data by scan converter 32 as described above is referred to herein as field formatted data.

In order to provide field formatted data, scan converter 32 can comprise a dual port RAM 70 as shown in FIG. 4*a*. The data contained in a digitized interlaced video signal input at terminal 30 is loaded into RAM 70 in the order received. A read address is generated to enable the data to be read out of RAM 70 in the field format. A pixel clock signal input at terminal 72 is coupled to a pixel counter 74 that outputs a digital signal ranging from 0 to M−1. This count forms the $\log_2 M$ least significant bits of the dual port RAM read address. A divider 76 and horizontal block counter 78 produce a signal ranging from 0 to j−1 and forms the next $\log_2 j$ bits of the read address. Another divider circuit 80 and line counter 82 provide an output ranging from 0 to N−1, and forms the next $\log_2 N$ bits of the read address. Divider 84 and vertical block counter 86 provide an output ranging from 0 to i−1 to form the next $\log_2 i$ bits. Finally, divider 88 provides the most significant bit of the dual port RAM address in order to toggle between Field 1 and Field 2 of each video frame. The composite address signal input to RAM 70 requires $1+\log_2 M+\log_2 j+\log_2 N+\log_2 i$ bits. For an 8×8 block size, the pixel and line counters will both require 3 bits. The

number of bits required for the horizontal and vertical block counters will depend on the size of the fields.

The result of the above is that the read address of RAM **70** will be incremented to output the video data in a field format. Those skilled in the art will appreciate that the pixels within each block may be scanned in a different order as determined by the input requirements of the DCT algorithm or other compression device used.

Referring again to FIG. **3**, the field formatted data is output from scan converter **32** to a first compression path comprising a DCT transform coder **36** and a quantizer **38**. These are conventional elements used in DCT compression, as described in the Chen and Pratt article referred to above. The field formatted data is also input to a second compression path comprising a second scan converter **42**, a transform coder **44**, and a quantizer **46**. Transform coder **44** and quantizer **46** are identical to those in the first compression path. Prior to inputting the field formatted data to the first and second compression paths, an optional predictor signal used for motion compensation can be subtracted by a subtraction circuit **34**. The motion compensation aspect of the present invention is described in more detail below.

Scan converter **42** is used to convert the field formatted data from scan converter **32** into a frame format. In this format, corresponding pairs of blocks from the even and odd fields are interleaved on a line-by-line basis. Components for performing this operation are illustrated in FIG. **5***a*. The frame format is illustrated in FIG. **5***b*, which shows a pair of vertically adjacent blocks **250** comprising odd block **164** and corresponding even block **200**. These are the same blocks that are illustrated in a field format in FIG. **6**. Block **164** contains 64 odd pixels **252** that represent portions of the odd lines contained in a video frame. Block **200** contains 64 even pixels **254** corresponding to portions of the even lines of the video frame.

The components of FIG. **5***a* scan the lines of pixels shown in FIG. **5***b* in an alternating odd/even line scanning order to provide the interleaved frame formatted data. The field formatted data input at terminal **90** is stored by dual port RAM **92** in the order received. The pixel clock signal input at terminal **72** of FIG. **5***a* is used to strobe a pixel counter **94** to provide an output signal ranging from 0 to M−1, which serves as the $\log_2 M$ least significant bits of the dual port RAM address. The pixel clock signal is divided by M at divider **96**, and input to another divide by **2** circuit **98** for input to a line counter **100**. The line counter outputs a digital signal ranging from 0 to N−1 which forms the next $\log_2 N$ bits of the dual port RAM address. The output of divide by M circuit **96** also serves as the most significant bit of the read address input of RAM **92**. The resultant read address signal consists of $1+\log_2 N+\log_2 M$ bits. This signal causes the data stored in RAM **92** to be read out in the frame format.

As indicated in FIG. **3**, the compressed field formatted data from the first compression path is output from quantizer **38** to a switch **39**. The frame formatted data compressed in the second compression path is output from quantizer **46** to switch **39**. In accordance with the present invention, errors in the compressed data from the two different compression paths are evaluated and the data having the least error for each odd/even block pair is selected for transmission. Thus, where a portion of a video frame having little or no motion is compressed, it is likely that the pixel data processed in the frame format will be selected. Where the portion of the video frame being evaluated is from a detailed moving area, it is probable that the data compressed in a field format will be selected.

Error evaluation and selection of frame processed or field processed data is achieved using hard wired logic generally designated by reference numeral **51**. The error is determined by comparing the quantized transform coefficients to the original unquantized transform coefficients in each data path. The unquantized coefficients input to quantizer **38** are subtracted at **48** from the quantized coefficients output from quantizer **38**. Similarly, the unquantized coefficients input to quantizer **46** are subtracted at **50** from the quantized coefficients output from quantizer **46**. The results are input to an error evaluation and selection circuit **52** that compares the errors in the two paths. In an alternate embodiment illustrated in FIG. **9**, an inverse transform circuit **53** is provided to recover the pixel data from quantizers **38** and **46**. Error evaluation and selection circuit **52** then determines the error between the recovered pixel data and the original pixel data presented to the first and second compression paths. It should be appreciated that the error evaluation and selection could alternately be implemented in software.

In a preferred embodiment, the error metric used is the sum of the absolute value of all the coefficient differences. However, other metrics such as the mean squared error will also perform satisfactorily. In either case, the average error is evaluated over a two-block region. This is required because the frame formatted data comprises interleaved data from odd/even block pairs, as shown in FIG. **5***b*. Comparison of field formatted data to frame formatted data must therefore occur over the two-block region.

The error evaluation and selection components **51** are illustrated in greater detail in FIG. **7**. As noted, these may be implemented in hardware or software. Quantized (Q) and unquantized ($\bar{Q}$) data from the frame format compression path are input to terminals **104** and **102** respectively of subtraction circuit **106**. The absolute value of the difference between these signals is determined by conventional means **108**, and accumulated at **110**. Similarly, the quantized and unquantized coefficients from the field format compression path are input at terminals **114**, **112** respectively of subtraction circuitry **116**. The absolute values of the differences are computed as indicated at **118**, and accumulated at **120**. The accumulated errors from the respective frame and field formatted paths are compared at a comparator **122**, which provides an output signal at terminal **124** indicative of which path produced the least error for a particular pair of pixel data blocks.

The output signal from the error evaluation and selection components actuates switch **39** (FIG. **3**) to connect the compression path having the least error to downstream processing circuitry. Such circuitry includes variable length coder **56** that assigns variable length codewords to represent the selected sets of quantized transform coefficients. An example of such a variable length coder is described in the Chen and Pratt article referred to above.

The output of variable length coder **56** is input to a multiplexer **58** that combines the compressed data with control data carried on data path **68**. The control data includes a bit for encoding the selected compressed signals to identify them as field formatted or frame formatted signals. This can be the same bit used to actu-

ate switch 39, wherein the selection of one of the compression paths is represented by "1" and the other compression path is represented by "0".

The adaptive field/frame encoding system shown in FIG. 3 can optionally be combined with motion compensation to provide additional compression efficiencies. Motion compensation techniques are well known in the art. Such techniques are described, for example, by Staffan Ericsson in "Fixed and Adaptive Predictors for Hybrid Predictive/Transform Coding", *IEEE Transactions on Communications*, Vol. COM-33, No. 12, December 1985, and Ninomiya and Ohtsuka, "A Motion-Compensated Interframe Coding Scheme for Television Pictures", *IEEE Transactions on Communications*, Vol. COM-30, No. 1, January 1982, both incorporated herein by reference. In order to provide motion compensation, the pixel data for the current video frame is predicted by motion compensator 64 and motion estimator 66 from pixel data of a previous video frame stored in frame store 62. The predicted pixel data is subtracted from the actual pixel data for the current video frame at subtracter 34 to produce a set of pixel data representing a prediction error. The prediction error pixel data is presented to the first and second compression paths for compression and selection as described above.

In order to obtain a prediction for the next frame, an inverse transformation to the processing stream selected by the error evaluation and selection components must be computed, followed by the inverse of the second scan converter 42 in cases where frame processing was selected. The inverse transform is provided by circuitry 40, and the inverse of the second scan converter is provided by circuitry 54. Switch 41 is actuated by the output signal from error evaluation and selection circuit 52 to couple appropriately formatted data to the motion compensation circuitry. The appropriate inverse transform data is added back at adder 60 to the predictor signal that was initially subtracted from the incoming video. The result is written into frame store 62 (e.g., a shift register or RAM) where it is delayed until it can be used as a prediction for the next frame.

Block displacement information, indicative of the location of a previous block that best matches a current block of pixel data within a predefined area, is determined by a motion estimator 66 which inputs corresponding motion vector data (X, Y) to motion compensator 64. The motion vector data is also input to multiplexer 58 from motion estimator 66 via path 68. Multiplexer 58 appends the motion vector data to the encoded video signal for use in deriving an identical prediction signal at a receiver.

Since the object of motion compensation is to improve compression performance in moving areas of a video picture, it is more effective to estimate the block displacements and perform the compensation using fields instead of frames. Therefore, the displacement of each block of a given field is determined with reference to the same field of the previous frame. In some cases, better results are obtainable if the field immediately preceding the given field is chosen for the reference. In this case, an even field would be matched with an odd field, and an odd field would be matched with an even field. However, such a strategy is more difficult to implement and is not as effective when the vertical displacement is zero.

Motion compensation is performed in the same manner regardless of whether field processing or frame processing is chosen for encoding. A prediction is obtained for each block of a given field by utilizing the estimated displacement vector to identify the matching block in the same field of the previous frame. In cases where frame processing is chosen for encoding, the prediction errors from two different fields are eventually interleaved by the second scan converter 42.

The compressed, encoded signals are output from multiplexer 58 to a transmitter (not shown). The transmitted signal is received by a digital television receiver, and the signals are decoded by a decoder such as that shown in FIG. 8. The received digital signals are input at terminal 130 to a demultiplexer 132 which separates the encoded control signals from the video data signals. A variable length decoder 134 recovers the quantized transform coefficients. Recovered coefficients for field processed blocks are decompressed in a first decompression path comprising inverse transform coder 136 and switch 142. Recovered coefficients for frame processed blocks are decompressed in a second decompression path comprising inverse transform coder 136, inverse scan converter 140, and switch 142. Inverse scan converter 140 is a memory device that restores the order of pixels resulting from the use of the second scan converter 42 at the encoder back to the original scanning order. The control data bit identifying each pixel data block as frame processed or field processed actuates switch 142 via path 152 to apply the appropriate decompressed data from the first decompression path or second decompression path to an inverse scan converter 150. This inverse scan converter is a memory device that restores the reordered pixels resulting from the use of the first scan converter 32 at the encoder back to the original raster scan order. The output of inverse scan converter 150 is the recovered, reconstructed digitized interlaced video signal originally input to the encoder. This output signal is coupled to a video monitor for display of the video program.

Motion compensation at the receiver is provided by frame store 146 and motion compensation circuitry 148. Motion vector data appended to blocks of pixel data at the encoder is retrieved by demultiplexer 132 at the receiver. The motion vector data is input via path 152 to motion compensation circuitry 148 which uses the data, together with data representing a previous video frame stored in frame store 146, to recompute the original prediction signals. The recomputed prediction signals are added to the decompressed blocks of pixel data for the current video frame at adder 144. Since the motion vector data computed by motion estimator 66 at the encoder is appended to the pixel data blocks, there is no need to provide motion estimation circuitry at the decoder, and the resultant decoder system is simplified.

It will now be appreciated that the present invention provides improved data compression techniques for use in digital data transmission, and particularly for use in the transmission of digital interlaced television signals. The invention may be advantageously used in the transmission of HDTV signals, and provides a means for substantially reducing the amount of data that must be transmitted to define HDTV television pictures.

A selection between frame processing and field processing based on achieving minimum error in accordance with the prevent invention has been found to be very effective in improving the picture quality of digitally compressed television signals. Still or slowly moving regions are rendered much more accurately than would be possible in a field processing system. Motion

rendition is much better than would be possible in a frame processing system. Since the selection is made on a local basis, the system can adjust to scenes containing both moving and nonmoving features.

Those skilled in the art will appreciate that numerous modifications and adaptations may be made to the system described without departing from the spirit and scope of the appended claims. For example, in order to choose between frame and field processed data, block error can be evaluated in the pixel domain. In this instance, instead of comparing transform coefficients, each block of data can be inverse transformed and then compared to the original block of pixels.

We claim:

1. Apparatus for processing digitized interlaced video signals for transmission in a compressed form comprising:
- first means for compressing a set of pixel data presented in a field format to provide a first compressed video signal;
- second means for compressing said set of pixel data presented in a frame format to provide a second compressed video signal;
- means coupled to said first means for evaluating errors in the first compressed video signal and coupled to said second means for evaluating errors in the second compressed video signal; and
- means responsive to said error evaluating means for selecting the compressed video signal having the least error.

2. Apparatus in accordance with claim 1 wherein:
- successive sets of pixel data are sequentially compressed and evaluated; and
- said selecting means selects the compressed video signal having the least error for each particular set.

3. Apparatus in accordance with claim 2 further comprising:
- means for encoding the selected signals to identify them as field formatted or frame formatted signals.

4. Apparatus in accordance with claim 3 further comprising:
- means for combining the encoded selected signals to provide a compressed video signal data stream for transmission.

5. Apparatus in accordance with claim 4 further comprising:
- means for dividing a digitized interlaced video signal into even and odd blocks of pixel data corresponding to even and odd fields of a video frame; and
- means for presenting said even and odd blocks to said first compressing means in an alternating order defining said field format.

6. Apparatus in accordance with claim 5 further comprising:
- means for grouping said blocks into corresponding odd/even block pairs and scanning the odd and even lines of each pair in an alternating order to provide interleaved lines of pixel data; and
- means for presenting the interleaved lines of pixel data from successive block pairs to said second compressing means.

7. Apparatus in accordance with claim 6 wherein said sets each comprise two vertically adjacent blocks of pixel data from a video frame.

8. Apparatus in accordance with claim 1 wherein:
- said first and second compressing means produce and quantize respective first and second arrays of transform coefficients for the set of pixel data; and
- said error evaluating means determines the error between the quantized transform coefficients and the unquantized transform coefficients of each array.

9. Apparatus in accordance with claim 8 wherein:
- said error evaluating means determines said error by computing the difference between each coefficient in an array before and after quantization; and
- said selecting means compares the average error of all the coefficient differences in said first array to the average error of all the coefficient differences in said second array to identify the array having the least total error.

10. Apparatus in accordance with claim 1 wherein:
- said first compressing means produces a first array of transform coefficients for said set of pixel data;
- said second compressing means produces a second array of transform coefficients for said set of pixel data; and
- said error evaluating means comprises:
  - means for inverse transforming said first and second arrays to recover the pixel data, and
  - means for determining the error between the pixel data recovered from each array and the original set of pixel data presented to the first and second compressing means.

11. Apparatus in accordance with claim 1 further comprising:
- means for receiving a digitized interlaced video signal containing pixel data defining a sequence of video frames;
- means for predicting the pixel data for a current video frame from pixel data of a previous video frame;
- means for subtracting the predicted pixel data from the actual pixel data for the current video frame to produce a set of pixel data representing a prediction error;
- means for presenting the prediction error pixel data to said first compressing means in a field format; and
- means for presenting the prediction error pixel data to said second compressing means in a frame format.

12. Apparatus in accordance with claim 11 further comprising:
- means for dividing each video frame of the digitized interlaced video signal into successive blocks of pixel data for processing on a block-by-block basis by said predicting, subtracting and presenting means.

13. Apparatus in accordance with claim 11 further comprising:
- means for encoding the selected signals with motion vector data generated by said predicting means.

14. Apparatus in accordance with claim 13 further comprising:
- means for encoding the selected signals to identify them as field formatted or frame formatted signals.

15. Apparatus in accordance with claim 14 further comprising:
- means for combining the encoded selected signals to provide a compressed video signal data stream for transmission.

16. Apparatus for optimizing the compression of successive blocks of digital data comprising:
- means for compressing data blocks in a first data path to provide a first compressed signal;

means for compressing said data blocks in a second data path to provide a second compressed signal;

means for evaluating errors in the first and second compressed signals;

means responsive to said evaluating means for selecting the compressed signal having the least error for each data block; and

means for combining the selected signals to provide a compressed digital data stream.

17. Apparatus in accordance with claim 16 further comprising:

means for encoding each selected signal with data indicative of the data path in which the signal originated.

18. A receiver for decoding the compressed digital data stream from the apparatus of claim 17 comprising:

means for detecting the encoding data from each selected signal to identify whether the signal originated in the first data path or the second data path; and

means responsive to said detecting means for processing the selected signals from the first data path in a corresponding first decompression path and for processing the selected signals from the second data path in a corresponding second decompression path.

19. Apparatus in accordance with claim 18 wherein:

said first data path and first decompression path use a first algorithm for compression and decompression of said data blocks; and

the second data path and second decompression path use a second algorithm for compression and decompression of said data blocks.

20. Apparatus in accordance with claim 16 wherein:

said data blocks are provided to said first data path in a first format and to said second data path in a second format.

21. Decoder apparatus comprising:

means for receiving compressed digital video signals transmitted in blocks of frame processed pixel data and field processed pixel data;

means coupled to said receiving means for determining whether a particular block of data contained in a received signal was frame processed or field processed;

first means for decoding received blocks of field processed pixel data;

second means for decoding received blocks of frame processed pixel data; and

means responsive to said determining means for selectively combining decoded blocks from said first and second means to recover an uncompressed video signal.

22. Apparatus in accordance with claim 21 further comprising means for converting the recovered signal to a digitized interlaced video signal.

23. Apparatus in accordance with claim 21 wherein said determining means comprises means for reading field and frame processing identification data appended to said blocks.

24. Apparatus in accordance with claim 21 wherein said blocks comprise arrays of transform coefficients, and the first and second means comprise means for inverse transforming said coefficients.

25. Apparatus in accordance with claim 24 wherein the inverse transforming means is shared by said first and second means.

26. Apparatus in accordance with claim 21 further comprising:

means for retrieving motion vector data appended to received blocks of pixel data representing a current video frame;

means for storing data representing a previous video frame;

means for computing prediction signals from the retrieved motion vector data and the stored data; and

means for adding said prediction signals to the received blocks for the current video frame.

27. A digital television system comprising:

first data compression means for compressing field formatted blocks of pixel data derived from a digitized interlaced video signal;

second data compression means for compressing frame formatted blocks of pixel data corresponding to said field formatted blocks;

means for evaluating errors in compressed data from said first and second data compression means;

means responsive to said error evaluating means for selecting the compressed data for each block having the least error;

means for encoding the selected data for each block to identify it as field processed or frame processed data; and

means for combining the encoded selected data to provide a compressed video data stream containing interspersed blocks of field processed pixel data and frame processed pixel data for transmission by a transmitter.

28. The system of claim 27 further comprising:

receiver means for receiving said compressed video data stream from said transmitter;

means operatively associated with said receiver means for decoding the encoded selected data in said data stream to identify field processed blocks and frame processed blocks;

first means for processing received blocks of field processed data;

second means for processing received blocks of frame processed data; and

means responsive to said decoding means for selectively combining blocks from said first and second processing means to recover an uncompressed digitized interlaced video signal.

29. The system of claim 28 wherein said digitized interlaced video signal defines a sequence of video frames, said system further comprising:

means for predicting the pixel data for a current video frame from pixel data of a previous video frame;

means for subtracting the predicted pixel data from the actual pixel data for the current video frame to produce a set of pixel data representing a prediction error;

means for presenting the prediction error pixel data to said first data compression means as field formatted blocks;

means for presenting the prediction error pixel data to said second data compression means as frame formatted blocks;

means operatively associated with said predicting means for generating motion vector data for the current video frame;

means operatively associated with said generating means for encoding the selected data for each block with corresponding motion vector data;

means operatively associated with said receiver means for retrieving the motion vector data from each block of a current video frame;

means operatively associated with said receiver for storing data representing a previous video frame;

means for computing prediction signals from the retrieved motion vector data and the stored data; and

means for adding said prediction signals to the received blocks for the current video frame.

30. A method for encoding television signals for digital transmission comprising the steps of:

dividing a digitized interlaced video signal into blocks of pixel data;

formatting said blocks in a field format;

compressing said field formatted blocks to provide a first compressed video signal;

formatting said blocks in a frame format;

compressing said frame formatted blocks to provide a second compressed video signal;

evaluating errors in said first and second compressed video signals;

selecting, for each block, the compressed video signal having the least error;

encoding the selected signals to identify them as field formatted or frame formatted signals; and

combining the encoded signals.

31. A method in accordance with claim 30 comprising the further steps of:

predicting the pixel data for a current video frame contained in said digitized interlaced signal from pixel data of a previous frame;

subtracting said predicted pixel data from the actual pixel data for the current frame to provide an abbreviated set of pixel data for use in producing said first and second compressed video signals; and

encoding the selected signals with motion vector data generated during said prediction step.

32. A method for decoding the combined encoded signals produced by the method of claim 31, comprising the steps of:

decompressing field formatted signals in a decompression path adapted for field processing of data;

decompressing frame formatted signals in a decompression path adapted for frame processing of data;

retrieving the motion vector data from encoded selected signals representing a current video frame;

storing data representing a previous video frame;

computing prediction signals from the retrieved motion vector data and the stored data;

adding said prediction signals to the decompressed signals; and

combining the decompressed signals to recover the digitized interlaced video signal.

33. A method for decoding the combined encoded signals produced by the method of claim 30, comprising the steps of:

decompressing field formatted signals in a decompression path adapted for field processing of data;

decompressing frame formatted signals in a decompression path adapted for frame processing of data; and

combining the decompressed signals to recover the digitized interlaced video signal.

* * * * *

Exhibit 5

United States Patent [19]

Murakami et al.

[11] **Patent Number: 5,072,295**

[45] **Date of Patent: Dec. 10, 1991**

[54] **ADAPTIVE QUANTIZATION CODER/DECODER WITH LIMITER CIRCUITRY**

[75] Inventors: **Tokumichi Murakami; Yoshiaki Kato; Hideo Ohira,** all of Kanagawa, Japan

[73] Assignee: **Mitsubishi Denki Kabushiki Kaisha,** Tokyo, Japan

[21] Appl. No.: **569,927**

[22] Filed: **Aug. 20, 1990**

[30] **Foreign Application Priority Data**

Aug. 21, 1989 [JP] Japan 1-215233

[51] **Int. Cl.**[5] **H04N 7/13**

[52] **U.S. Cl.** **358/136;** 358/135

[58] **Field of Search** 358/136, 135; 375/27, 375/122

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,636,856	1/1987	Starck	358/135
4,743,967	5/1988	Takenaka et al.	358/136
4,891,698	1/1990	Mattausch et al.	358/136 X
4,893,184	1/1990	Mattausch et al.	358/136 X

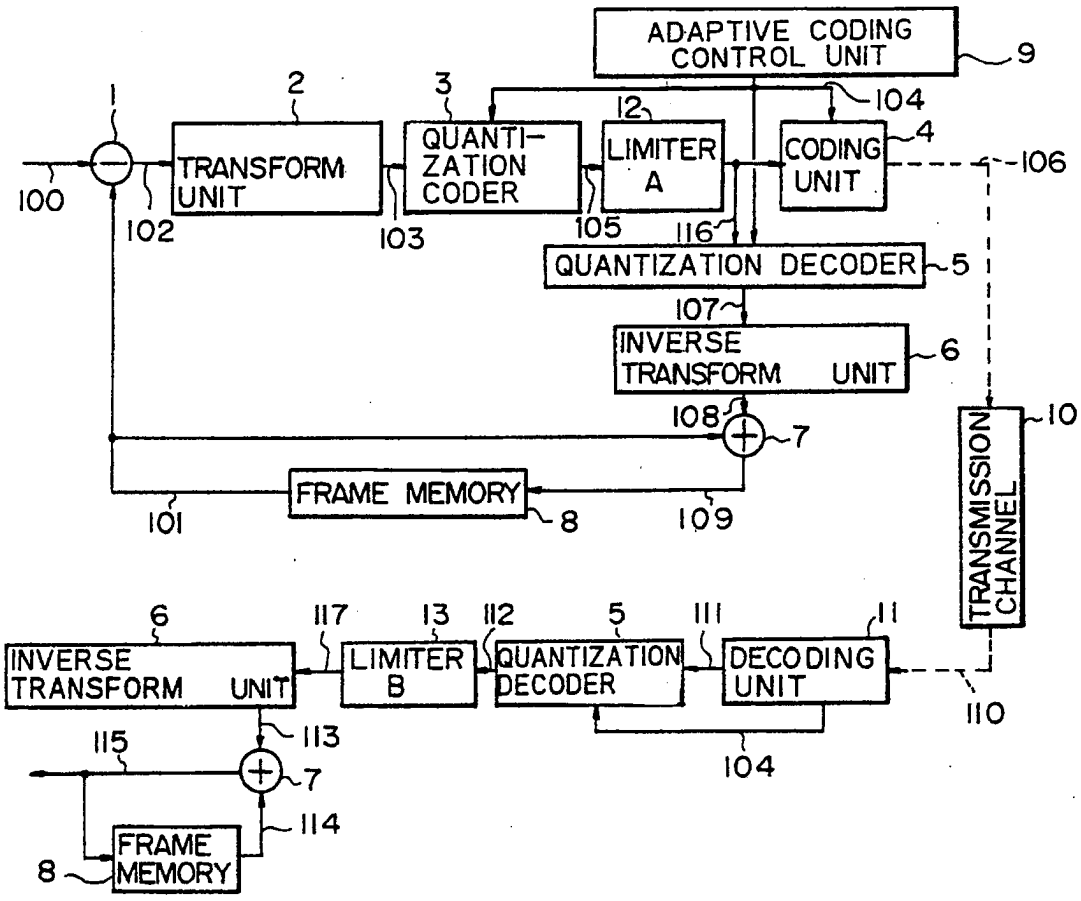
Primary Examiner—Victor R. Kostak

Attorney, Agent, or Firm—Wolf, Greenfield & Sacks

[57] **ABSTRACT**

An adaptive quantization coder/decoder having a limiter in a quantization coding module so that a reconstruction value of a quantization level is not in excess of a predetermined allowable range, or providing a limiter in a local quantization decoding module so that an output signal level falls within a predetermined allowable range, or providing a limiter in a quantization decoding module so that the output signal level falls within the predetermined allowable range.

6 Claims, 8 Drawing Sheets



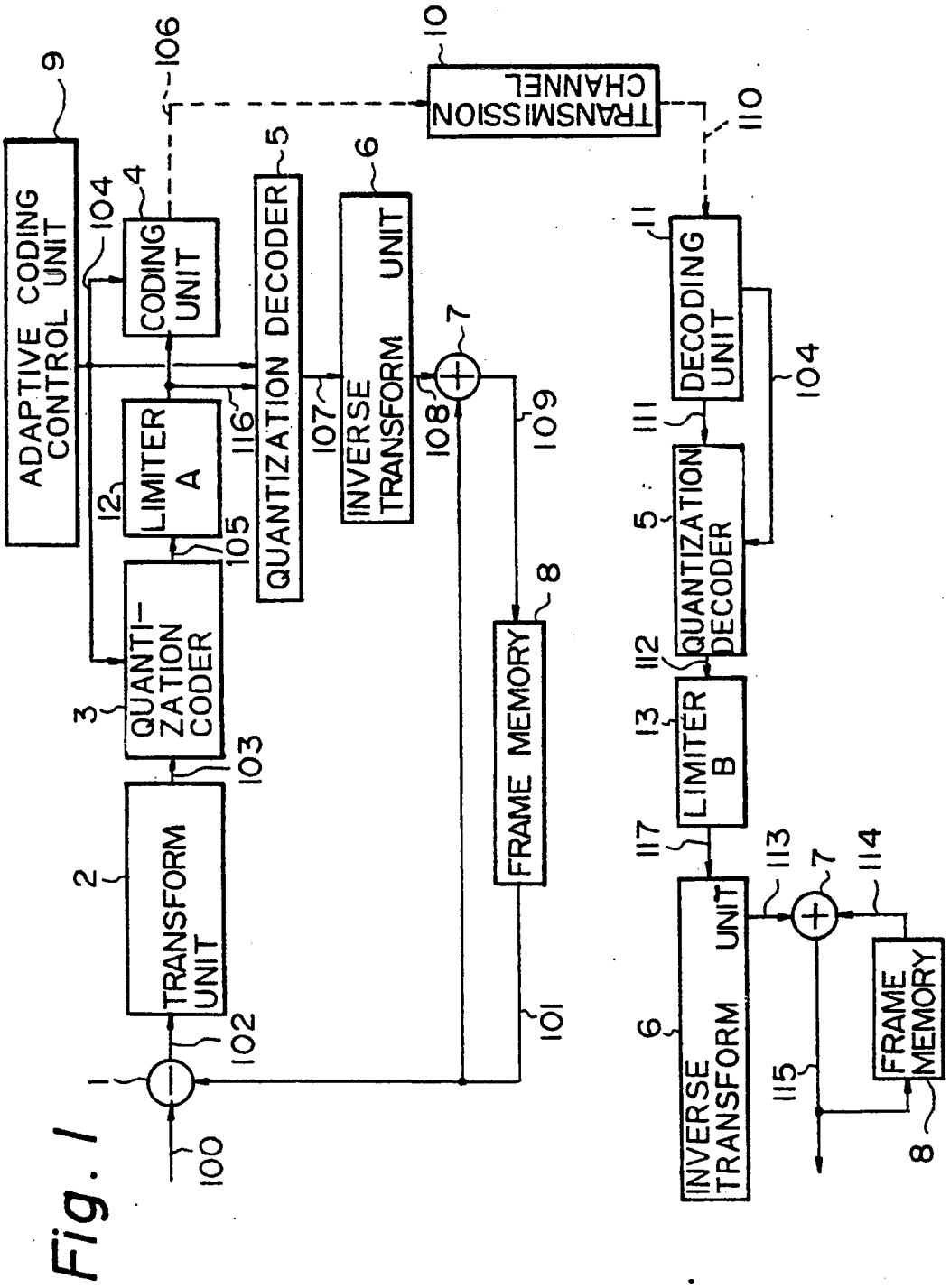
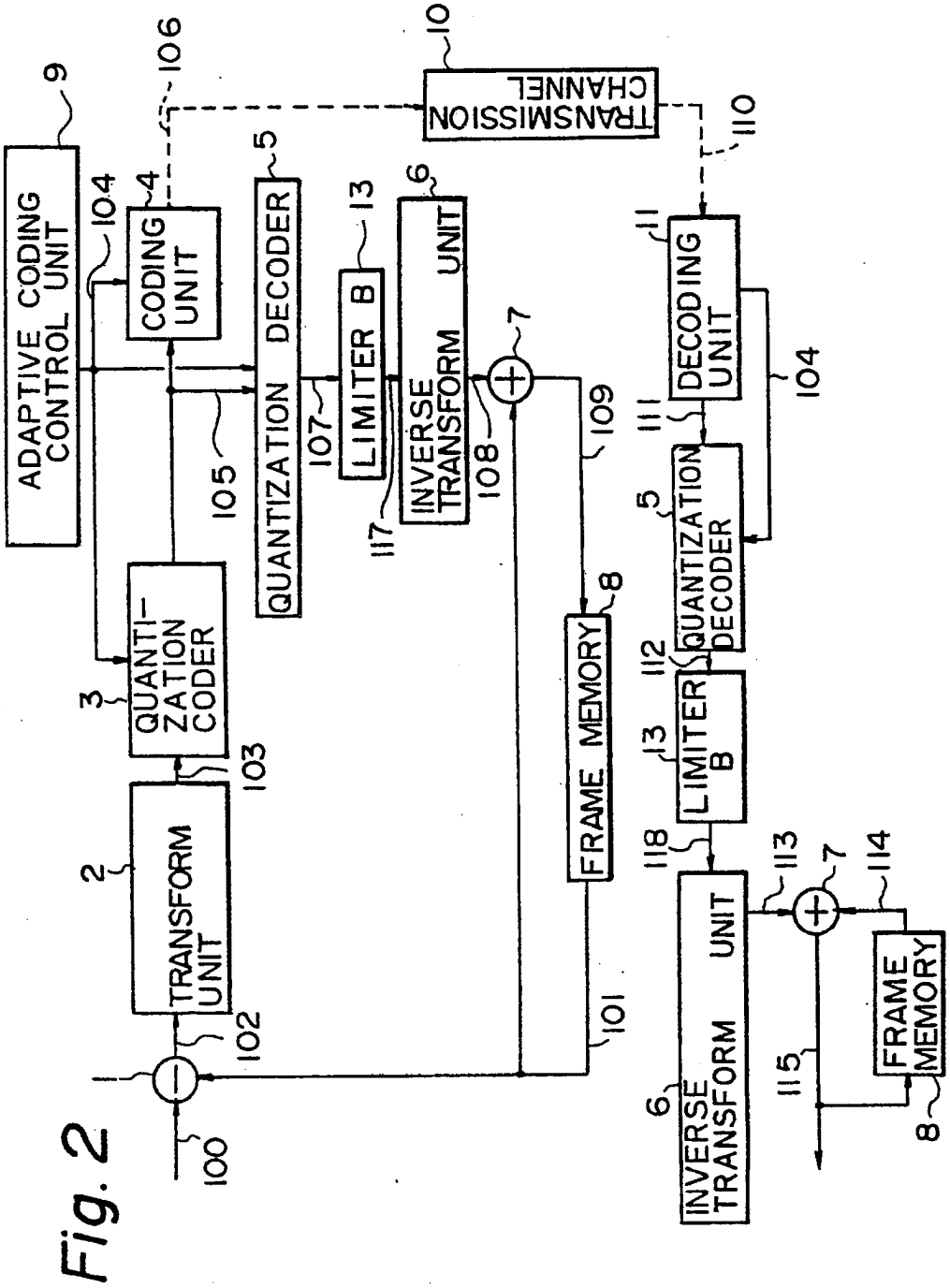

ADAPTIVE CODING CONTROL UNIT
9
CODING UNIT
4
LIMITER A
12
QUANTI-ZATION CODER
3
TRANSFORM UNIT
2
QUANTIZATION DECODER
5
INVERSE TRANSFORM UNIT
6
FRAME MEMORY
8
TRANSMISSION CHANNEL
10
DECODING UNIT
11
QUANTIZATION DECODER
5
LIMITER B
13
INVERSE TRANSFORM UNIT
6
FRAME MEMORY
8
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117

Fig. 1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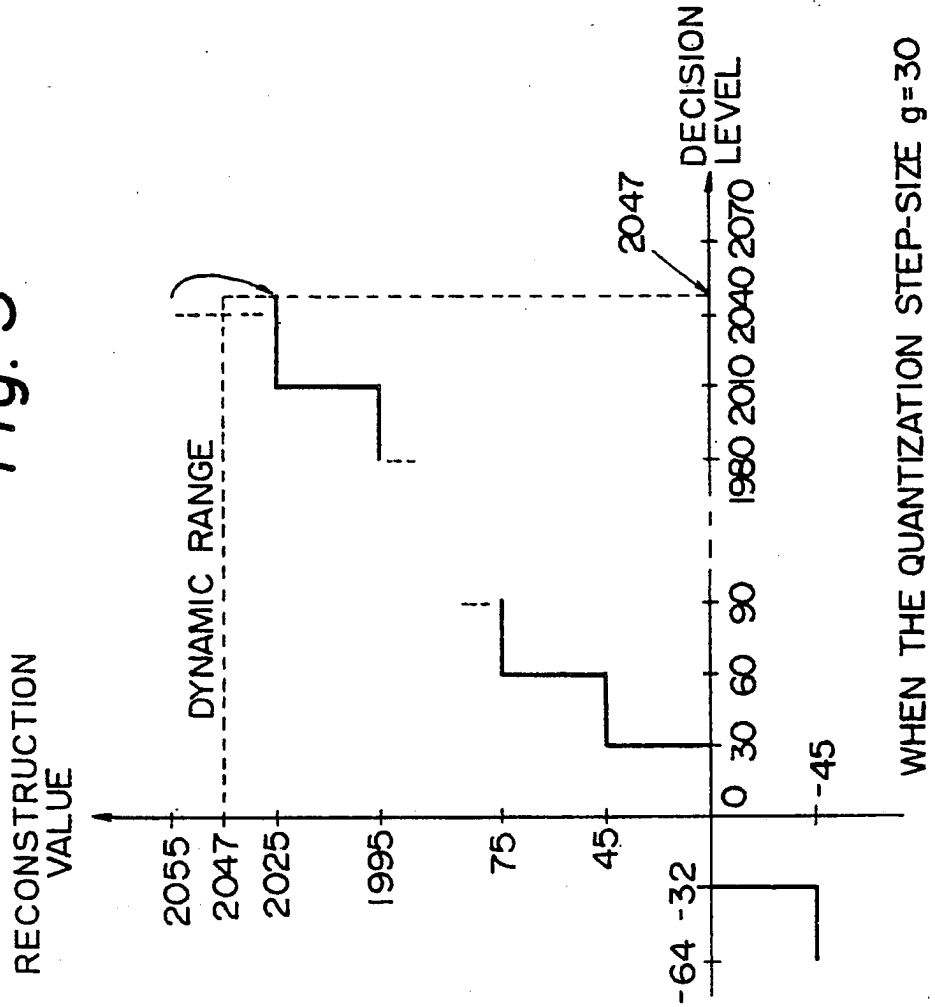
13
INVERSE TRANSFORM UNIT
6
DECODING UNIT
11
104
7
109
107
105
108
117
111
QUANTI-ZATION CODER
3
FRAME MEMORY
8
QUANTIZATION DECODER
5
112
LIMITER B
13
118
TRANSFORM UNIT
2
103
102
101
INVERSE TRANSFORM UNIT
6
113
7
114
FRAME MEMORY
8
115
100

Fig. 2

Fig. 3


RECONSTRUCTION VALUE
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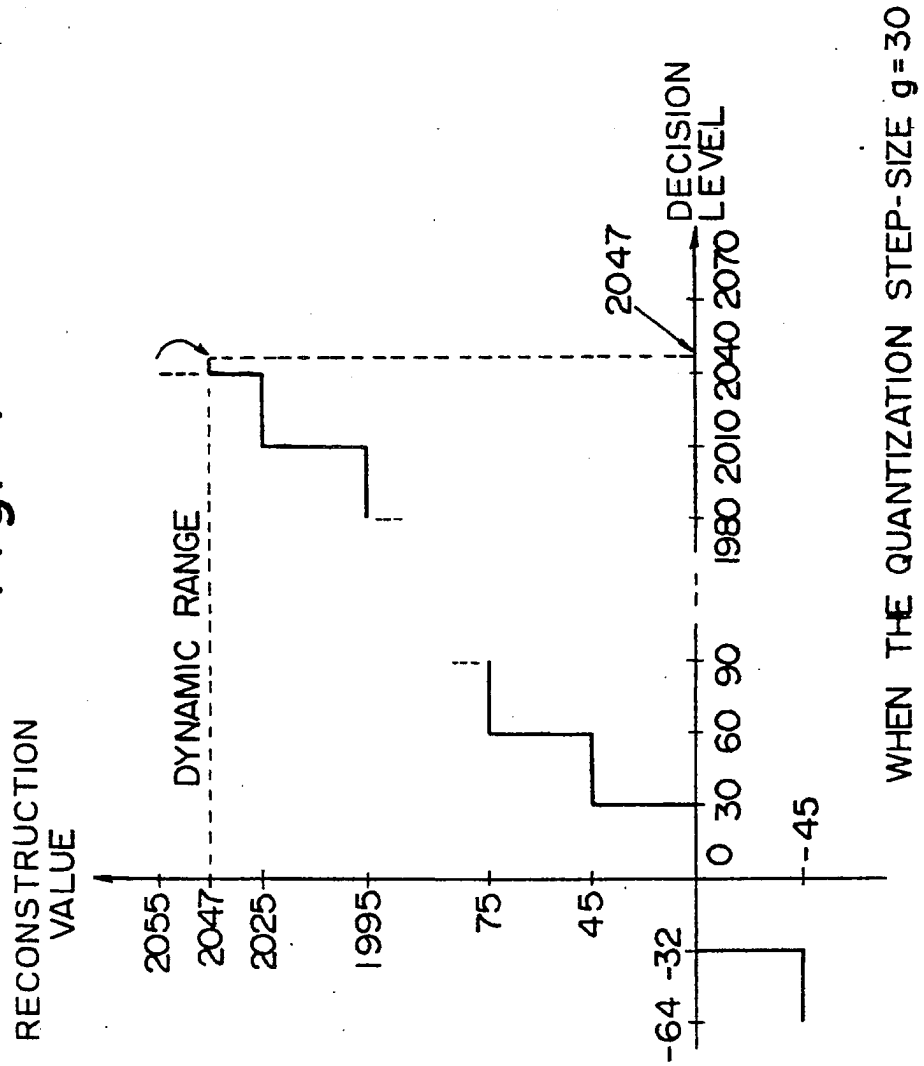
2055
2047
2025
1995
75
45
-64
-32
0
30
60
90
1980
2010
2040
2070
2047
DECISION LEVEL
-45
WHEN THE QUANTIZATION STEP-SIZE g=30

Fig. 4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DECISION LEVEL
-45
WHEN THE QUANTIZATION STEP-SIZE g=30

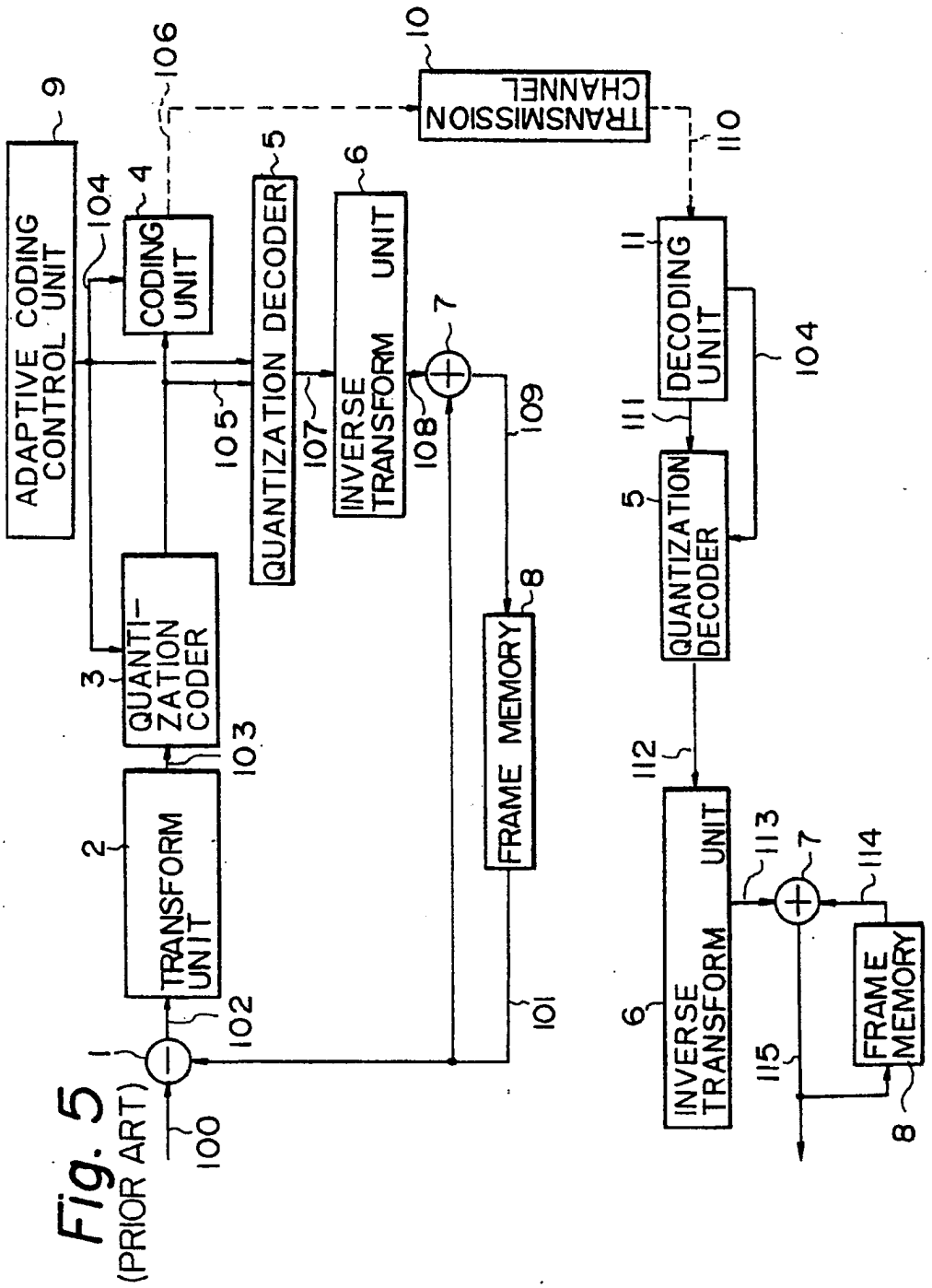


Fig. 5
(PRIOR ART)

Fig. 6

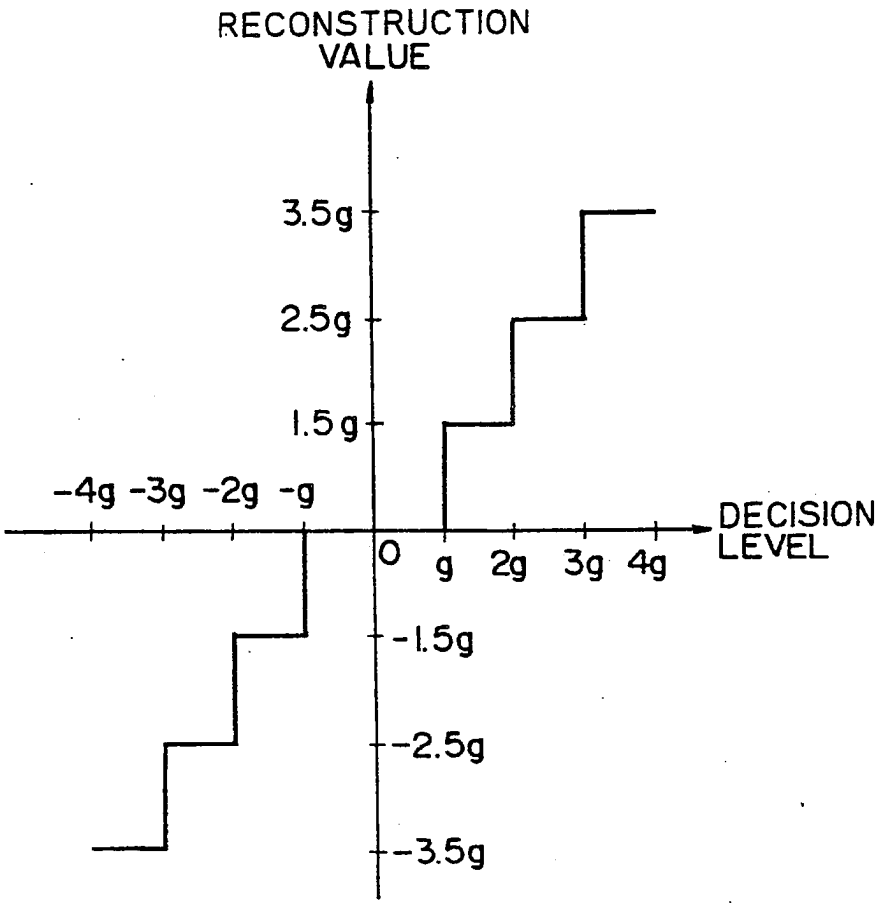
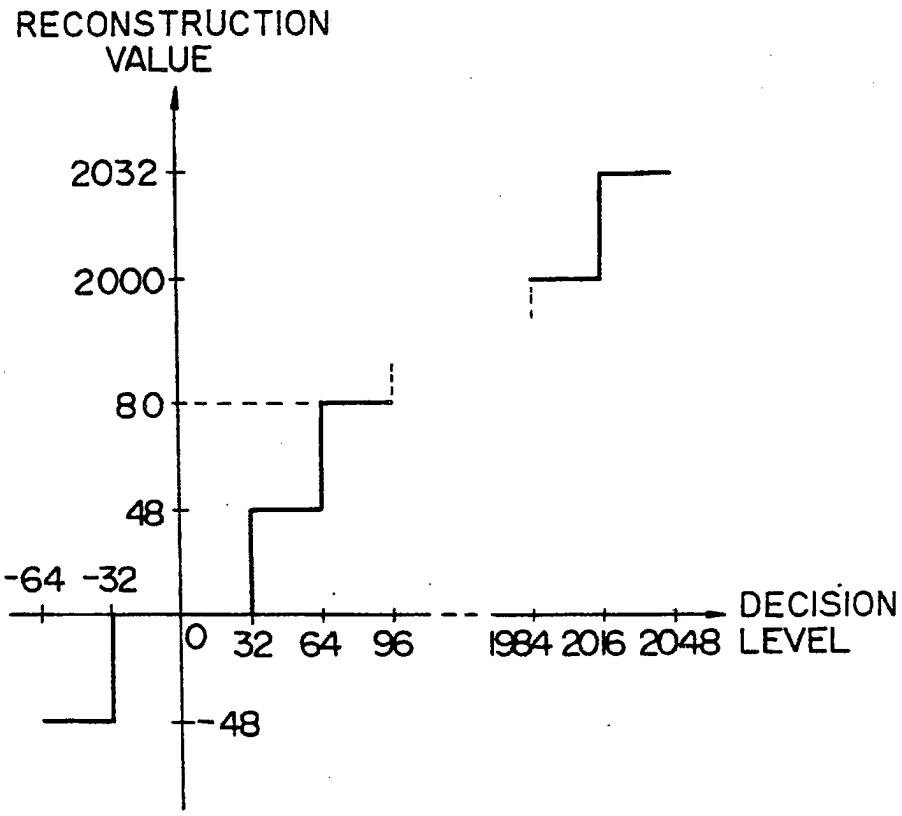
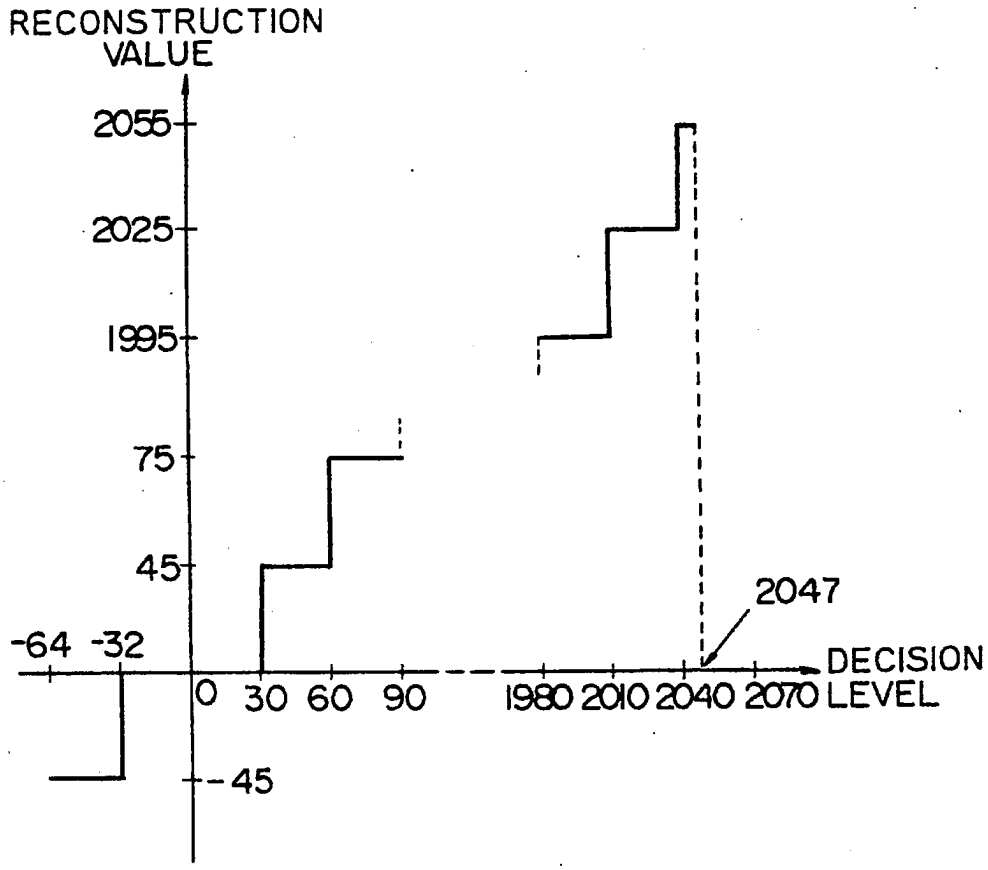

RECONSTRUCTION VALUE
3.5g
2.5g
1.5g
-4g -3g -2g -g
0 g 2g 3g 4g
DECISION LEVEL
-1.5g
-2.5g
-3.5g

Fig. 7



WHEN THE QUANTIZATION STEP-SIZE g = 32

Fig. 8



WHEN THE QUANTIZATION STEP-SIZE g=30

ADAPTIVE QUANTIZATION CODER/DECODER WITH LIMITER CIRCUITRY

BACKGROUND OF THE INVENTION

The present invention is directed to a quantizer for compressing an amount of information of digital signals and also to a coder/decoder employing this quantizer.

Referring to FIG. **5**, there is illustrated a prior art adaptive quantization coder/decoder reported in, e.g., [A Proposal of Coding Control Method for MC.DCT Coding Scheme] written by Kato et al (The National Convention of Information and Systems Group; The Institute of Electronic, Information and Communication Engineers, 1987). In FIG. **5**, the numeral **1** designates a subtracter; **2** a transform unit; **3** a quantization coder; **4** a coding unit; **5** a quantization decoder; **6** an inverse transform unit; **7** an adder; **8** a frame memory; **9** an adaptive coding control unit; **10** a transmission channel; and **11** a decoding unit.

Operations of the system depicted in FIG. **5** will next be described. On the transmitting side, a difference signal between a digitized input image signal **100** and a predictive signal **101** which is a previous frame signal of the frame memory **8** is obtained by the subtracter **1**. The thus obtained difference signal is defined as a predictive error signal **102**. The predictive error signal **102** is transformed into a transform coefficient **103** of a frequency domain in the transform unit **2** by a transform function such as, e.g., a discrete cosine transform. The transform coefficient **103** is quantized to a discrete level (hereinafter referred to as a quantization level) **105** by the quantization coder **3** in accordance with a quantization step-size **104** provided by the adaptive coding control unit **9**. A code is allocated to the quantization level **105** by means of the coding unit **4**, as a result of which coded data **106** is transmitted together with information of the quantization step-size **104** to the transmission channel **10**. The transform unit **2**, the quantization coder **3** and the coding unit **4** are combined to constitute a quantization coding module. A decode transform coefficient **107** is obtained from the quantization level **105** by the quantization decoder **5**, employing the quantization step-size **104**. The decode transform coefficient **107** undergoes an inverse transform in the inverse transform unit **6** to thereby, obtain a decode predictive error signal **108**. A local quantization decoding module is composed of the quantization decoder **5** and the inverse transform unit **6** on the transmitting side. The decode predictive error signals **108** is added to the predictive signal **101** by the adder **7**. The added value is held as a local decode signal **109** in the frame memory **8** to be used as a predictive signal **101** of the next frame.

On the other hand, coding data **110** transmitted via the transmission channel **10** is decoded to a quantization level **111** by the decoding unit **11** on the receiving side. A decode transform coefficient **112** is obtained from the quantization level **111** by means of the quantization decoder **5**, employing the quantization step-size **104** given from the decoding unit **11**. The decode transform coefficient **112** undergoes an inverse transform in the inverse transform unit **6**, thus acquiring a decode predictive error signal **113**. A quantization decoding module consists of the decoding unit **11**, the quantization decoder **5** and the inverse transform unit **6** on the receiving side. The decode predictive error signal **113** is added to a predictive signal **114** by the adder **7**. The thus added signal is outputted as a decode signal **115** and

at the same moment held in the frame memory **8** to be used as a predictive signal **114** of the next frame.

The quantization coder **3** for effecting the quantization as the quantization step-size **104** is adaptively controlled will hereinafter be described. Each dynamic range of the digitized input image signal **100** and the predictive signal **101** is from 0 to 255, i.e., 8 bits. In this case, the dynamic range of the predictive error signal **102** is from −255 to 255, viz., 9 bits (1 bit of which is a sign bit). The 9 bit predictive error signal **102** is arranged in (8×8) blocks and transformed into the transform coefficient **103** of the frequency domain of a 2 dimensional discrete cosine transform. In consequence of this, the dynamic range of the transform coefficient **103** ranges from −2048 to 2047, i.e., 12 bits (1 bit of which is a sign bit). Hence, the dynamic ranges of the input signal to the quantization coder **3** and of the output signal from the quantization decoder **5** are from −2048 to 2047. It is now assumed that a characteristic of the quantizer is defined, for simplicity, as a linear quantization characteristic of a mid-tread type wherein the quantization step-size shown in the following formula (**1**) is constant at all the decision levels.

$$q_{dec}(n)=(|n|\times g)\times n/|n|$$

$$q_{rep}(n)=\tfrac{1}{2}\{q_{dec}(n)+q_{dec}(n+n/|n|)\}$$

$$q_{rep}(O)=0 \qquad (1)$$

where $q_{dec}(n)$ is the decision level, $q_{rep}(n)$ is the reconstruction value, g is the quantization step-size, and n is the quantization index. Here, g is the positive even number. Turning to FIG. **6**, there is shown a quantization characteristic in this case. In FIG. **6**, the horizontal axis indicates the decision level of the quantizer, while the vertical axis indicates the reconstruction value. For example, when the transform coefficient CO is prescribed such as $3\,g \leqq CO < 4\,g$, CO is quantized to 3.5 g, and the quantization index, which undergoes a coding transmission, becomes 3. More specifically, as illustrated in FIG. **7**, when the quantization step-size g is set to 32, the transform coefficient CO, which is prescribed such as $64 \leqq CO < 96$, is quantized to a reconstruction value 80. A magnitude of the quantization step-size corresponds to the fineness of the quantization. The quantization becomes less fine with the increasing quantization step-size g. A difference (quantization error) between the input value and the reconstruction value increases, thereby causing a deterioration in the quality of the decoded image. The dynamic range of the input value is, as discussed above, fixed. Therefore, when the quantization step-size g is large, the dynamic range of the coded quantization index decreases to thereby reduce the amount of information to be transmitted. When the quantization step-size g is, e.g., 16, the dynamic range of the quantization index ranges from −128 to 127. In contrast, when the quantization step-size g is 64, the dynamic range of the quantization index is from −32 to 31. Hence, it is possible to optimize the relationship between the quality of the decoded image and the amount of information to be transmitted by adaptively controlling the quantization step-size g in accordance with the image inputted.

Supposing that the quantization step-size g is varied and set to 30, a quantization characteristic at that time is shown in FIG. **8**. Namely, the transform coefficient CO, which is prescribed such as $2040 \leqq CO \leqq 2047$, is quan-

tized to a reconstruction value 2055. In the case of being negative, the transform coefficient CO, which is prescribed such as $-2048 \leqq CO \leqq 2040$, is similarly quantized to a reconstruction value −2055.

There arises, however, the following problem inherent in the prior art adaptive quantization coder/decoder having the above-described construction. There exists a possibility that the reconstruction value outputted when changing the quantization step-size exceeds an allowable range of inputting at the next stage. For instance, a value-outputted from the quantization decoder in the quantization decoding module rises beyond the allowable range, resulting in a failure of operation.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention, which has been devised to obviate the foregoing problem, to provide an adaptive quantization coder/decoder wherein a reconstruction value to be outputted does not exceed an allowable input range of the next stage, and no operation failure occurs.

The adaptive quantization coder/decoder according to the present invention is characterized by providing a limiter in a quantization coding module so that a reconstruction value of a quantization level is not in excess of a predetermined allowable range, or providing a limiter in a local quantization decoding module so that an output signal level falls within a predetermined allowable range, or providing a limiter in a quantization decoding module so that the output signal level falls within the predetermined allowable range.

The adaptive quantization coder/decoder of the invention is arranged such that the reconstruction value of the quantization level does not exceed the predetermined allowable range by virtue of the limiter provided in the quantization coding module, or alternatively the output signal level falls within the predetermined allowable range by virtue of the limiter provided in the quantization.decoding module.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the present invention will become apparent during the following discussion taken in conjunction with the accompanying drawings, in which:

FIG. **1** is a block diagram showing a first embodiment of an adaptive quantization coder/decoder according to the present invention;

FIG. **2** is a block diagram showing a second embodiment of the adaptive quantization coder/decoder of the invention;

FIG. **3** is a chart illustrating a characteristic of a limiter A provided in a quantization coding module according to the present invention;

FIG. **4** is a chart illustrating a characteristic of a limiter B provided in a quantization decoding module or a local quantization decoding module according to the present invention;

FIG. **5** is a block diagram depicting a prior art adaptive quantization coder/decoder;

FIG. **6** is a chart of assistance in explaining a quantization characteristic; and

FIGS. **7** and **8** are explanatory charts each showing the quantization characteristic when quantization step-sizes are set to 32, and 30, respectively.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Illustrative embodiments of the present invention will hereinafter be described with reference to the accompanying drawings. In a first embodiment shown in FIG. **1**, the numeral **12** represents a limiter A provided in a quantization coding module. Designated at **13** is a limiter B provided in a quantization decoding module. Other components are the same as those depicted in FIG. **5**.

An operation of the limiter A of the quantization coding module will be explained referring to FIG. **1**. The operation starts by, as in the prior art, quantizing a transform coefficient **103** to a quantization level **105** in a quantization coder **3** by a quantization step-size **104**. Next, whether or not a reconstruction value exceeds an allowable dynamic range, herein from −2048 to 2047, of an input signal of the next stage is judged from the quantization step-size **104** and the quantization level **105** by means of the limiter A **12**. If greater than the dynamic range, there is outputted a quantization level **116** restricted closer by 1 level to the origin. To be specific, as illustrated in FIG. **3**, when the quantization step-size g is 30, a transform coefficient ranging from 2010 to 2047 is quantized to 2025. FIG. **3** shows a case where the transform coefficient is positive. In the case of being negative, the transform coefficient ranging from −2010 to −2048 is likewise quantized to −2025.

An operation of the limiter B provided in the quantization decoding module depicted also in FIG. **1** will be described with reference to FIG. **2**. Inputted to the limiter B **13** is a decode transform coefficient **112** conceived as an output signal from a quantization decoder **5** of the decoding module. If a value thereof exceeds the allowable dynamic range, the value is restricted to fall within a dynamic range of the transform coefficient. A transform coefficient **118** thus restricted is then outputted. In accordance with a second embodiment shown in FIG. **2**, instead of the limiter A of the quantization coding module depicted in FIG. **1**, a decode transform coefficient **107** of the quantization decoder **5** is restricted within the allowable dynamic range by the limiter B **13** in the local quantization decoding module. A transform coefficient **117** thus restricted is outputted. Namely, in the limiter B, as illustrated in FIG. **4**, when the quantization step-size g is 30, the transform coefficient ranging from 2040 to 2047 is outputted as a numeric value of 2047. FIG. **4** demonstrates a case where the transform coefficient is positive. In the case of being negative, the transform coefficient ranging from −2040 to −2048 is similarly outputted as −2048.

In accordance with the first and second embodiments, the limiters are provided respectively on the transmitting and receiving sides of the system. However, the effects are, as a matter of course, exhibited by providing the limiter on one side alone.

As discussed above, according to the present invention, the limiter A or B is provided in the quantization coding module or the local quantization decoding module; or the limiter B is provided in the quantization decoding module. With this arrangement, the reconstruction value of the discrete level due to the quantization decoding does not exceed the allowable range of the input signal of the next stage; or alternatively the output signal level falls within the allowable range. This in turn prevents any operation failure from occurring when effecting the quantization decoder.

Although the illustrative embodiments of the present invention have been described in detail with reference to the accompanying drawings, it is to be understood that the present invention is not limited to those embodiments. Various changes or modifications may be effected therein by one skilled in the art without departing from the scope or the spirit of the invention.

What is claimed is:

1. In a coder for compressively transforming each of digital input signals of a finite word length by quantizing said each input signal to a discrete level while adaptively varying a quantization step-size per said digital input signal,

an adaptive quantization coder comprising

an quantization coding module for coding said input signal by quantizing said input signal;

a local decoding module for generating a local decode signal from a quantized value of said input signal; and

a frame memory for storing said local decode signal,

characterized in that said quantization coding module includes:

means for generating an initial reconstruction value of a discrete level from said quantized value of said input signal;

detecting means for detecting when said initial reconstruction value exceeds a predetermined allowable range,

limiting means for generating a final reconstruction value, said final reconstruction value being equal to said initial reconstruction value when said initial reconstruction value falls within the predetermined allowable range, said final reconstruction value being limited to a discrete level closer by 1 level to an origin within said allowable range when said initial reconstruction value exceeds the predetermined allowable range.

2. The coder as set forth in claim 1, wherein said quantization coding module is composed of a transform unit for receiving and linearly transforming a difference signal between said input signal and said local decode signal, a quantizer for receiving and quantizing a signal from said transform unit, a limiter for restricting an output signal from said quantizer within a predetermined allowable range and a coding unit for receiving and coding a signal from said limiter.

3. In a coder for compressively transforming each of digital input signals of a finite word length by quantizing said each input signal to a discrete level while adaptively varying a quantization step-size per said digital input signal,

an adaptive quantization coder comprising:

a quantization coding module for coding said input signal by quantizing said input signal;

a local decoding module for generating a local decode signal from a quantized value of said input signal; and

a frame memory for storing said local decode signal, characterized in that said local decoding module is composed of a quantization decoder for receiving and reversely quantizing a discrete level generated after being quantized, a limiter for restricting an output signal from said quantization decoder within a predetermined allowable range and an inverse transform unit for receiving and inversely linearly transforming a signal from said limiter.

4. In a decoder for decoding a coded signal compressively transformed by quantizing each of input signals of a finite word length to a discrete level while adaptively varying a quantization step-size per said digital input signal,

an adaptive quantization decoder comprising:

a quantization decoding module for generating a decode signal after receiving a coded signal; and

a frame memory for storing said decode signal,

characterized in that said quantization decoding module is composed of a decoding unit for receiving and decoding said coded signal, a quantization decoder for receiving and reversely quantizing a decode signal from said decoding unit, a limiter for restricting said output signal from said quantization decoder within a predetermined allowable range and an inverse transform unit for receiving and inversely transforming a signal from said limiter.

5. In an adaptive quantization coding/decoding system consisting of a coder for compressively transforming each of digital input signals of a finite word length by quantizing said each input signal to a discrete level while adaptively varying a quantization step-size per said digital input signal and a decoder for decoding a coded signal,

the improvement characterized by said coder including:

a quantization coding module for coding said input signal by quantizing said input signal;

a local decoding module for generating a local decode signal from a quantized value of said input signal; and

a frame memory for storing said local decode signal,

said quantization coding module having means for generating an initial reconstruction value of a discrete level from said quantized value of said input signal;

detecting means for detecting when said initial reconstruction value exceeds a predetermined allowable range,

limiting means for generating a final reconstruction value, said final reconstruction value being equal to said initial reconstruction value when said initial reconstruction value falls within the predetermined allowable range, said final reconstruction value being limited to a discrete level closer by 1 level to an origin within said allowable range when said initial reconstruction value exceeds the predetermined allowable range,

said decoder including:

a quantization decoding module for generating a decode signal after receiving said coded signal; and

a frame memory, for storing said decode signal.

6. In an adaptive quantization coding/decoding system consisting of a coder for compressively transforming each of digital input signals of a finite word length by quantizing said each input signal to a discrete level while adaptively varying a quantization step-size per said digital input signal and a decoder for decoding a coded signal,

the improvement characterized by said coder including:

a quantization coding module for coding said input signal by quantizing said input signal;

a local decoding module for generating a local decode signal from a quantized value of said input signal; and

a frame memory for storing said local decode signal, said local decoding unit being composed of a quantization decoder for receiving and reversely quan-

tizing a discrete level generated after being quantized, a limiter for restricting an output signal from said quantization decoder within a predetermined allowable range and an inverse transform unit for receiving and inversely linearly transforming a signal from said limiter,

said decoder including:

a quantization decoding module for generating a decode signal after receiving said coded signal; and

a frame memory for storing said decode signal,

said quantization decoding module is composed of a decoding unit for receiving and decoding said coded signal, a quantization decoder for receiving and reversely quantizing a decode signal from said decoding unit, a limiter for restricting said output signal from said quantization decoder within a predetermined allowable range and an inverse transform unit for receiving and inversely transforming a signal from said limiter.

* * * * *

Exhibit 6

US005990960A

United States Patent [19]

Murakami et al.

[11] Patent Number: 5,990,960

[45] Date of Patent: Nov. 23, 1999

[54] **IMAGE SIGNAL CODING SYSTEM**

[75] Inventors: **Tokumichi Murakami; Kohtaro Asai; Hirofumi Nishikawa; Yoshihisa Yamada,** all of Kanagawa-ken, Japan

[73] Assignee: **Mitsubishi Denki Kabushiki Kaisha,** Tokyo, Japan

[21] Appl. No.: **09/207,919**

[22] Filed: **Dec. 9, 1998**

Related U.S. Application Data

[62] Division of application No. 08/803,235, Feb. 20, 1997, Pat. No. 5,867,220, which is a continuation of application No. 08/121,293, Sep. 13, 1993, Pat. No. 5,638,127, which is a division of application No. 07/962,299, Oct. 16, 1992, Pat. No. 5,274,442.

[30] **Foreign Application Priority Data**

Oct. 22, 1991 [JP] Japan 3-273843
Feb. 4, 1992 [JP] Japan 4-80654

[51] **Int. Cl.**[6] **H04N 7/32**

[52] **U.S. Cl.** **348/409**; 348/415

[58] **Field of Search** 348/384, 390, 348/400, 401, 402, 403, 404, 405, 409, 415, 416, 420; 382/232, 233, 236, 238

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,437,119	3/1984	Matsumoto et al.	348/412
4,546,386	10/1985	Matsumoto et al.	348/412
4,571,618	2/1986	Hatori et al.	348/412
4,675,733	6/1987	Tanimoto	348/399
4,691,329	9/1987	Juri et al.	348/420
4,703,351	10/1987	Kondo	348/415
4,772,947	9/1988	Kono	348/420
4,783,698	11/1988	Harney	348/390
4,849,812	7/1989	Borgers	348/400
4,931,869	6/1990	Amor et al.	348/403
5,045,938	9/1991	Sugiyama	348/408
5,046,119	9/1991	Hoffert et al.	348/391
5,068,724	11/1991	Krause et al.	348/402
5,083,720	1/1992	Krause	348/413
5,091,782	2/1992	Krause et al.	348/400
5,157,747	10/1992	Nuhara	348/416
5,193,004	3/1993	Wang et al.	348/420
5,274,442	12/1993	Murakami et al.	348/405
5,347,309	9/1994	Takahashi	348/420
5,416,523	5/1995	Murakami et al.	348/420
5,428,693	6/1995	Murakami	348/415
5,583,657	12/1996	Jeong	348/408
5,638,127	6/1997	Murakami et al.	348/419
5,767,909	6/1998	Jung	348/403
5,838,825	11/1998	Obayashi	382/233

FOREIGN PATENT DOCUMENTS

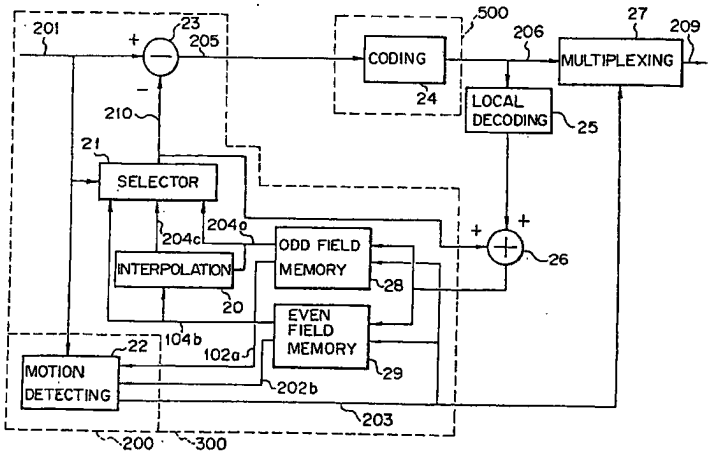
385654	2/1989	European Pat. Off. .
484140	5/1992	European Pat. Off. .
490799	6/1992	European Pat. Off. .
499307	8/1992	European Pat. Off. .
510972	10/1992	European Pat. Off. .
62-102685	5/1987	Japan .
63-224491	9/1988	Japan .
1278184	11/1989	Japan .
220082	8/1990	Japan .
3001688	1/1991	Japan .
3097320	4/1991	Japan .
4-167882	6/1992	Japan .
4178088	6/1992	Japan .
4-252690	9/1992	Japan .
4-288790	10/1992	Japan .
5022718	1/1993	Japan .
WO 9210060	6/1992	WIPO .

Primary Examiner—Bryan Tung

[57] **ABSTRACT**

An adaptive blocking coding system selects an effective blocking of an input image signal to be encoded in accordance with the correlation between fields, even if motion is detected between the fields. The blocking patterns include an individual field blocking, a non-interlace blocking, a split blocking and an inverted split blocking. Further, the coding system searches for motion from both odd and even fields of a frame for producing a motion, compensated prediction signal in order to provide high-efficient coding.

10 Claims, 21 Drawing Sheets



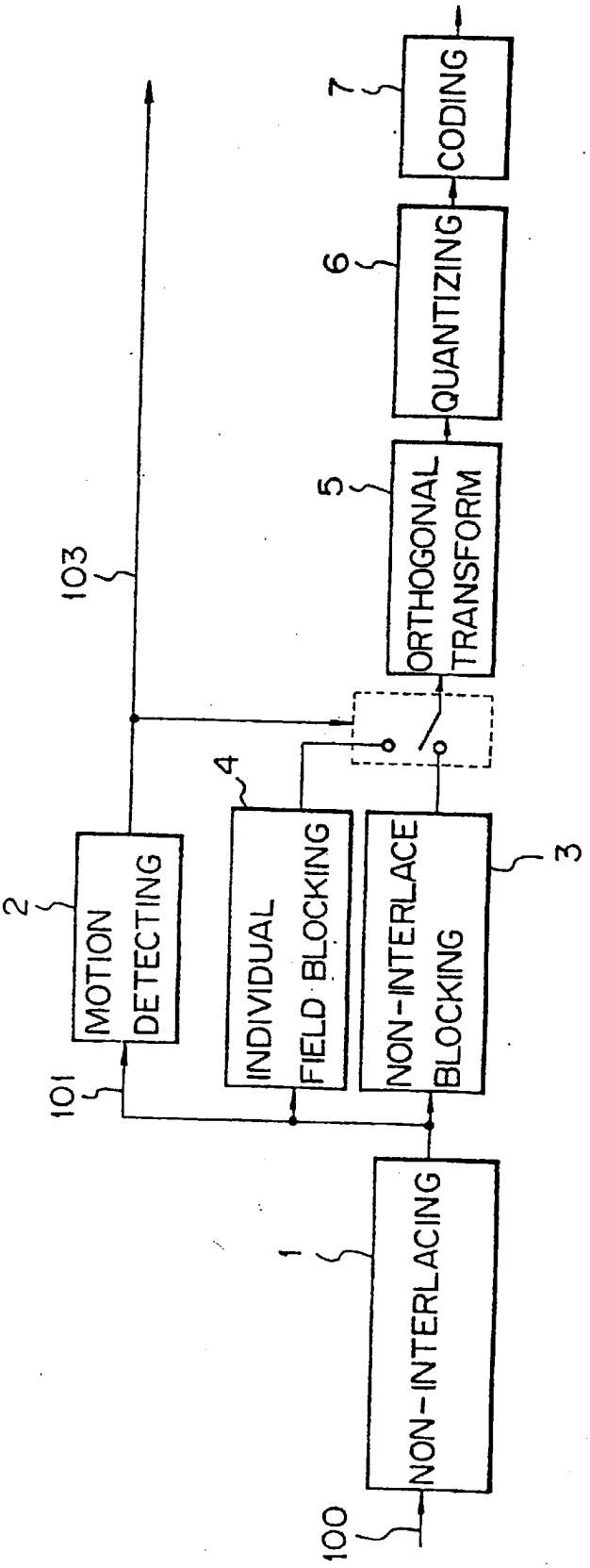
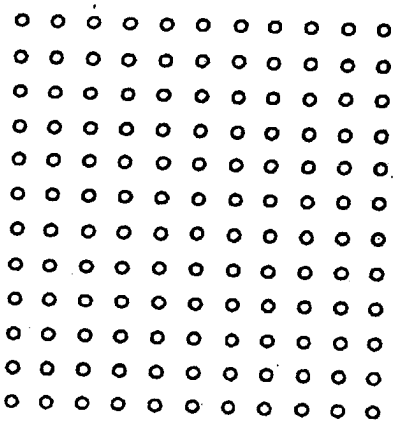
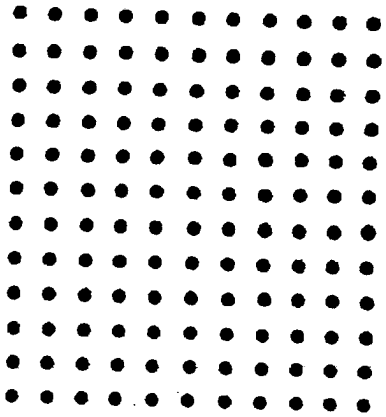


Fig. 1 (PRIOR ART)



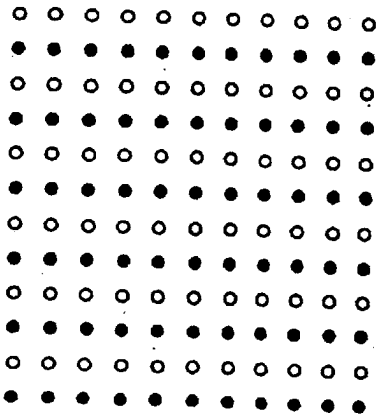
ODD FIELD

Fig. 2(A)
PRIOR ART



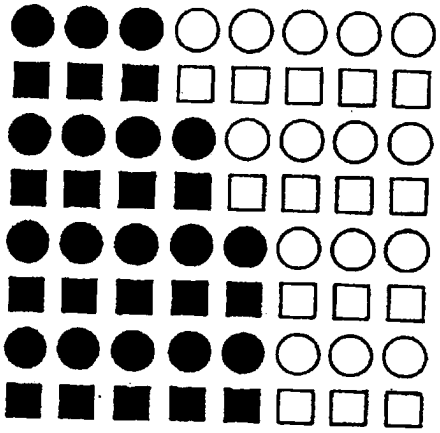
EVEN FIELD

Fig. 2(B)
PRIOR ART



NON-INTERLACED FRAME

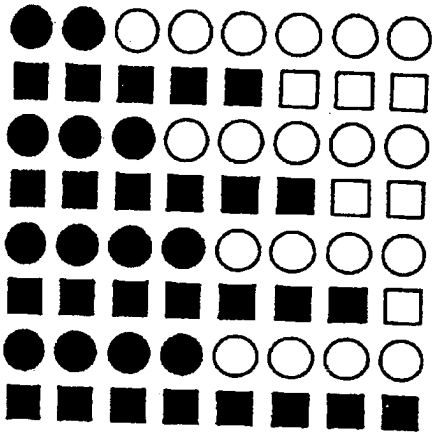
Fig. 2(C)
PRIOR ART



NON-INTERLACE IS SUITABLE

Fig. 3(A)

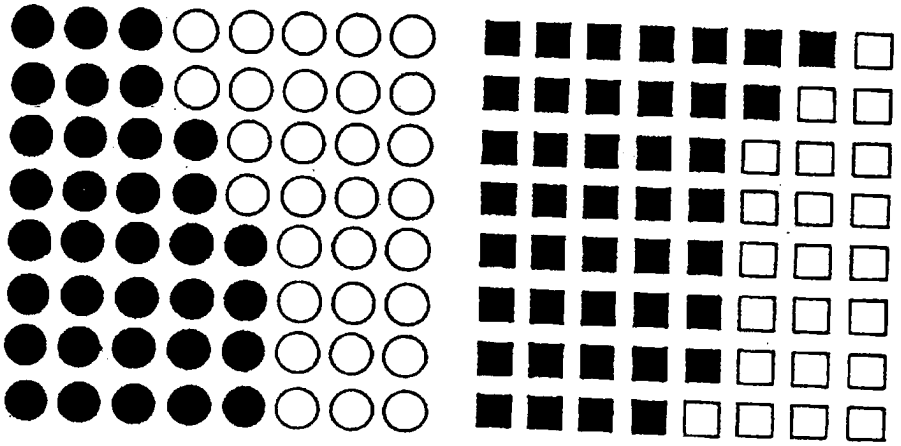
PRIOR ART



NON-INTERLACE IS NOT SUITABLE

Fig. 3(B)

PRIOR ART



INDIVIDUAL FIELD BLOCKING IS SUITABLE

Fig. 3(C)

PRIOR ART

○: ODD FIELD □: EVEN FIELD

(THIS DENOTATION IS USED ONLY HERE.)

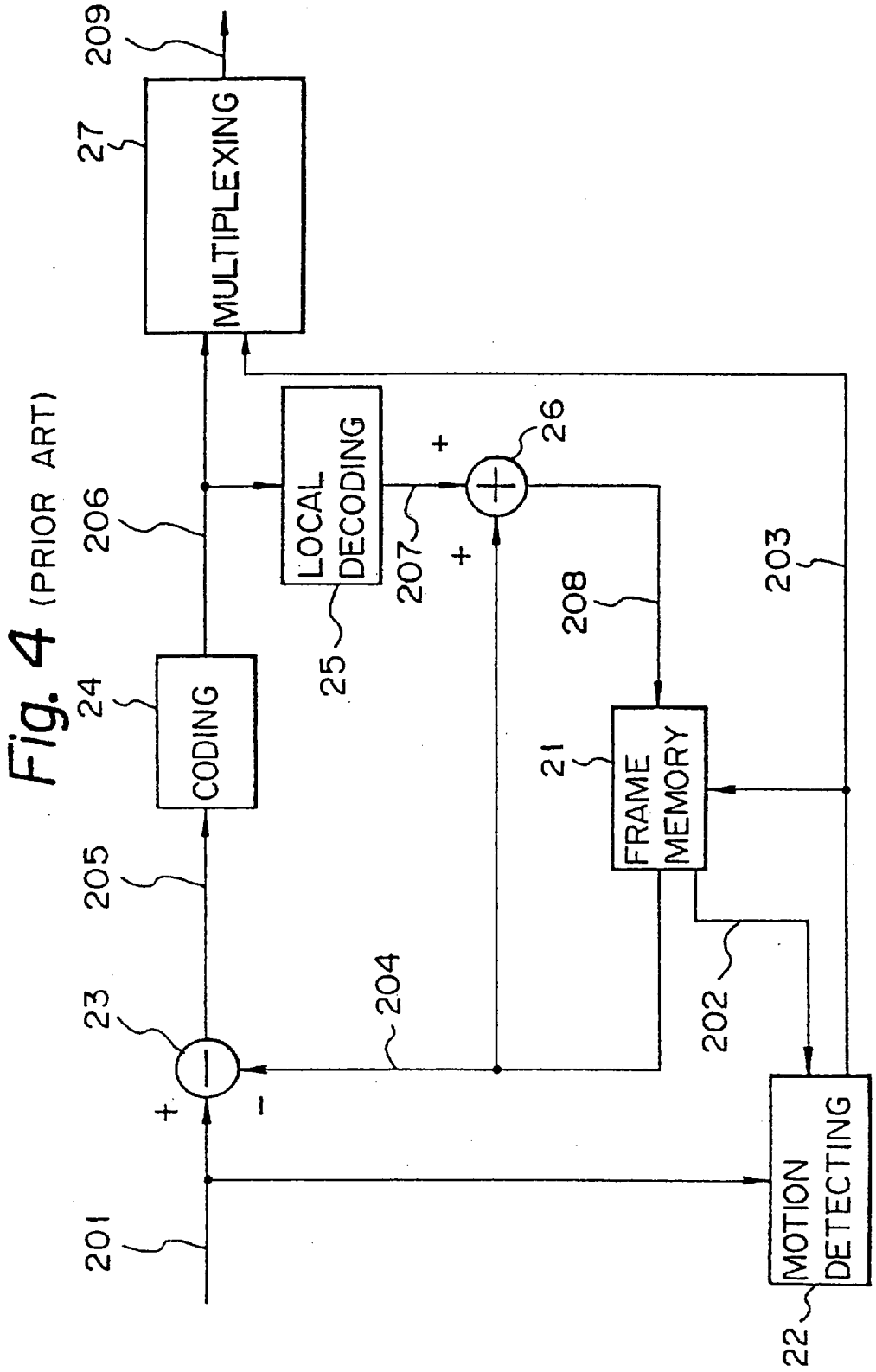
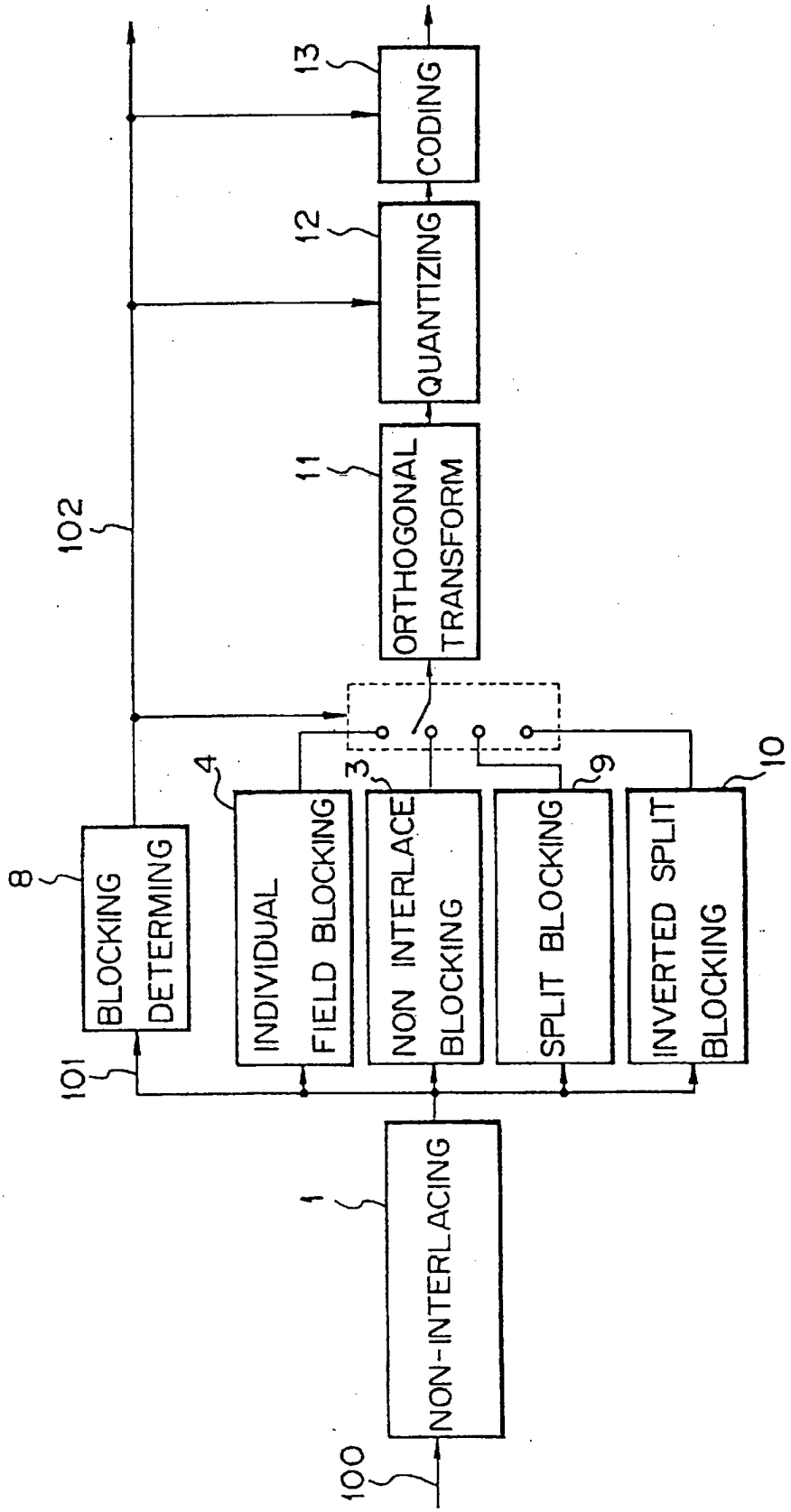


Fig. 4 (PRIOR ART)

Fig. 5


NON-INTERLACING
1
100
101
BLOCKING DETERMING
8
INDIVIDUAL FIELD BLOCKING
4
NON INTERLACE BLOCKING
3
SPLIT BLOCKING
9
INVERTED SPLIT BLOCKING
10
102
ORTHOGONAL TRANSFORM
11
QUANTIZING
12
CODING
13

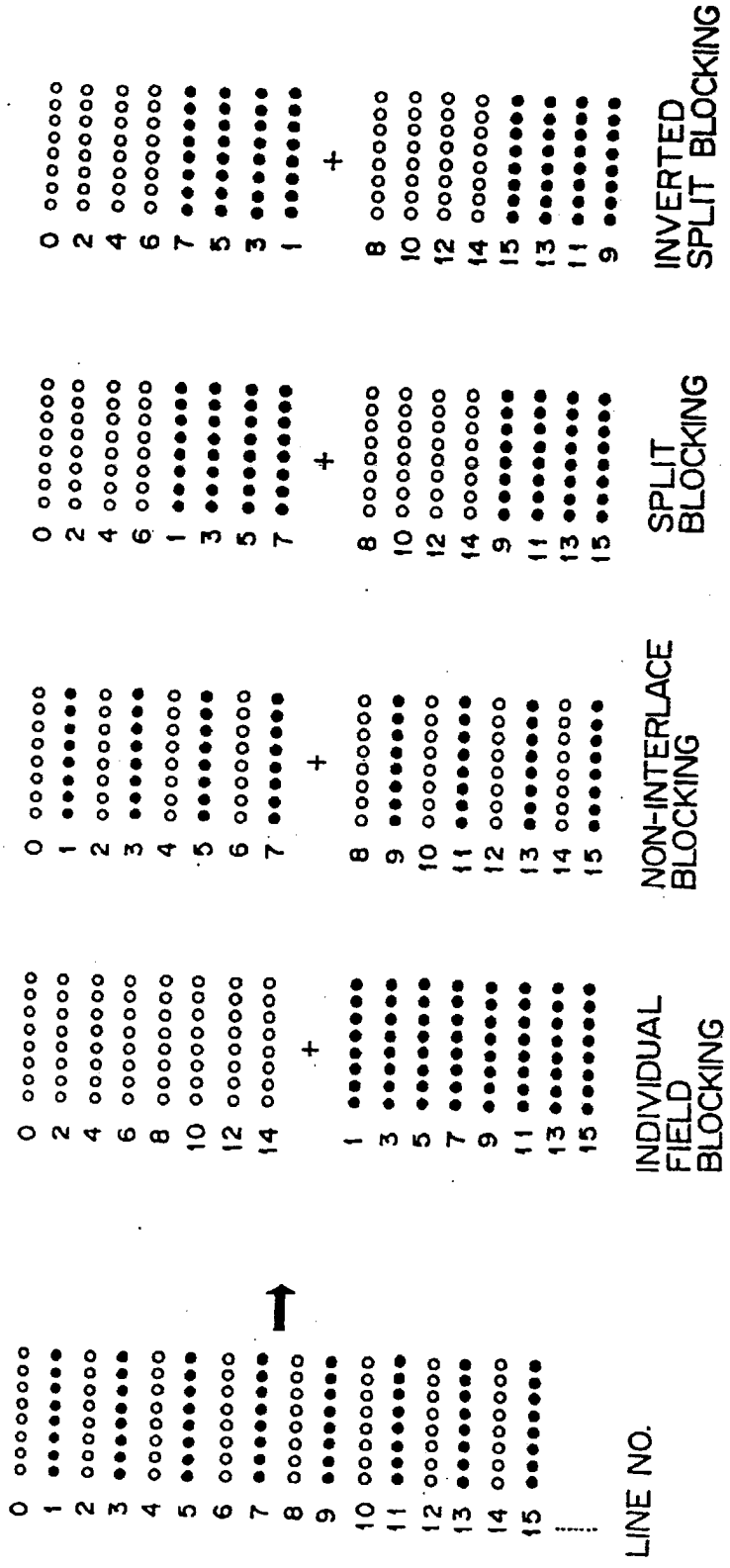


Fig. 6 Fig. 6(A) Fig. 6(B) Fig. 6(C) Fig. 6(D)

Fig. 7

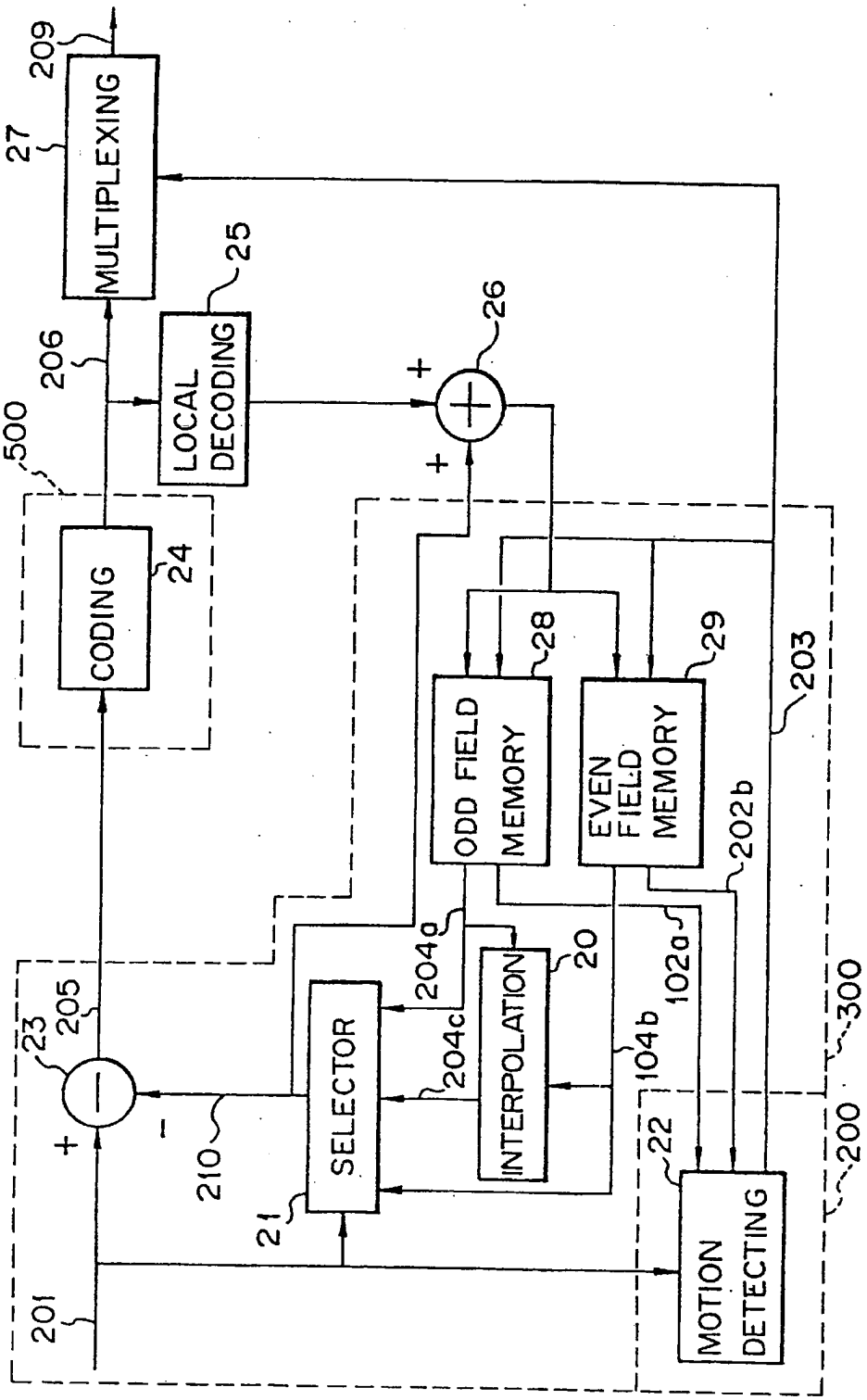

209
27
MULTIPLEXING
25
LOCAL DECODING
26
206
500
CODING
24
28
ODD FIELD MEMORY
29
EVEN FIELD MEMORY
203
202b
204a
20
102a
23
205
204c
SELECTOR
INTERPOLATION
104b
300
210
22
200
21
MOTION DETECTING
201

Fig. 8

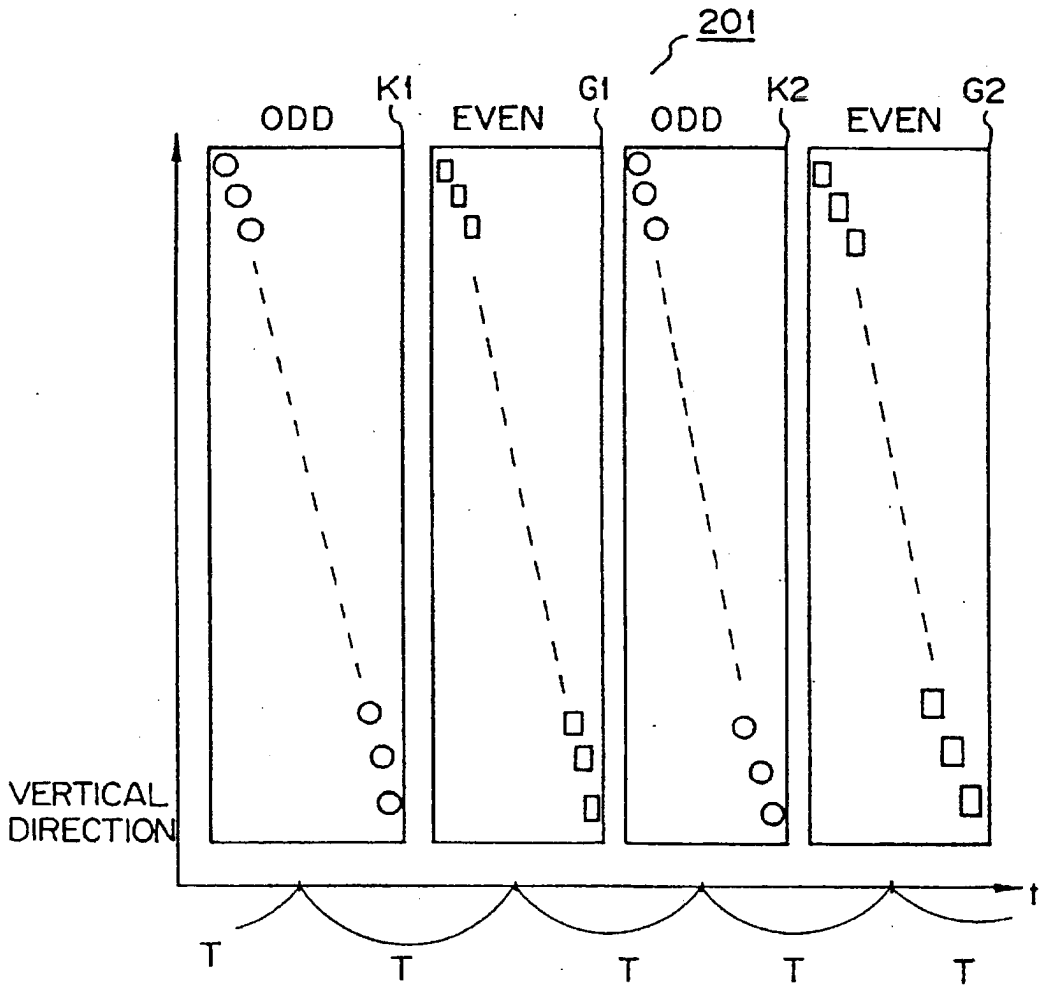
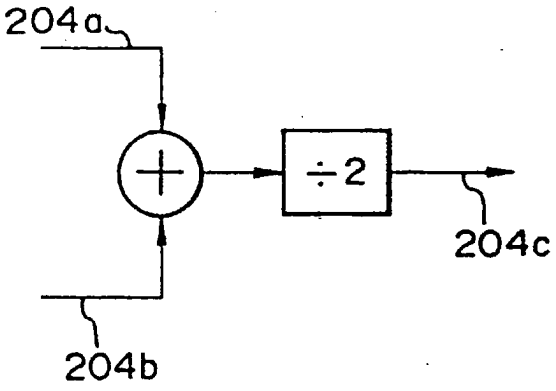


Fig. 9



INTERPOLATION SECTION

Fig. 10(A)

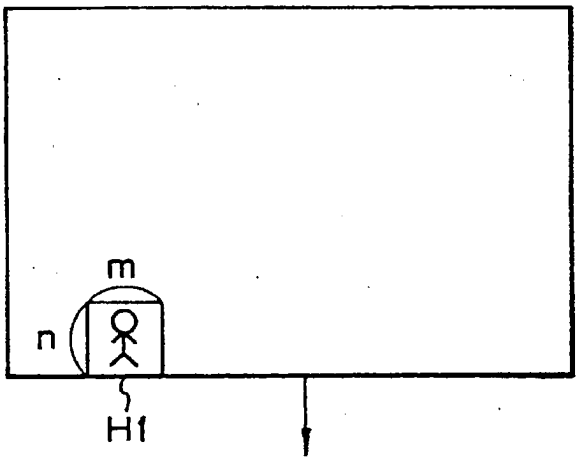


Fig. 10(B)

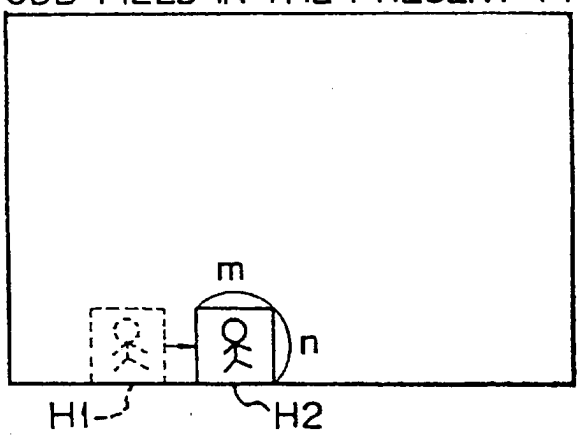


Fig. 11

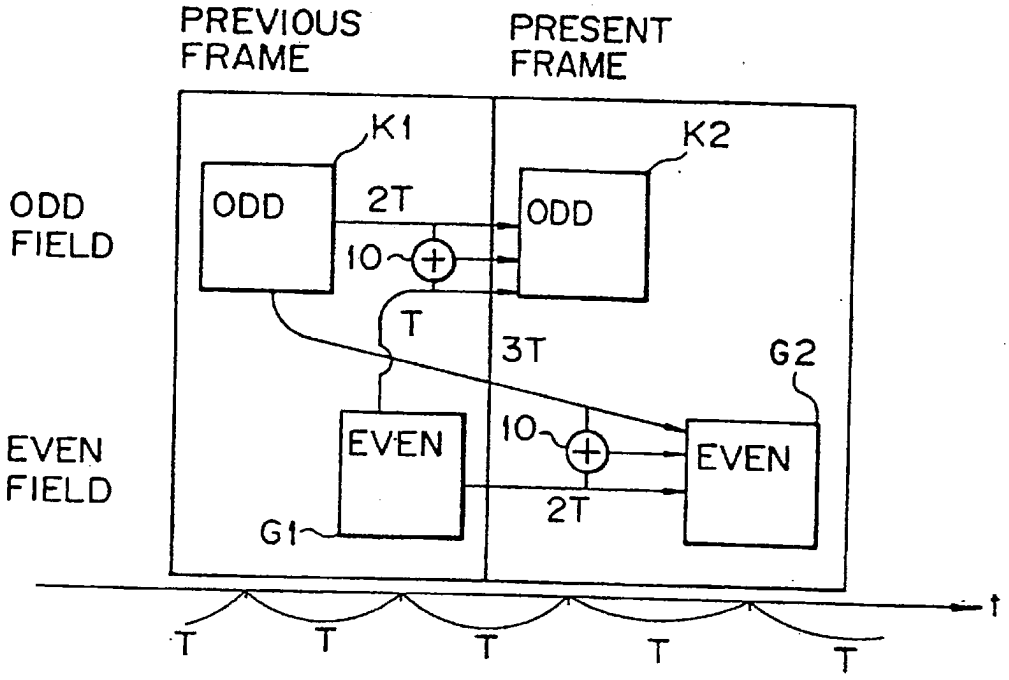

PREVIOUS FRAME
PRESENT FRAME
ODD FIELD
EVEN FIELD
K1
K2
ODD
ODD
2T
10
T
3T
G2
EVEN
EVEN
10
2T
G1
t
T
T
T
T
T

Fig. 12

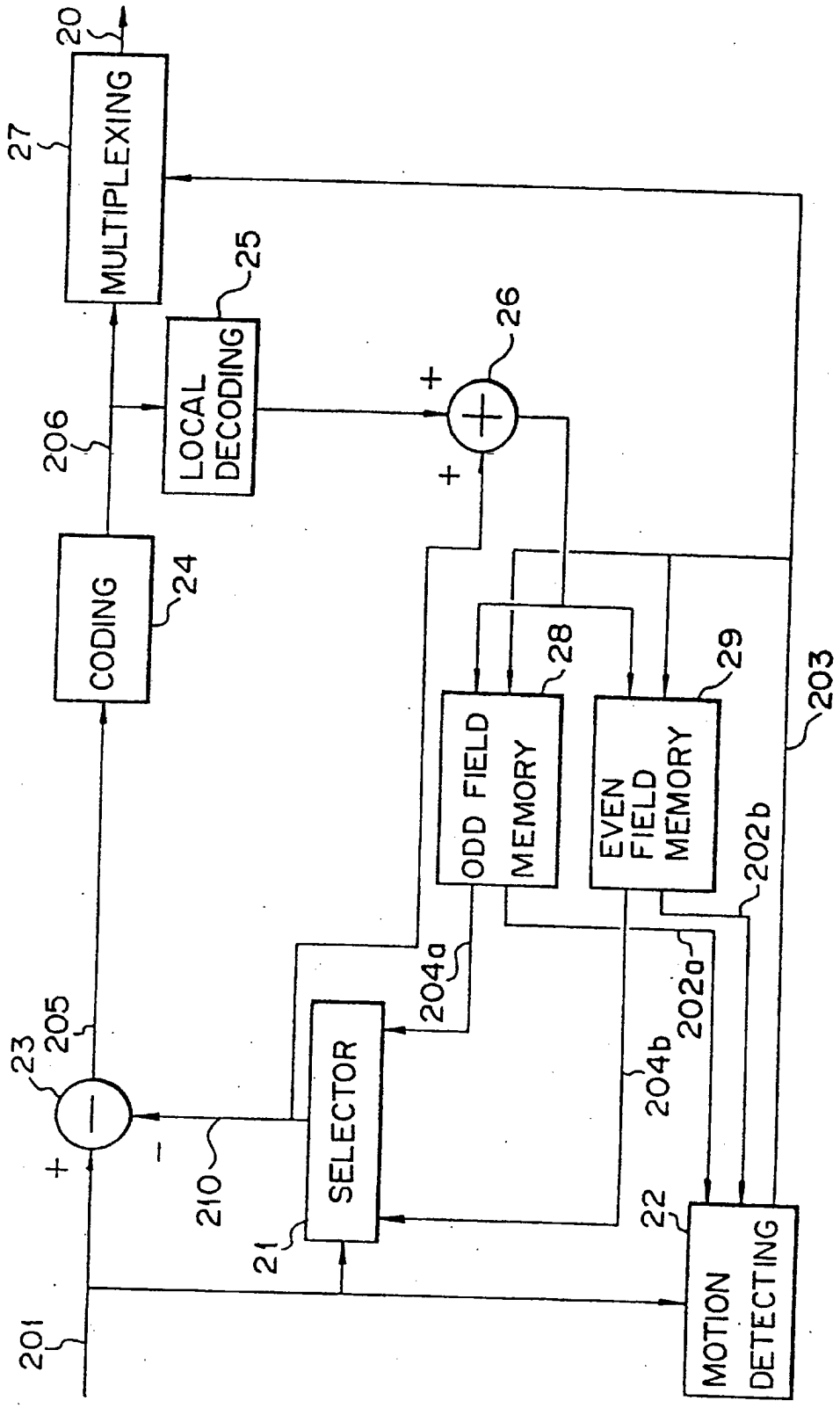
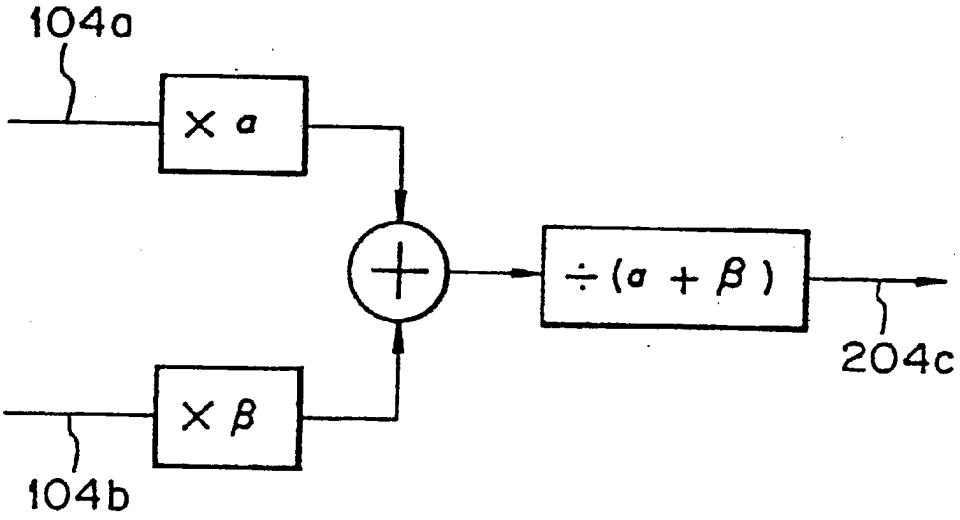

20
MULTIPLEXING
27
25
LOCAL DECODING
26
206
+
+
CODING
24
28
ODD FIELD MEMORY
29
EVEN FIELD MEMORY
203
202b
204a
202a
204b
205
23
+
−
210
SELECTOR
21
22
MOTION DETECTING
201

Fig. 13



INTERPOLATION SECTION

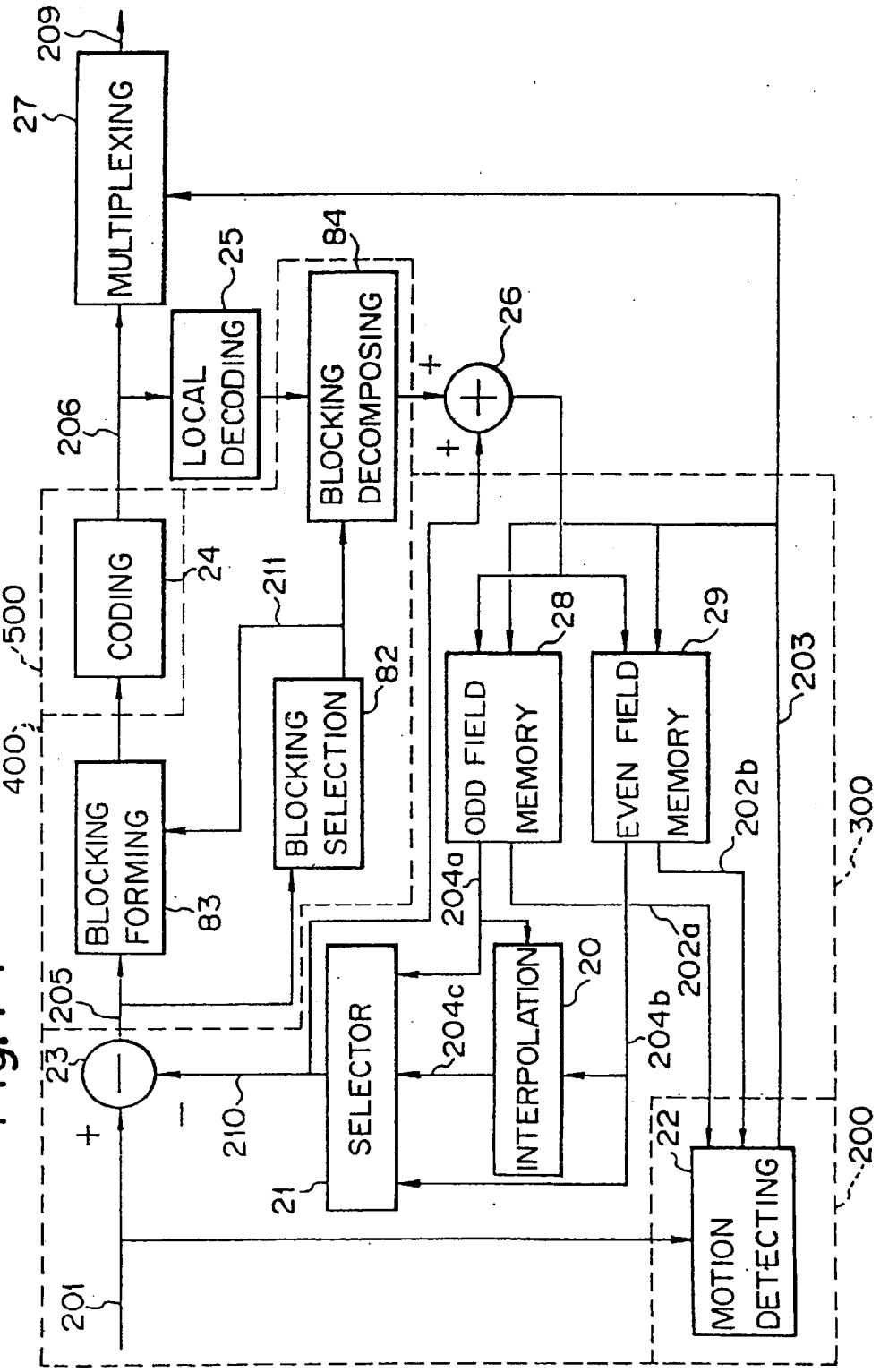

209
27
MULTIPLEXING
25
LOCAL DECODING
84
BLOCKING DECOMPOSING
26
206
CODING
24
211
500
400
BLOCKING SELECTION
82
ODD FIELD MEMORY
28
EVEN FIELD MEMORY
29
203
202b
300
BLOCKING FORMING
83
204a
205
23
210
SELECTOR
204c
INTERPOLATION
20
204b
202a
21
22
MOTION DETECTING
200
201

Fig. 14

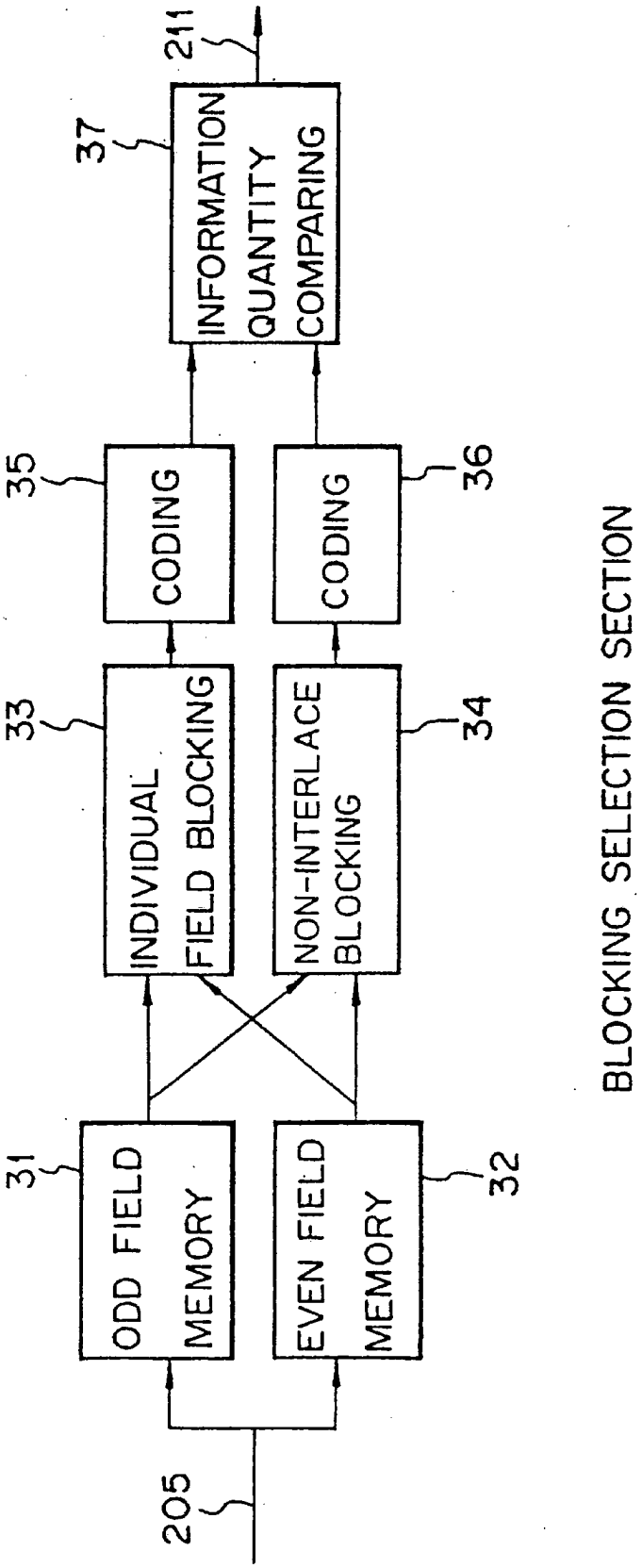

211
37
INFORMATION QUANTITY COMPARING
35
CODING
36
CODING
33
INDIVIDUAL FIELD BLOCKING
34
NON-INTERLACE BLOCKING
31
ODD FIELD MEMORY
32
EVEN FIELD MEMORY
205
BLOCKING SELECTION SECTION

Fig. 15

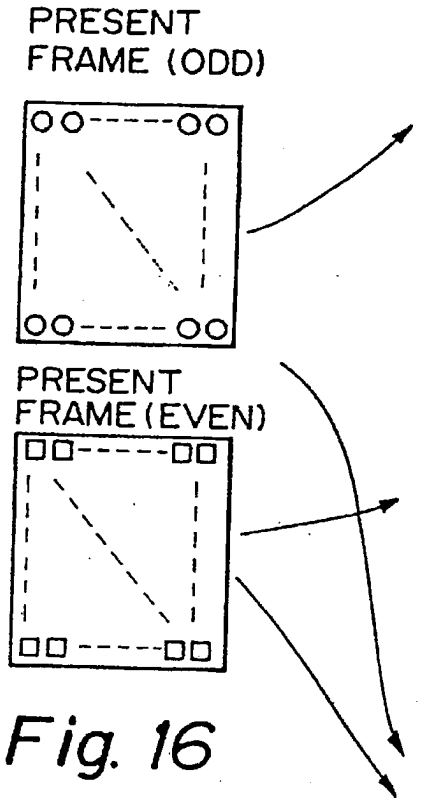


Fig. 16

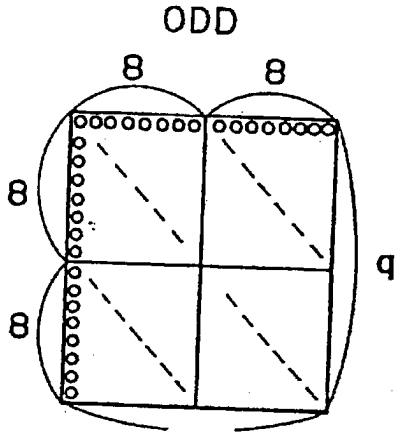


Fig. 16(A)

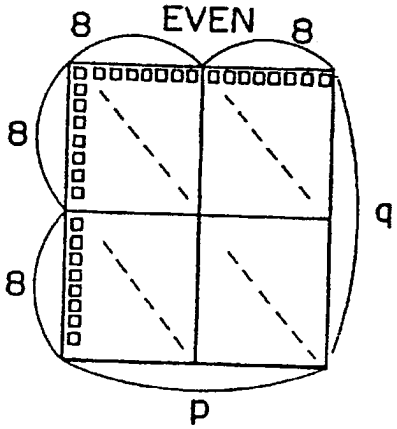


Fig. 16(B)

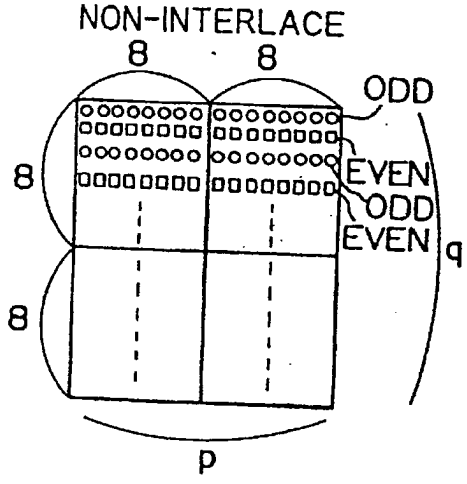
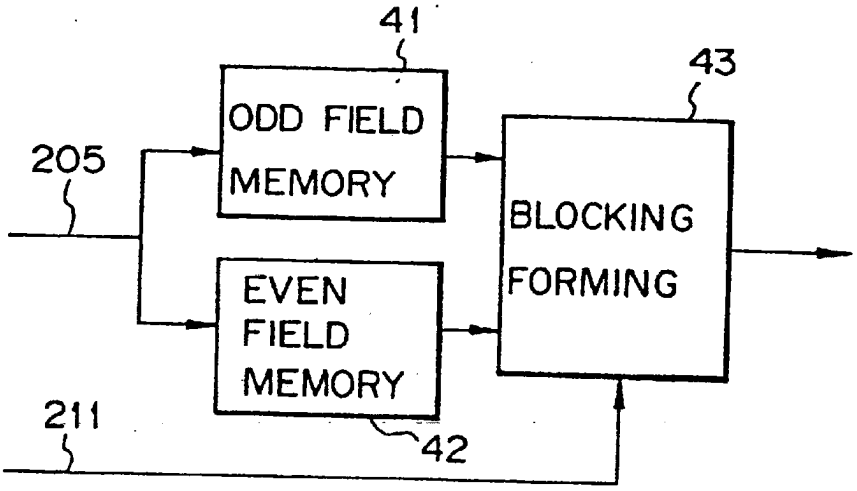


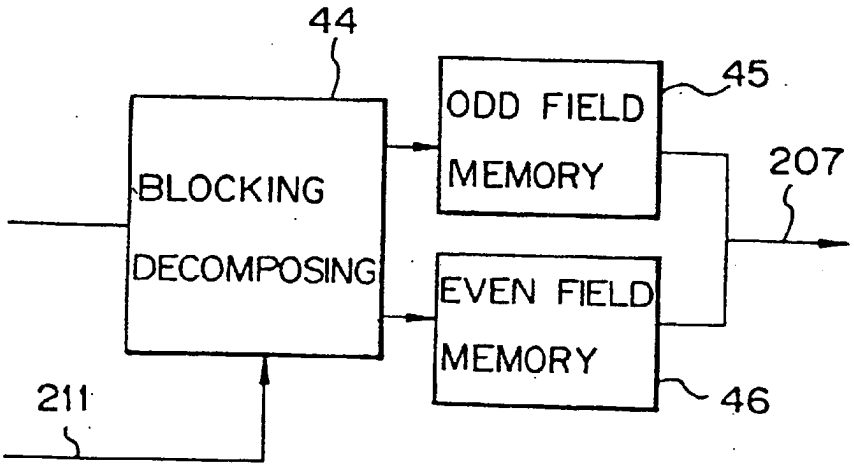
Fig. 16(C)

Fig. 17



BLOCKING FORMING SECTION

Fig. 18



BLOCKING DECOMPOSING SECTION

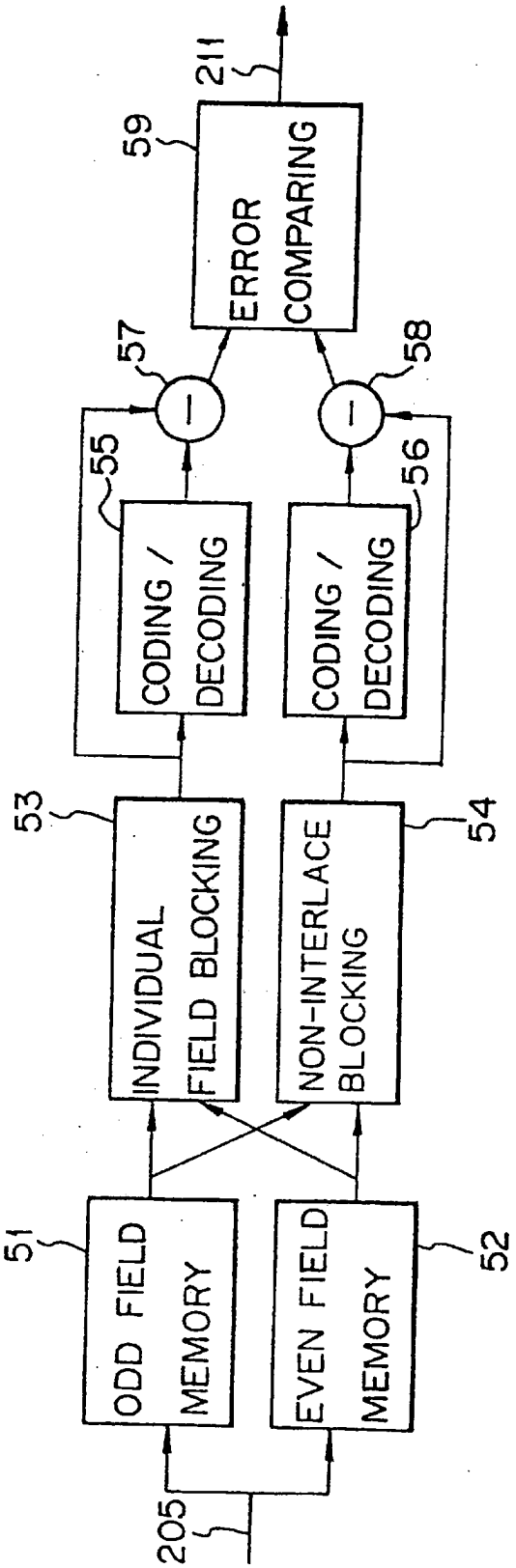

211
59
ERROR COMPARING
57
58
55
56
CODING / DECODING
CODING / DECODING
53
54
INDIVIDUAL FIELD BLOCKING
NON-INTERLACE BLOCKING
51
52
ODD FIELD MEMORY
EVEN FIELD MEMORY
205

Fig. 19

Fig. 20

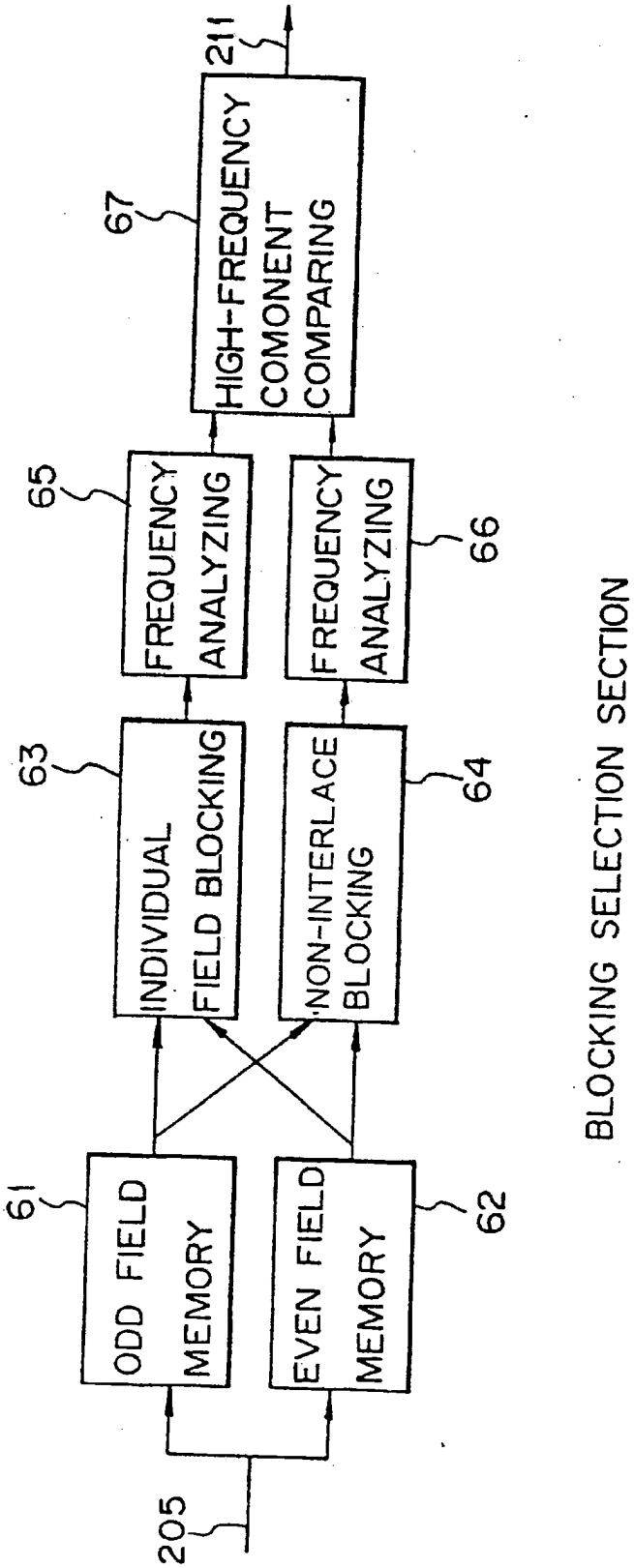

211
67
HIGH-FREQUENCY COMONENT COMPARING
65
FREQUENCY ANALYZING
66
FREQUENCY ANALYZING
63
INDIVIDUAL FIELD BLOCKING
64
NON-INTERLACE BLOCKING
61
ODD FIELD MEMORY
62
EVEN FIELD MEMORY
205
BLOCKING SELECTION SECTION

Fig. 21

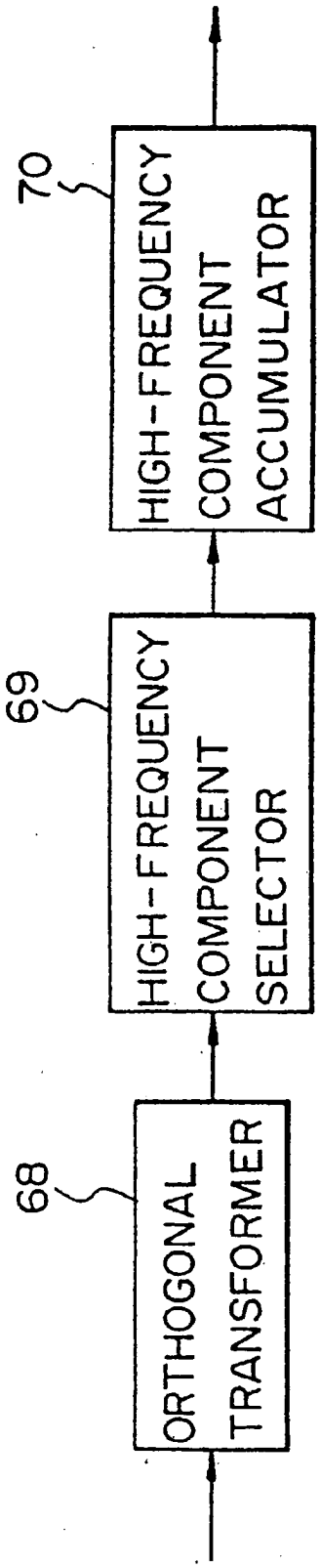
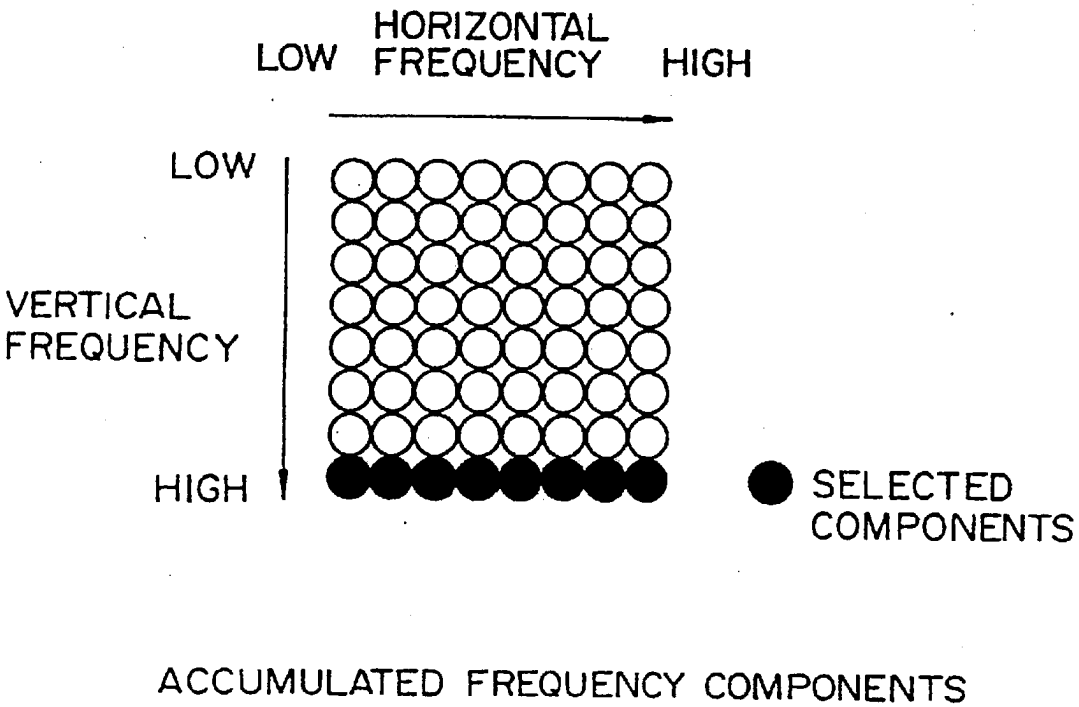

68
ORTHOGONAL TRANSFORMER
69
HIGH-FREQUENCY COMPONENT SELECTOR
70
HIGH-FREQUENCY COMPONENT ACCUMULATOR
FREQUENCY ANALYZING SECTION

Fig. 22


HORIZONTAL FREQUENCY
LOW
HIGH
LOW
VERTICAL FREQUENCY
HIGH
SELECTED COMPONENTS
ACCUMULATED FREQUENCY COMPONENTS

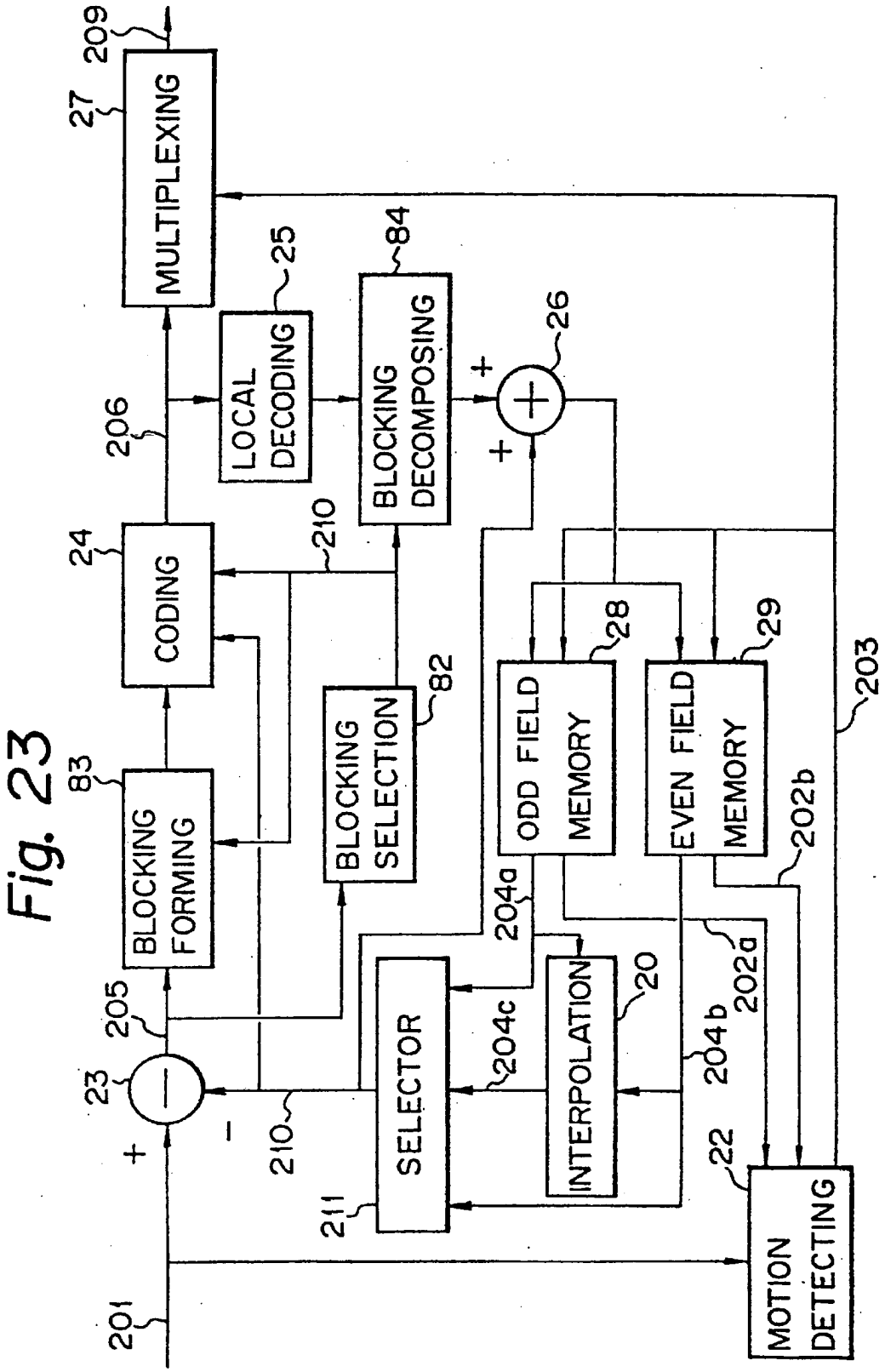

MULTIPLEXING
209
27
LOCAL DECODING
25
BLOCKING DECOMPOSING
84
26
206
CODING
24
210
BLOCKING FORMING
83
BLOCKING SELECTION
82
ODD FIELD MEMORY
28
EVEN FIELD MEMORY
29
203
202b
204a
202a
204b
204c
SELECTOR
INTERPOLATION
20
205
23
210
211
22
MOTION DETECTING
201

Fig. 23

IMAGE SIGNAL CODING SYSTEM

This application is a divisional of application Ser. No. 08/803,235, filed on Feb. 20, 1997, now U.S. Pat. No. 5,867,220 which is a continuation of application Ser. No. 08/121,293, filed Sep. 13, 1993, now U.S. Pat. No. 5,638,127, which is a divisional of application Ser. No. 07/962,299 filed Oct. 16, 1992, now U.S. Pat. No. 5,274,442, the entire contents of which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION:

1. Field of the Invention

The present invention relates to an image coding system for coding an image signal with high efficiency.

2. Description of the Prior Art

As is known in the art, means for eliminating redundant components included in an image signal is used for coding an image signal. A typical approach to image coding is the transform coding method wherein an image is divided into blocks, an orthogonal transform is carried out for each of the blocks, and the transform coefficients are encoded.

In the case of television signals such as an NTSC signal, interlaced scanning is used whereby an image signal of one frame is scanned twice, once in the odd field and once in the even field. The two fields scan different but complementary spaces of an image. The fields have image information at different times but there is a relatively strong correlation therebetween because the scanned lines of the two fields are alternate and adjacent. There is a technique in which coding is carried out after combining the fields and dividing them into blocks when coding an image signal produced by the interlaced scanning.

FIG. **1** is a block diagram showing the structure of an embodiment of "High Efficiency Image Coding System" described in the Japanese Patent Public Disclosure No. 1688/1991. In FIG. **1**, the coding system includes a non-interlacing section **1**, a motion detecting section **2**, a non-interlace blocking section **3**, an individual field blocking section **4**, an orthogonal transform section **5**, a quantizing section **6** for quantizing a conversion coefficient at the output of the orthogonal transform section **5**, and coding section **7**.

In operation, a series of input image signals **100**, which are produced by the interlaced scanning method and applied to each field, are converted to a non-interlaced signal **101** in the non-interlacing section **1** as indicated in FIG. **2**(C). As shown, the pixels belonging to the odd field and the pixels belonging to the even field appear alternately in every other line.

When an object is stationary and the correlation between adjacent lines is high, it is effective to use a non-interlaced signal and to code the image signal in a block including components from both fields. FIG. **3**(A) shows an example of such a condition. On the other hand, when an object is moving, the correlation between adjacent lines is lowered and it is considered to be effective to execute the coding in units of individual fields. This is because a non-interlaced signal is used for the moving object results in discontinuation as shown in FIG. **3**(B), causing a power to be generated in high frequency coefficients during the transform coding. In this case, the blocking as indicated in FIG. **3**(C) is adequate.

Thus, the motion detector **2** detects the motion of an object and changes the operation when the object is detected as being stationary by a signal **103** indicating motion, to conduct the blocking shown in FIG. **3**(A) (hereinafter, this

arrangement of FIG. **3**(A) is called the non-interlace blocking) in the non-interlace blocking circuit **3**. If the object is detected to be moving, the motion detector **2** changes the operation to conduct the blocking shown in FIG. **3**(C) (hereinafter, this arrangement of FIG. **3**(C) is called the individual field blocking) in the individual field blocking circuit **4**.

The blocks obtained by changing the blocking as explained above are subjected to the discrete cosine transformation (DCT) in the orthogonal transform section **5**. The transform coefficients obtained as described above are quantized in the quantizing section **6**, and a variable length code is assigned in the coding section **7** in accordance with the occurrence probability of respective events.

Since a conventional image coding system has been structured as described above, it has been difficult to realize the blocking utilizing the correlation between fields when an object is moving. Moreover, such a system has not utilized the property of different intensities in power distribution of the coefficients after conversion caused by the difference in arrangement of pixels within the block. In addition, there is the difference in power between the stationary blocks and moving blocks. The moving blocks having a high signal power which has not been utilized.

FIG. **4** is a block diagram of another conventional inter-frame predictive coding system described, for example, in the transactions on the 3rd HDTV International Work Shop, "A Study on HDTV Signal Coding with Motion Adaptive Noise Reduction" (Vol 3, 1989). In FIG. **4**, this system comprises a frame memory **21**, a motion detecting section **22**. a subtracter **23**, a coding section **24**, a local decoding section **25**, an adder **26** and a multiplexing section **27**. Although omitted in this figure, the encoded date is decoded at a receiving side in order to reproduce the transmitted signal.

In operation, the motion of an object between the current field and the field of the same type of the preceding frame is detected block by block, the block consisting of a plurality of pixels of an input image signal **201** which is provided by the interlaced scanning method and formed of frames, each frame having both odd and even fields. The motion between odd fields is detected in the motion detecting section **22** by searching the block which has the most distinctive resemblance to the currently processing block among the already encoded blocks **202**, adjacent to the position corresponding to the currently processing block in the odd fields stored within the frame memory **91**. The degree of resemblance is evaluated by using an absolute sum of differential values or a square sum of differential values of the corresponding pixels in both blocks. The amount of motion in both horizontal and vertical directions between the current block and the block determined to be the most similar is provided as a motion vector **203**. The frame memory **21** outputs a motion compensated prediction signal **204** corresponding to this motion vector **203**.

A prediction error signal **205** obtained in the subtracter **23** by subtracting the motion compensated prediction signal **204** from the input signal **201** :is applied to the coding circuit **24** in which the spatial redundancy is removed. Since low frequency components of an image signal generally occupy a greater part of the power thereof information can be compressed by quantizing high power portions with a large number of bits and quantizing low power portions with a small number of bits. According to an example of this information compression method, the frequency conversion is carried out for an 8×8 pixels block by conducting an

orthogonal transform such as a discrete cosine transform to scalar-quantize the transform coefficients. The scalar-quantized coding data **206** is sent to the local decoding section **25** and to the multiplexing section **27**. The multiplexing section **27** conducts multiplexing and encoding for the coding data **206** and the motion vector **203** to output these signals to a transmission line **209**.

Meanwhile, the local decoding circuit **25** executes the inverse operation of the operation in the coding section **24**, namely the inverse scalar quantization and inverse orthogonal transform to obtain a decoded error signal **207**. The motion compensated prediction signal **204** is added to the decoded error signal **207** in the adder **26** and stored in the frame memory **21** to detect motion of the odd field of the next frame.

In addition, the motion of the even fields of the input image signal **201** with respect to the already encoded field of the frame memory **21** is also detected for the coding of the motion compensated prediction error signal. As described above, in the conventional interframe predictive coding system, redundancy with respect to time included in moving image signals is removed by the motion compensated prediction coding and redundancy with respect to space is removed by the orthogonal transform.

Since the conventional interframe predictive coding system is structured to individually encode both the odd field and even field by predicting the current (present) odd field from the odd field of the already encoded frame and predicting the current even field from the even field of the already encoded frame, the encoding efficieny is low because the spatial correlation existing between the continuous fields, produced by the interlaced scanning method, is not used.

SUMMARY OF THE INVENTION

The present invention has been proposed to overcome the problems in the prior art. Therefore it is an object of the present invention not only to adaptively discriminate between a block which is effective for non-interlace blocking and a block which is effective for individual field blocking, but also to enhance coding efficiency by adding a class of blocking so that field correlation is used even for a moving image, the quantization accuracy is controlled and the scanning sequence of transform coeffecients is changed in accordance with switching of the blocking.

It is another object of the present invention to provide a coding system for searching motion from both odd and even fields of the frame which is already encoded in order to predict each present field.

It is a further object of the present invention to provide a coding system for enabling highly efficient coding by realizing blocking for adaptively switching the field and frame in the block coding of prediction errors.

According to the first aspect of the present invention, an adaptive blocking image coding system encodes an input image signal obtained by interlaced scanning in a unit of the block of M pixels×N lines. More specifically, the adaptive blocking image coding system comprises blocking means for selectively forming a first type block including only the pixels of M pixels×N lines belonging to the odd field of the input image signal or the pixels of M pixels×N lines belonging to the even field thereof, a second type block wherein the pixels of the M pixels×N/2 lines belonging to the odd field and the pixels of the N/2 lines belonging to the even field are arranged alternately in every other line corresponding to scanning positions on a display screen, a third type block

wherein the pixels of M pixels×N/2 lines belonging to the odd field are arranged in the upper or lower half of the block and the pixels of M pixels×N/2 lines belonging to the even field are arranged in the remaining half of the block, and a fourth type block wherein the pixels of M pixels×N/2 lines belonging to the odd field are arranged in the upper or lower half of the block, the pixels of M pixels×N/2 lines belonging to the even field are arranged in the remaining half of the block and the pixels of either field are inverted upside down in the vertical direction with respect to the display screen. The system further includes blocking determining means for determining the type of blocking by the blocking means, a transform means for orthogonally transforming the block formed by the blocking means, quantizing means for quantizing the transform coefficient obtained by the transform means, and coding means for encoding the quantized index obtained by the quantizing means.

With the structure described above, the block of the M pixels×N lines if obtained by one blocking selected from the non-interlace blocking where the pixels of M pixels×N/2 lines belonging to the odd field and the pixels of M pixels×N/2 lines belonging to the even field are arranged in every other line corresponding to the scanning positions on the display screen, an arrangement (hereinafter, called split blocking) where the pixels of M pixels×N/2 lines belonging to the odd number field are arranged in the upper half or lower half block and the pixels of M pixels×N/2 lines belonging to the even field are arranged in the remaining half block, and an arrangement (hereinafter, called inverted split blocking) where the pixels of M pixels×N/2 lines belonging to the odd field are arranged in the upper or lower half block, the pixels of M pixels×N/2 lines belonging to the even field are arranged in the remaining half block and the pixels of either field are inverted in the vertical direction with respect to the display screen. The obtained block is orthogonally transformed the transform coefficients are quantized, and then the quantization index is encoded.

According to the second aspect of the present invention, the quantizing means for quantizing the transform coefficient in the adaptive blocking image coding system variably controls the quantization accuracy in accordance with the type of arrangement blocking-processed by the blocking means.

More specifically, one of the arrangements including individual field blocking, non-interlace blocking, split blocking, or inverted split blocking is orthogonally transformed, the transform coefficient is quantized and the quantizing index is encoded with the quantizing accuracy in accordance with the information, indicating the selected blocking.

According to the third aspect of the present invention, the coding means for encoding the quantizing index produced when quantizing the transform coefficient in the adaptive blocking image coding system determines the scanning sequence (path), for quantizing the transform coefficient in accordance with the type of arrangement to be blocking-processed by the blocking means.

More specifically, one of the arrangements to be blocking-processed by the individual field blocking, non-interlace blocking, split blocking, or inverted split blocking is orthogonally transformed, the transform coefficient is quantized, and the quantizing index is encoded with the quantization accuracy and the scanning sequence in accordance with the information indicating the selected blocking.

According to the fourth aspect of the present invention, the adaptive blocking image coding system comprises

blocking determining means for selecting the type of arrangement to be blocking-processed in accordance with the value obtained by multiplying a predetermined weighting coefficient with the pixels of each line included in the block and then totaling such multiplied values.

More particularly, one of the arrangements to be blocking-processed by individual field blocking, non-interlace blocking, split blocking, or inverted split blocking is selected by the value obtained by multiplying the predetermined weighting coefficient with the pixels of each line included in the block and then totaling such multiplied values. The selected block is orthogonally transformed, the transform coefficient is quantized and the quantizing index is encoded.

According to the fifth aspect of the present invention, the adaptive blocking image coding system also comprises a blocking determining means for selecting the type of arrangement which has the minimum coefficient power of a predetermined high frequency component among the transform coefficients obtained by discrete cosine transform of the block.

In other words, one of the arrangements to be blocking-processed by individual field blocking, non-interlace blocking, split blocking, or inverted split blocking is selected in such a manner that the coefficient power of the predetermined high frequency element component is the minimum among the transform coefficients obtained by discrete cosine transform of the block. The determined block is orthogonally transformed, the transform coefficient is quantized, and the quantizing index is encoded.

According to the sixth aspect of the present invention, there is provided a coding system which individually searches the motion from both odd and even fields of the already encoded frame in order to predict the field to be encoded, the system comprising the following elements:

(a) input means for inputting an input signal to be encoded;

(b) a field memory for storing signals based on the input signal by dividing it into a plurality of fields such as the odd field and even field;

(c) predictive signal output means for outputting predictive signals of a plurality of types predicting the change of input signal on the basis of signal stored in the field memory;

(d) a selector for selecting a predictive signal from the predictive signals provided by the predictive signal output means; and

(e) coding means for encoding the input signal using the relationship between the predictive signal selected by the selector and the input signal from the input means.

With such an arrangement, the coding system can provide stabilized prediction efficiency regardless of motion of an object by making reference to both fields of the already encoded frame for the purpose of prediction.

According to the seventh aspect of the present invention, the coding system is structured to realize adaptive prediction from the searched two kinds of motion compensated predictive signals and a plurality of predictive signals combining interpolation signals of these motion compensated predictive signals.

Since the coding system as constructed utilizes a predictive signal produced by interpolating the predictive signals from both fields of the already encoded frame motion at the intermediate point of time and space of the two fields used for the prediction can be considered. Moreover, this coding system also functions as a low-pass filter, whereby the prediction efficiency can be improved and the encoded image is stabilized.

According to the eighth aspect of the present invention, the coding system executes the encoding, for example encoding prediction error signals, by adaptively switching the encoding operation from blocking of the pixels of only the odd field or even field of the frame for encodement to blocking of both odd and even fields for encodement, the system comprising the following elements:

(a) input means for inputting an input signal to be encoded by dividing into a plurality of fields such as an odd field and even field;

(b) a blocking selection section for selecting, at the time of blocking and encoding the signal from the input means, a block suitable for the encoding between the block consisting of the signal of only one kind of field and the block consisting of the signal combining signals of a plurality of fields;

(c) a block forming section for forming a block selected by the blocking selection section; and

(d) coding means for encoding a block formed by the block forming section.

The coding system having such a structure provides high efficiency encoding by selecting the blocking method most suitable for the encoding, i.e., blocking the pixels of only either of the odd field or even field, or blocking the pixels of both odd and even fields.

According to the ninth aspect of the present invention, the coding system also comprises a concrete selecting means for adaptively switching the block selection. This selecting means includes any one of the following selecting mans:

(a) selecting means for selecting the block with the least amount of encoding information from a plurality kinds of block;

(b) selecting means for selecting the block with the least amount of encoding errors from a plurality kinds of block; and

(c) selecting means for selecting the block with the least amount of high-frequency components in the signal to be encoded from a plurality kinds of block.

The coding system having such a structure enables adaptive switching of the blocking by selecting the blocking with less encoding information, the blocking with less encoding errors, or the blocking with less high frequency components included in the signal to be encoded, from the blocking of the pixels of one of only the odd or even field or the blocking of the pixels of both odd and even fields.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be more fully understood from the following detailed description and the accompanying drawings in which:

FIG. **1** is a block diagram of an image coding system in the prior art;

FIGS. **2**(A) through **2**(C) are diagrams for explaining non-interlace blocking;

FIGS. **3**(A) through **3**(C) are diagrams for explaining an adaptive blocking of the prior art;

FIG. **4** is a block diagram showing the structure of another coding system of the prior art;

FIG. **5** is a block diagram of an embodiment of the present invention;

FIG. **6** and FIGS. **6**(A) through **6**(D) are diagrams for explaining adaptive blocking in the embodiment shown in FIG. **5**;

FIG. **7** is a block diagram showing the structure of an adaptive field/frame coding system of another embodiment of the present invention;

FIG. **8** is a diagram showing an exemplary input image signal;

FIG. **9** is a block diagram showing an example of the structure of an interpolating section shown in FIG. **7**;

FIGS. **10**(A) and **10**(B) are diagrams for explaining the operation of a motion detecting circuit;

FIG. **11** is a diagram for explaining the operation for using a motion compensated predictive signal in the embodiment shown in FIG. **7**;

FIG. **12** is a block diagram showing the structure of an adaptive field/frame coding system according to another embodiment of the present invention;

FIG. **13** is a block diagram showing another example or the interpolating section;

FIG. **14** is a block diagram showing an adaptive field/frame coding system according to embodiment of the present invention;

FIG. **15** is a block diagram showing an example of the structure of the blocking selection section;

FIG. **16** and FIGS. **16**(A) through **16**(C) are diagrams showing a structural example of the block selected by the blocking selecting section;

FIG. **17** is a block diagram showing a structural example of the blocking forming section;

FIG. **18** is a block diagram showing a structural example of the blocking decomposing section;

FIG. **19** is a block diagram showing another structural example of the blocking selecting section;

FIG. **20** is a block diagram showing another structural example of the blocking selecting section;

FIG. **21** is a block diagram showing a structural example of the frequency analyzing section;

FIG. **22** is a diagram showing an example of the accumulated frequency components; and

FIG. **23** is a block diagram showing another structural example of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. **5**, an embodiment of the present invention is shown as an adaptive blocking image coding system. In FIG. **5**, the image coding system comprises a non-interlacing section **1** for conducting non-interlace processing; a blocking determination section **8**; an individual field blocking section **4**; a non-interlace blocking section **3**; a split blocking section **9**; an inverted split blocking section **10**; an orthogonal transform section **11**; a quantizing section **12** and coding section **13**. Such various types of blocking are shown in FIG. **6**. FIGS. **6**A–**6**D show individual field blocking non-interlace blocking, split blocking and inverted split blocking, respectively.

The operation will be explained with reference to FIG. **5** and FIGS. **6**A–**6**D. The input image signal series **100** which is scanned by the interlace scanning method and is inputted field by field is converted into a non-interlaced signal **101** in the non-interlace section **1**.

FIG. **2** shows a profile of non-interlace processing in the prior art similar to the non-interlace processing in the present invention. When (A) is defined as an input image signal from the odd field and (B) as an input image signal of the even field, the non-interlaced signal **101** shown in (C), alternately combining the lines from respective fields can be obtained.

The individual field blocking section **4** executes, as shown in FIG. **6**(A), blocking in which the fields are processed individually. This blocking is effective when the correlation between the fields is not available because of quick motion.

The non-interlace blocking section **3** executes the blocking shown in FIG. **6**(B). In the case of a stationary or still image, a continuous image can be obtained by non-interlaced processing of the fields. The wavelength of the signal thereby becomes substantially longer, resulting in power being concentrated on low frequency components in the successive transform coding.

The split blocking section **9** conducts the blocking as shown in FIG. **6**(C). This blocking is effective in the case where the correlation between the fields exists but the fields are noncontinuous when non-interlace blocking is carried out.

The inverted split blocking section **10** conducts the blocking shown in FIG. **6**(D). This blocking is also effective in the case where the correlation between fields exists but the fields are noncontinuous when non-interlace blocking is carried out. This blocking prevents discontinuation at the center of the block when the split blocking method is used.

The blocking determining section **8** determines the optimum blocking from a plurality of blockings as explained above and outputs a blocking arrangement selecting signal **102** for selecting the determined blocking. Here, it is important to enhance the concentration of power, on the low frequency coefficients in the transform coding. For this purpose, it is effective to evaluate the amplitude of high frequency components in each blocking and select the blocking hasting the minimum amplitude.

In one of the evaluation methods, a weight is multiplied with the pixels of each line and the obtained values are then totaled. For example, the weight of +1 is given to the lines **0, 2, 4, 6** using the line numbers shown in FIG. **6**, and the weight of −1 is given to the lines **1, 3, 5, 7**. Thereafter, the obtained values are totaled to obtain the absolute value of the sum. Moreover, the weight +1 is given to the lines **8, 10, 12, 14**, and the weight −1 is given to the lines **9, 11, 13, 15**. The obtained values are then totaled to also obtain the absolute values of the sum. Both absolute values are totaled. Thus, the weighting is inverted alternately for respective lines and it is equivalent to the evaluation of the maximum frequency component when non-interlace blocking has been conducted.

Further, the weight +1 is given to the lines **0, 4, 8, 12** and the weight −1 to the lines **2, 6, 10, 14**. The obtained values are totaled to obtain the absolute value of the sum. In addition, the weight +1 is given to the lines **1, 5, 9, 13** and the weight −1 to the lines **3, 7, 11, 15**. The obtained values are then totaled to obtain the absolute value of the sum. These absolute values are also totaled to evaluate the maximum frequency component of the individual field blocking.

In addition, the weight +1 is given to the lines **0, 4, 1, 5** and the weight −1 to the lines **2, 6, 3, 7**. The obtained values are totaled to obtain the absolute value of the sum. The weight +1 is also given to the lines **8, 12, 9, 13** and the weight −1 to the lines **10, 14, 11, 15**. The obtained values are totaled to obtain the absolute value of the sum. Both absolute values are then totaled to evaluate the maximum frequency component of the split blocking.

The weight +1 is given to the lines **0, 4, 7, 3** and the weight −1 to the lines **2, 6, 5, 1**. The obtained values are totaled to obtain the absolute value of the sum. Moreover, the weight +1 is given to the lines **8, 12, 15, 11** and the weight −1 to the lines **10, 14, 13, 9**. The obtained values are totaled to obtain the absolute value of the sum. These absolute values are totaled to evaluate the maximum frequency component of the inverted split blocking.

In another method for evaluation of each blocking, the number of orthogonal transformed coefficients having an amplitude larger than a predetermined threshold value for the respective blockings is counted, and the blocking having the minimum number is selected.

The orthogonal transform section **11** carried out the orthogonal transform of the selected block to obtain the transform coefficients. The obtained transform coefficients are quantized in a fixed sequence by the quantizing section **12**. In this case, some difference lies in the power of the coefficients depending on the type of blocking. In general, non-interlace blocking tends to be selected for a stationary region and the power is comparatively small.

Meanwhile, since the correlation between fields becomes small in a quick motion area, individual field blocking is often selected and the power is large. Moreover, split blocking and inverted split blocking are considered to be intermediate to the above two blockings. Therefore, efficiency can be improved by variably controlling quantization accuracy in accordance with the type of blocking.

The quantizing accuracy can also be controlled variably in accordance with not only the type of blocking but also the combination of actual signal power and quantization error power. In this case, it is also possible to execute variable length coding by combining the information indicating type of blocking and the information indicating quantization accuracy.

Indexes obtained by quantizing the coefficients are encoded in the coding section **13**. In this case, the coefficients are scanned from those having a larger coefficient power to those having a smaller one in order to enhance the efficiency of encoding. For the coefficients having a power lower than a certain specified value, the encoding may cease. Therefore, it is very convenient if the power distribution can be anticipated. There is a tendency with respect to the distribution of power of the coefficients that the power is increased as the frequency is lower. However, if the blocking is adaptively changing, as in the present invention, the coefficients having lower power do not always correspond to low frequency components. Then, the coding efficiency can be improved by changing the scanning sequence or path in accordance with the type of blocking.

Since the present invention is structured as explained above, the, following effects can be obtained.

The coding efficiency of transform coding is improved by switching the blocking of an image signal scanned by the interlaced scanning method into an adapted blocking. Moreover, the efficient assignment of information quantity can be realized by variably controlling the quantizing accuracy of transform coefficients correspondingly to the switching of the blocking. In addition, the encoding efficiency can also be improved in transform coding by changing the scanning sequence of the transform coefficients within the block.

Referring now to FIG. **7**, a structural diagram of an adaptive field/frame coding system according to another embodiment of the present invention is shown. The system includes an odd field memory **28** for storing local decoded signals of odd fields, an even field memory **29** for storing local decoded signals of even fields, an interpolation section **20** for interpolating a predictive signal with motion compensated from the two fields, and a selector **21** for selecting a predictive signal which gives the optimum prediction from three signals of the signals predicted from the odd and even fields and the interpolated predictive signal. In FIG. **7**, sections **200**, **300** and **500** enclosed by a broken line respectively denote motion detecting means, predicting error signal output means and coding means.

FIG. **8** shows a profile of input image signals **201** which are scanned by the interlaced scanning method, wherein the odd and even fields are alternately applied. FIG. **8** shows the fields in the coordinates where time is plotted on the horizontal axis and vertical direction on the vertical axis. In FIG. **8**, K1 indicates an odd field of the first frame, while G1, an even field of the first frame. In the same manner, K2 is an odd field of the second frame, while G2, an even field of the second frame.

FIG. **9** is a block diagram of an example of the interpolating section **20**. A simple arithmetic mean of the motion compensated prediction signal **204***a* from the inputted odd fields and the motion compensated prediction signal **204***b* from the inputted even fields is obtained and is used as an interpolation predictive signal **204***c*.

The operation will be explained with reference to FIGS. **7**, **8** and **9**. Motion of the odd fields and even fields of the present frame in relation to the preceding frame is detected in units of blocks including pixels (n×m) in response to the input image signal **201** which is scanned by the interlace scanning method and includes the odd and even fields alternately. The motion of the odd fields between the present and the preceding frames is detected by searching, in the motion detecting section **22**, the block which most resembles the currently processed block in the image signal **201** from the blocks adjacent **202***a* to the position corresponding to the currently encoded object in the already encoded odd fields stored within the odd field memory **28**.

As shown in FIG. **10**, for example, it is assumed that image H1 exists within one block unit (n×m) in the preceding frame, and the image moves to position H2 from position H1 in the present input image signal. The motion detecting section **22** outputs a motion vector **203** which indicates the block has moved horizontally to H2 from H1. In this case, since motion is not detected in the vertical direction, the motion vector **203** has the value of 0 with regard to vertical direction. The motion in the horizontal and vertical directions thus obtained is outputted as the motion vector **203**.

The odd field memory **28** outputs a motion compensated prediction signal **204***a* corresponding to this motion vector **203**. Similarly, compensation for motion of the even fields in the preceding frame is carried out in the motion detecting section **22**, by searching the block resembling the currently processed block from the adjacent blocks **202***b* within the even field memory **29** and outputting the result as the motion vector **203**. The motion compensated prediction signal **204***b* corresponding to this motion vector **203** is outputted from the even field memory **29**.

The interpolation processing is carried out in the interpolating section **20** shown in FIG. **9**, by using the motion compensated prediction signals **204***a* and **204***b* to generate the interpolation predictive signal **204***c*, signal **204***a* being generated by motion compensated in accordance with the motion vector **203** and provided from the odd field memory **28**, and motion compensated predictive signal **204***b* being generated by motion compensated in accordance with the motion vector **203** and provided from the second field memory **9**. A predictive signal having the minimum error signal power with respect to the currently encoding object block of the input image signal **201** is selected by the selector **21** from among the motion compensated prediction signal **204***a* obtained from the odd field, the motion compensated prediction signal **204***b* obtained from the even field, and the interpolated motion compensated prediction signal **204***c*, and then the predictive signal **210** is produced.

FIG. **11** is a diagram showing the operation explained above. It is assumed that the odd field memory **28** shown in FIG. **7** stores an odd field K1 of the preceding (previous) frame, while the even field memory **29** of FIG. **7** stores an even field G1 of the preceding frame. Here, the case where an odd field K2 and an even field G2 are included in the current (present) frame of the input image signal **201** will be discussed. First, when the odd field K2 is inputted, the motion compensated prediction signal **204***a* from the odd field K1 of the preceding frame stored in the odd field memory **28** is provided to the selector **21**. In the same manner, the even field G1 of the preceding frame stored in the even field memory **29** is provided to the selector **21** as the motion compensated prediction signal **204***b*. Then, the data of K1 and G1 are applied to the interpolating section **20** and the interpolation processing as shown in FIG. **9** is conducted. Thereafter, such data is supplied to the selector **21** as the motion compensated prediction signal **204***c*. The selector **21** compares these three kinds of motion compensated prediction signals **204***a*, **204***b*, **204***c* and the input image signal **201** to select the prediction signal which has the minimum error signal power.

In the same manner, the selector **21** is responsive to the even field G2 of the current frame to receive the prediction signal **204***a* based on the odd field K1 stored in the odd field memory **28**, the motion compensated prediction signal **204***b* based on the even field G1 stored in the even field memory **29**, and the motion compensated prediction signal **204***c* obtained by the interpolation process on the basis of these motion compensated prediction signals **204***a*, **204***b* based on both fields, and to select the prediction signal which has the minimum error signal power.

In this embodiment (FIG. **7**), the interpolation section is provided to conduct the interpolation processing based on the motion compensated prediction signals **204***a*, **204***b* from the odd field memory **28** and even field memory **29** and thereby motion compensated prediction signal **204***c* is produced. However, it is also possible that the interpolation section **20** is not used as shown in FIG. **12**. In this case, the motion compensated prediction signal is generated in the selector **21** on the basis of the preceding odd field K1 stored in the odd field memory **28** and the preceding even field G1 stored in the even field memory **29** and the selector **21** selects the prediction signal minimizing the error signal power in these two kinds of motion compensated prediction signals **204***a*, **204***b*.

Further, in the embodiment shown in FIG. **7** the simple arithmetic mean has been used for the interpolation section, but coding ensuring higher prediction efficiency can be realized by utilizing a weighted arithmetic mean taking into consideration field distance, as will be explained hereunder with reference to FIG. **13**.

FIG. **13** is a block diagram of an example of the interpolation circuit **20**. The motion compensated prediction signal **204***a* from the odd field is multiplied by a weight α based on the distance to the field to be encoded, and the motion compensated prediction signal **204***b* from the even field is multiplied by a weight β based on the distance to the field to be encoded. Thereafter, the arithmetic mean of these values is obtained and the output thereof is used as interpolation predictive signal **204***c*.

The practical value of the weighting by the interpolation section **20** in relation to the embodiment shown in FIG. **13** will be explained with reference to FIG. **11**.

As shown in FIG. **11**, when T is considered a unit of time for inputting an odd field or an even field, there is a time difference of 2T between odd field K1 and odd field K2. On the other hand, there is a time difference of T between even field G1 and odd field K2. Thus, the weights α and β can be determined by utilizing such time differences. For example, since the odd field K1 has a time distance of 2 T, the weight α is set to 1. Also, since even field G1 has a time distance of T from odd field K2, the value of weight can be increased for the field having the lesser time distance by setting the value of β B to 2. In the same manner, odd field K1 has a time distance of 3 T from even field G2 and even field G1 has a time difference of 2 T. Thus, it is possible to give the value of weight which is proportional to the time difference by setting α to 2 and β to 3 for weighting even field G2.

In the embodiment shown in FIG. **13**, the weights α and β are determined in the interpolating section on the basis of time distance. However, it is also possible that the weight α to be given to the odd field is always set, for example, larger or smaller than weight β to be given to the even field regardless of the time distance. Further, in this embodiment, weights α and β used for the odd fields are different from those used for the even fields, but the weights for the odd fields may be equal to those for the even fields. In addition, in this embodiment only weights α and β are used, but the weights may be determined in accordance with the other coefficients, for example, a coefficient having a quadratic function or another function having particular characteristics. Moreover, weights α and β do not have to be restricted only to one kind of value; it is possible that several kinds of weights α and β are prepared and selected in accordance with the kind of input signal or the characteristic of input signal.

Another embodiment of the present invention will be explained with reference to FIG. **14**.

The embodiment shown in FIG. **14** comprises a blocking selection section **82** for selecting between an individual blocking of a prediction error signal for the odd and even fields and a non-interlace blocking including both odd and even fields; a blocking forming section **83** for conducting the blocking in accordance with the output of the blocking selection section **82**; and a blocking decomposing section **84** for decomposing the blocking to form the original field in accordance with the block selection output. Section **400** enclosed by a broken line denotes blocking means and the other sections **200**, **300**, **500** are similar to those shown in FIG. **7**.

FIG. **15** is a block diagram of an example of the blocking selection section **82**. The prediction error signal **205** is stored in the odd field memory **31** for the odd field and in the even field memory **32** for the even field. As shown in FIG. **16**(*a*) and **16**(*b*), a block of p=16, q=16 is considered. The individual field blocking section **33** executes the blocking including the pixels of either of the odd or even field within the block of (p pixelsxq lines), and these pixels are encoded in a coding section **35**. As shown in FIG. **16**(*c*), a non-interlace blocking section **34** executes the blocking of (p pixelsxq lines) included in the block by alternately arranging the pixels of both odd and even fields, and these pixels are encoded in a coding circuit **36**. The information quantity comparing section **37** compares the quantity of data encoded in the coding section **35** and the coding circuit **36**, and outputs a blocking selection signal **211** indicating the blocking having the least amount of information.

FIG. **17** is a block diagram of an example of the blocking forming section **83**. The prediction error signal **205** is stored in the odd field memory **41** for the odd field and in the even field memory **42** for the even field. In accordance with the

blocking selection signal **211** supplied from the blocking selection section **82**, the blocking forming section **43** selects the blocking of the prediction error signals stored in the odd field memory **41** and even field memory **42** from the blocking including pixels of either of the odd or even field within the block of (p pixels×q lines) and the blocking including pixels of both odd and even fields within the block of (p pixels×q lines), and then outputs the blocked prediction error signal.

FIG. **18** is a block diagram of an example of the blocking decomposing section **84**. The data decoded by a local decoding circuit **25** is applied to the blocking decomposing section **44** in which the blocking is decomposed in accordance with the blocking selection signal **211** from the blocking selecting section **82**, and the decomposed block is then stored in the individual field memories **45**, **46**. The stored data is supplied as a decoded error signal **207**.

The operation of this embodiment is explained hereunder.

The prediction error signal **205** obtained by subtracting the prediction signal **210** from an input signal **201** in a difference circuit **23** is sent to the blocking forming section **83** shown in FIG. **17** and to the blocking selection section S8 shown in FIG. **15**. The blocking selection section **82** produces the blocking selection signal **211** for selecting the blocking including the pixels of either the odd or e-en field in the block of (p pixels×q lines), or the blocking including the pixels of both odd and even fields in the block of (p pixels×q lines). The blocking forming section **83** conducts individual field blocking or non-interlace blocking in units of (p×q) blocks in accordance with the blocking selection signal **211**. The blocked signal Is applied to the coding circuit **24**. The coding section **24** execute the orthogonal transform and sends the encoded data **206** which is a scalar-quantized transform coefficient to both the local decoding section **25** and the multiplexing section **28**.

After the inverse scalar-quantization and inverse orthogonal transform by the local decoding section **25**, the data is decomposed into the odd and even fields in the blocking decomposing section shown in FIG. **18** which decomposes the blocking into the fields in accordance with the blocking selection signal **211** in order to obtain the decoded difference signal **207**. The local decoded signal **208** obtained by adding a predictive signal **210** to the decoded difference signal **207** in the adder **207** is stored in the first field memory **28** when it is the odd field or in the second field memory **29** when it is the even field, to detect the motion of each field of the next frame.

In this embodiment, a unit of blocks is formed of p=16, q=16, but it is desirable that the values of p and q have the following relationship with the block size n×m used by the motion detecting section **22** as explained in the embodiment shown in FIG. **7**:

p=n, q=2m

Since DCT transform is often carried out in the block unit of 8 pixels×8 lines, the size of 16 pixels×16 lines combining four block units is selected as the values of p and q in the blocking forming section. In this example, since P=n, n=16 pixels. Also, since q=2m, m=8. Thus, it is desirable that the number of lines be reduced to 8 because the motion detecting section **22** detects motion for both the odd and even fields. Meanwhile, since it is possible to employ the blocking combining the odd field and even field in the blocking forming section, it is desirable to form a block of 16 lines including the odd and even fields.

In the embodiment shown in FIG. **14**, the blocking has been selected by comparing the quantity of information generated as shown in FIG. **15**, but coding based on the quality of encoding can be realized by selecting the blocking on the basis of the comparison of encoding quality as shown in FIG. **19**.

FIG. **19** is a block diagram of an example of the blocking selection section **82**. The predicting error signal **205** is stored in the odd field memory **51** for the odd field and in the even field memory **52** for the even field. The individual field blocking section **53** realizes the blocking including the pixels of either the odd field or the even field within the block of (p pixels×q lines), and the coding/decoding section **55** enables encoding/decoding. At the same time, the non-interlace blocking section **54** realizes the blocking including the pixels of both fields within the block of (p pixels×q lines), and the coding/decoding circuit **56** enables coding/decoding. The difference between the encoded/decoded data of the individual field blocking and the data just before the encoding is compared with the difference between the encoded/decoded data of the combined field blocking and the data just before the encoding, by the error comparator **59** in order to select the blocking with less errors and to provide an output as the blocking selection signal **211**.

In the embodiment shown in FIG. **14**, the quantity of generated information has been compared for the selection of the block, while in the embodiment shown in FIG. **19**, the encoding errors have been compared. However, encoding with higher efficiency can be realized when conducting encoding utilizing the orthogonal transform, by selecting the blocking on the basis of the comparison of frequency components produced by the difference of blocking as shown in FIG. **20**.

FIG. **20** is a block diagram of an example of the blocking selection circuit **82**. The predicting error signal **205** is stored in the odd field memory **61** for the odd field and in the even field memory **62** for the even field. The individual field blocking section **63** executes the blocking including the pixels of only either the odd field or even field within the block of (p pixels×q lines), and a frequency analyzing section **65** such as that shown in FIG. **21** executes the frequency analysis. The non-interlace blocking circuit **64** executes the blocking including pixels of both fields within the block of (p pixels×q lines), and a frequency analyzing circuit **66** such as that shown in FIG. **21** executes the frequency analysis. The blocking with fewer high-frequency components is selected from the individual field blocking and the combined field blocking to output the blocking selection signal **211**.

FIG. **21** is a block diagram of an example of the frequency analyzing sections **65** and **66**. The signal obtained by individually blocking the odd and even fields from the individual field blocking circuit **63**, and the signal obtained by blocking the pixels of both odd and even fields from the non-interlace blocking section **64**, are supplied to sections **65** and **66**. These signals are converted to a signal in the frequency domain from a signal in the pixel domain using the orthogonal transform **68**. The high-frequency components are extracted from the converted signal in the frequency domain by a high-frequency component selector **69** and the extracted high-frequency components are totaled by a high-frequency component accumulator **70**. The accumulated high-frequency components are compared in a high-frequency component comparing section **67** to select the blocking with fewer amount high-frequency components.

FIG. **22** shows an example of the components accumulated by the high-frequency component adder **70** from the orthogonal transformed frequency domain signal. Here, eight components, for example, having the maximum frequency component in the vertical frequency component, are selected.

In this embodiment, the coding section **24** does not use the selection information of predictive signals or the selection information of blocking, but according to another embodiment shown in FIG. **23**, finer control is possible and high encoding quality can be realized by inputting an output of the selector **11** as the selection signal for the predictive signal and the blocking selection signal as the selection signal for the blocking to the coding section **24** and by controlling the encoding characteristic with the selected prediction signal and the information of the selected blocking.

As explained above, the embodiment of FIG. **7** relates to a system for realizing predictive coding of an input image signal obtained by the interlaced scanning method with the motion compensation. The system includes motion detecting means for obtaining, for the odd or even field of the input image signal, the amount of displacement, in order to carry out the individual motion compensated prediction, in units of the block of (n pixels×m lines) (n and m: positive integer) from both the odd and even fields of the already encoded frame, and the prediction error signal output means for selecting, with a selector **21**, the predictive signal indicating the optimum prediction from signals including a first predictive signal **204***a* obtained by the motion compensation from the odd field, a second predictive signal **204***b* obtained by the motion compensation from the even field, and a third predictive signal **204***c* obtained by interpolating the first and second predictive signals in order to obtain the difference from the field of the input signal and output the result as the prediction error signal.

Moreover, the embodiment of FIG. **7** is an adaptive field/frame coding system characterized in that the interpolation means for obtaining the third predictive signal is the simple arithmetic mean of the first predictive signal and the second predictive signal.

Thus, the hardware can be minimized in size and encoding with higher prediction efficiency can be realized by generating an interpolation signal of the predictive signal by simply obtaining the arithmetic mean of both predicted odd and even fields with motion compensation.

Further, the embodiment of FIG. **13** is an adaptive field/frame coding system characterized in that the interpolation means for obtaining the third predictive signal is the weighted arithmetic mean of the first predictive signal and the second predictive signal, also considering the time distance of the field used for the prediction and the field to be encoded.

Thus, encoding ensuring very high prediction efficiency can be realized by generating the interpolation signal from the weighted arithmetic mean of both predicted odd and even fields with the motion compensation, while considering the time distance of the field used for the prediction and the field to be encoded.

The embodiment shown in FIG. **14** is an adaptive field/frame coding system comprising means for enabling encoding by selecting blocking including the pixels of either the odd field or even field within the block of (p pixels×q lines), or blocking including the pixels of both odd and even fields within the block of (p pixels×q lines), in order to encode the prediction error signal for the odd and even fields of the input image signal in units of the block of (p pixels×q lines) (p and q: positive integer).

Moreover, the embodiment shown in FIG. **14** is an adaptive field/frame coding system characterized in that the blocking means for enabling encoding while selecting the blocks comprises selecting means for selecting the blocking with less information for encoding from blocking including the pixels of only one of the odd field and even field within the block of (p pixels×q lines), and blocking including the pixels of both odd and even fields within the block of (p pixels×q lines).

The embodiment shown in FIG. **19** is an adaptive field/frame coding system characterized in that the blocking means for enabling encoding while selecting the blocks comprises means for selecting the blocking with less encoding error from blocking including the pixels of only one of the odd field and even field within the block of (p pixels×q lines), and blocking including the pixels of both odd and even fields within the block of (p pixels×q lines).

The embodiment shown in FIG. **20** is an adaptive field/frame coding system characterized in that the blocking means for enabling encoding while selecting the blocks comprises selecting means for selecting the blocking with less high-frequency components included in the signal to be encoded from blocking including the pixels of only one of the odd field and even field within the block of (p pixels×q lines), and blocking including the pixels of both odd and even fields within the block of (p pixels×q lines).

In addition, the embodiment shown in FIG. **23** is an adaptive field/frame coding system characterized by enabling encoding while selecting the quantization characteristic of the transform coefficient in accordance with the selected predictive signal and the selected blocking, in the case of employing the orthogonal transformer and carrying out encoding by the quantization of transform coefficient in the coding section for the encoding in units of the block of (p pixels×q lines).

In the above embodiments, an input image signal **201** is formed of the frame including the odd field and even field. However, the use of the odd field and even field is intended to show only an example, and the field is not restricted to the odd or even field. The present invention can be useful whenever one frame is divided into fields, the odd field and even field being only examples of such fields of a frame. For instance, the present invention can also be applied to a case of storing data by dividing the frame into two fields every two lines by, for example defining the first field as the 1st and 2nd lines and the second field as the 3rd and 4th lines, and defining the first field as the 5th and 6th lines and the second field as the 7th line and 8th line, etc. Moreover, in addition to dividing a frame into two kinds of fields, such as the odd field and the even field or the first field and the second field, the present invention can also be applied to the case of dividing a frame into more than two fields, for example, three or four kinds of fields. In such a case, the number of field memories corresponds to the number of kinds of fields, and the processing explained above is carried out for each field.

In the above embodiments, the blocking selection section selects the blocking from two kinds of blocking, including the blocking of the pixels of only one of the odd field and even field and the blocking of the pixels of both odd and even fields. However, the blocking may include various combinations when two or more fields are prepared in addition to the odd and even fields. The blocks shown in FIGS. **16**(*a*), (*b*), (*c*) are only examples and various block forming methods may be used to form the block other than the blocks of FIG. **16**.

In the above embodiments, the blocking means shown in FIG. **14** is used with the prediction error signal output means and motion detecting means. Even if the sections other than the blocking means **400** are replaced with conventional means, the 8th and 9th aspects explained above can be provided.

According to the 6th and 7th aspect explained above, a stable encoded image with high efficiency can be obtained by individually searching the motion from each field of the already encoded frame to predict each field and by conducting adaptive prediction from the searched motion compensated predictive signals (and interpolation signals).

In addition, according to the 8th and 9th aspects explained above, a stable encoded image with high efficiency can also be obtained by adaptively selecting the encoding from the blocking of the pixels of only one of the fields of the frame to be encoded, and the encoding after conducting the blocking of the pixels of the respective fields when encoding the prediction error signal.

What is claimed is:

1. A video signal encoder for encoding a first motion video signal representative of sequential video images including first and second video images into a second motion video signal comprising:

a predictive error signal generator for generating a predictive error signal representative of the error in the second video image based on a prediction formed at least in part from the first video image;

a coder for transform coding the predictive error signal to produce a coded predictive error signal, said coder varying the scanning sequence of the transform coefficients thereof;

a local decoder detecting the scanning sequence of transform coefficients used in transform coding, and decoding the transform coefficients of the coded predictive error signal to produce information representative of the first motion video signal including the first video image;

a combiner, operatively connected to said local decoder, and combining the predictive error signal with a predictive signal;

a field memory, operatively connected to said combiner, for storing information representative of the first video image as plural image fields;

a predictive signal generator, operatively connected to said field memory, and supplying the predictive signal from the plural fields stored in said field memory to said predictive error signal generator and said combiner;

wherein a signal representative of the second video image of the first motion video signal is assembled from the predictive error signal developed from a difference between the first video image and the second video image;

wherein the coded predictive error signal from said coder is output as the second motion video signal.

2. The encoder of claim 1 wherein said coder varies the scanning sequence used in transform coding based on encoding efficiency.

3. The encoder of claim 1 wherein:

said predictive error signal generator includes a subtracter, operatively connected to said predictive signal generator, and subtracting the predictive signal from a signal representative of the second video image of the first motion video signal to form the predictive error signal; and

a block former, operatively connected to said subtracter, and forming the predictive error signal into blocks;

said coder being operatively connected to said block former, and encoding the blocked predictive error signal to form the coded predictive error signal.

4. A video signal conversion system for converting between a first motion video signal representative of sequential video images including first and second video images and a second motion video signal comprising:

a decoder detecting the scanning sequence of transform coefficients used in transform coding, and decoding the transform coefficients to produce information representative of the first and second video images;

a field memory for storing information representative of the first video image as plural image fields;

a predictive signal generator, operatively connected to said field memory, and supplying a predictive signal from the plural fields stored in said field memory;

wherein a signal representative of the second video image is assembled from a predictive error signal output from said decoder and developed from a difference between the first video image and the second video image; and

a combiner, operatively connected to said field memory, and combining the signal representative of the second video image with the predictive signal produced by said predictive signal generator.

5. The video signal conversion system of claim 4 wherein the scanning sequence used in transform coding the transform coefficients is determined based on coding efficiency.

6. The video signal conversion system of claim 4 wherein the conversion system converts from the first motion video signal to the second video signal.

7. The video signal conversion system of claim 4 wherein said field memory stores plural image fields and said predictive signal generator supplies plural predictive signals from the plural image fields, said predictive signal generator including,

an interpolator, operatively connected to said field memory, interpolating at least some of the plurality of predictive signals and generating an interpolated predictive signal which is different from any of the plurality of predictive signals supplied by said predictive signal generator, and

a selector, receiving the plural predictive signals and the interpolated predictive signal, and selecting a predictive signal from the plurality of predictive signals and the interpolated predictive signal.

8. The video signal conversion system of claim 7 wherein said combiner includes an adder, said adder adding the predictive error signal and the interpolated signal produced by said interpolator and supplying the output thereof to said field memory.

9. The video signal conversion system of claim 7 further comprising:

a subtracter, operatively connected to said selector, and subtracting one of the plural predictive signals including the interpolative predictive signal from a signal representative of the second video image of the first motion video signal to form the predictive error signal; and

an encoder, operatively connected to said subtracter, and encoding the predictive error signal to form an encoded predictive error signal, wherein said encoder varies the scanning sequence used in transform coding the transform coefficients;

said decoder being operatively connected to said encoder, for decoding the encoded predictive error signal for supply to said combiner.

10. The video signal conversion system of claim 7 wherein the interpolator produces the interpolated predictive signal by computing the arithmetic mean of at least some of the plural predictive signals.

* * * * *

Exhibit 7

US006097759A

United States Patent [19]

Murakami et al.

[11] Patent Number: 6,097,759

[45] Date of Patent: Aug. 1, 2000

[54] **IMAGE SIGNAL CODING SYSTEM**

[75] Inventors: **Tokumichi Murakami; Kohtaro Asai; Hirofumi Nishikawa; Yoshihisa Yamada**, all of Kanagawa-ken, Japan

[73] Assignee: **Mitsubishi Denki Kabushiki Kaisha**, Tokyo, Japan

[21] Appl. No.: **09/444,455**

[22] Filed: **Nov. 22, 1999**

Related U.S. Application Data

[62] Division of application No. 09/207,919, Dec. 9, 1998, Pat. No. 5,990,960, which is a division of application No. 08/803,235, Feb. 20, 1997, Pat. No. 5,867,220, which is a continuation of application No. 08/121,293, Sep. 13, 1993, Pat. No. 5,638,127, which is a division of application No. 07/962,299, Oct. 16, 1992, Pat. No. 5,274,442.

[30] **Foreign Application Priority Data**

Oct. 22, 1991 [JP] Japan 3-273843
Feb. 4, 1992 [JP] Japan 4-80654

[51] **Int. Cl.**[7] **H04N 7/36**

[52] **U.S. Cl.** **375/240**; 348/409; 348/415

[58] **Field of Search** 348/384, 390, 348/400, 401, 402, 403, 404, 405, 409, 415, 416, 420; 382/232, 233, 236, 238

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,437,119	3/1984	Matsumoto et al.	348/412
4,546,386	10/1985	Matsumoto et al.	348/412
4,571,618	2/1986	Hatori et al.	348/412
4,675,733	6/1987	Tanimoto	348/399
4,691,329	9/1987	Juri et al.	348/420
4,703,351	10/1987	Kondo	348/415
4,772,947	9/1988	Kono	348/420
4,783,698	11/1988	Harney	348/390
4,849,812	7/1989	Borgers	348/400
4,931,869	6/1990	Amor et al.	348/403
5,045,938	9/1991	Sugiyama	348/408
5,046,119	9/1991	Hoffert et al.	348/391
5,068,724	11/1991	Krause et al.	348/402
5,083,720	1/1992	Krause	348/413
5,091,782	2/1992	Krause et al.	348/400
5,157,747	10/1992	Nuhara	348/416
5,193,004	3/1993	Wang et al.	348/420
5,274,442	12/1993	Murakami et al.	348/405
5,347,309	9/1994	Takahashi	348/420
5,416,523	5/1995	Murakami et al.	348/420
5,428,693	6/1995	Murakami	348/415
5,583,657	12/1996	Jeong	348/408
5,638,127	6/1997	Murakami et al.	348/412
5,767,909	6/1998	Jung	348/403
5,838,825	11/1998	Obayashi	382/233

FOREIGN PATENT DOCUMENTS

385654	2/1989	European Pat. Off. .
484140	5/1992	European Pat. Off. .
490799	6/1992	European Pat. Off. .
499307	8/1992	European Pat. Off. .
510972	10/1992	European Pat. Off. .
58-137379	8/1983	Japan .
62-102685	5/1987	Japan .
63-224491	9/1988	Japan .
1278184	11/1989	Japan .

(List continued on next page.)

OTHER PUBLICATIONS

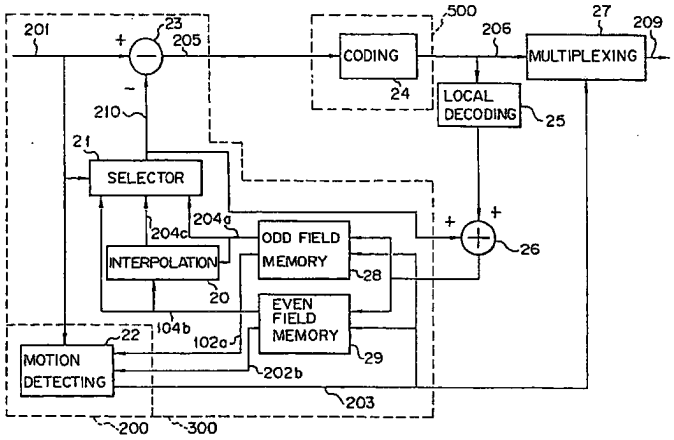
Chiang, et al. "Compatible Coding of Digital Interlaced HDTV Using Prediction of the Even Fields from the Odd Fields", Apr. 9, 1991, pp. 523–530.

Primary Examiner—Bryan Tung

[57] **ABSTRACT**

An adaptive blocking coding system selects an effective blocking of an input image signal to be encoded in accordance with the correlation between fields, even if motion is detected between the fields. The blocking patterns include an individual field blocking, a non-interlace blocking, a split blocking and an inverted split blocking. Further, the coding system searches for motion from both odd and even fields of a frame for producing a motion compensated prediction signal in order to provide high-efficient coding.

10 Claims, 21 Drawing Sheets



FOREIGN PATENT DOCUMENTS

220082	8/1990	Japan .
3001688	1/1991	Japan .
3097320	4/1991	Japan .
4-167882	6/1992	Japan .
4178088	6/1992	Japan .
4-252690	9/1992	Japan .
4-288790	10/1992	Japan .
5022718	1/1993	Japan .
WO 9210060	6/1992	WIPO .

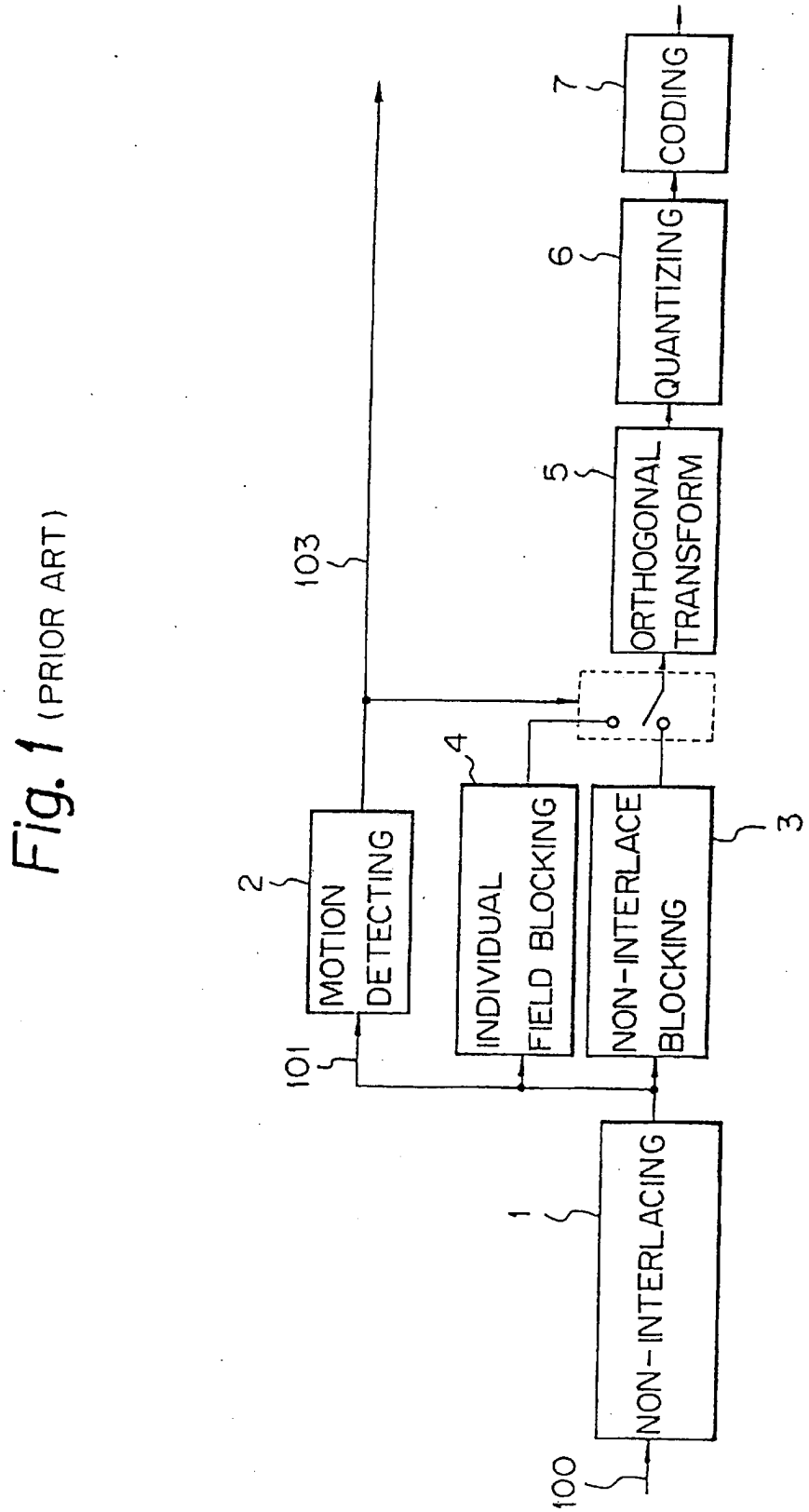
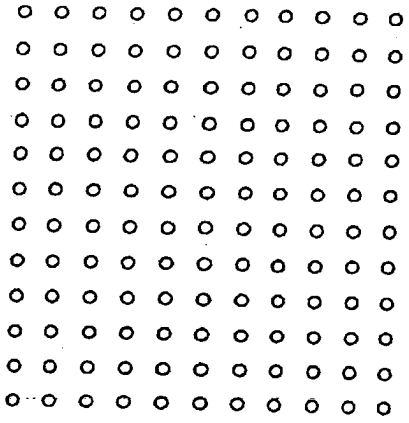
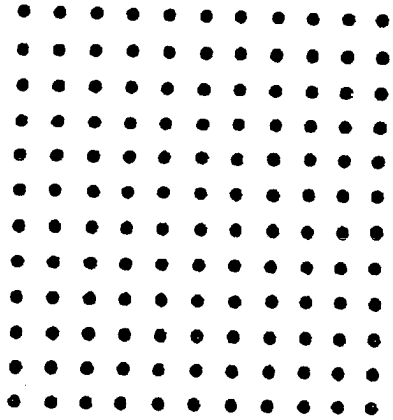


Fig. 1 (PRIOR ART)



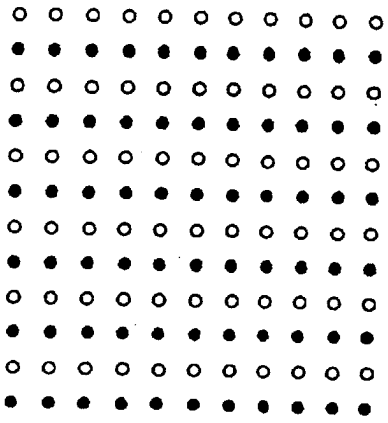
ODD FIELD

Fig. 2(A)
PRIOR ART



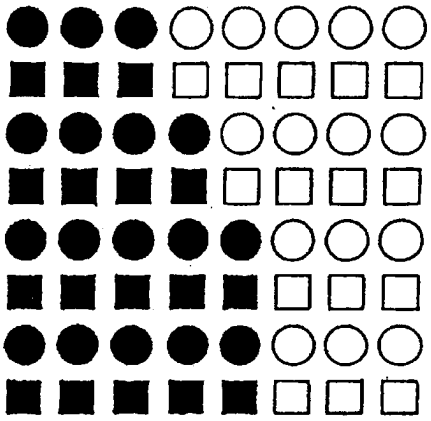
EVEN FIELD

Fig. 2(B)
PRIOR ART



NON-INTERLACED FRAME

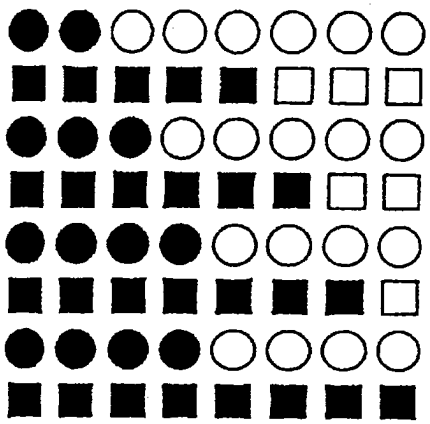
Fig. 2(C)
PRIOR ART



NON-INTERLACE IS SUITABLE

Fig. 3(A)

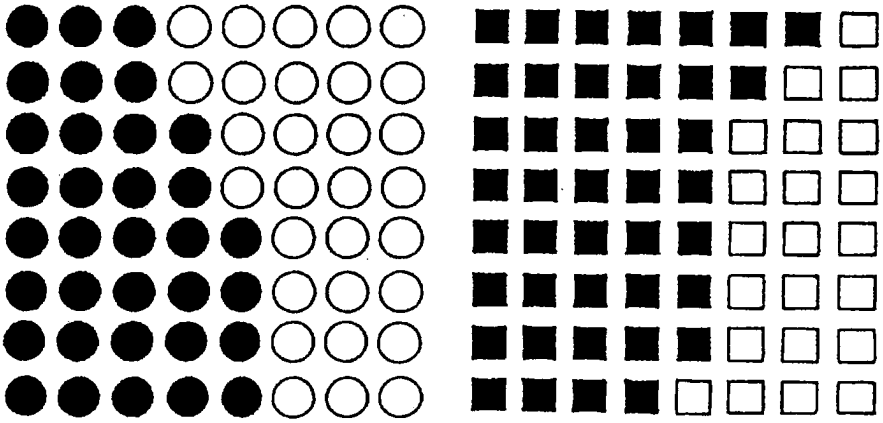
PRIOR ART



NON-INTERLACE IS NOT SUITABLE

Fig. 3(B)

PRIOR ART



INDIVIDUAL FIELD BLOCKING IS SUITABLE

Fig. 3(C)

PRIOR ART

○: ODD FIELD □: EVEN FIELD

(THIS DENOTATION IS USED ONLY HERE.)

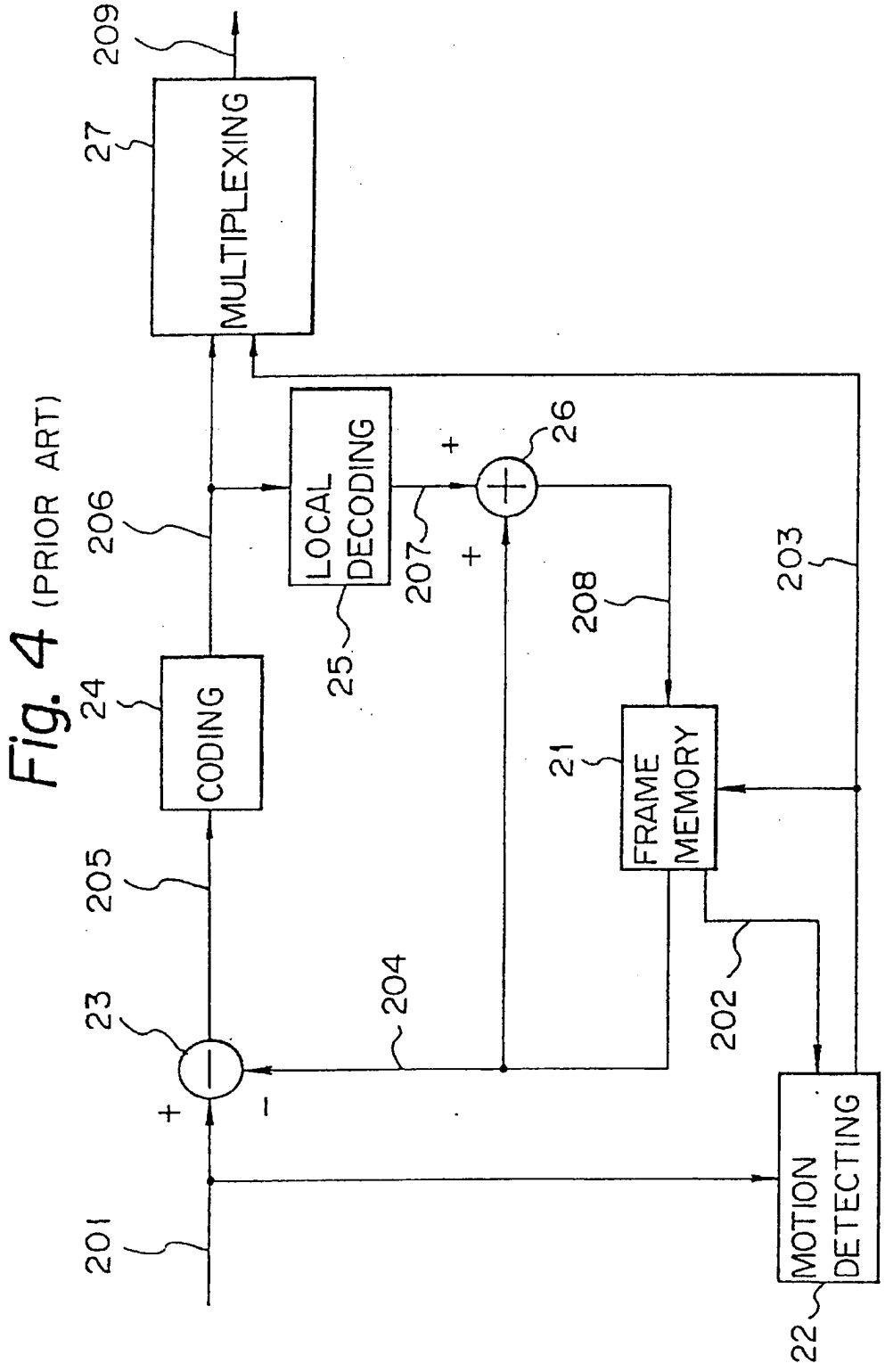
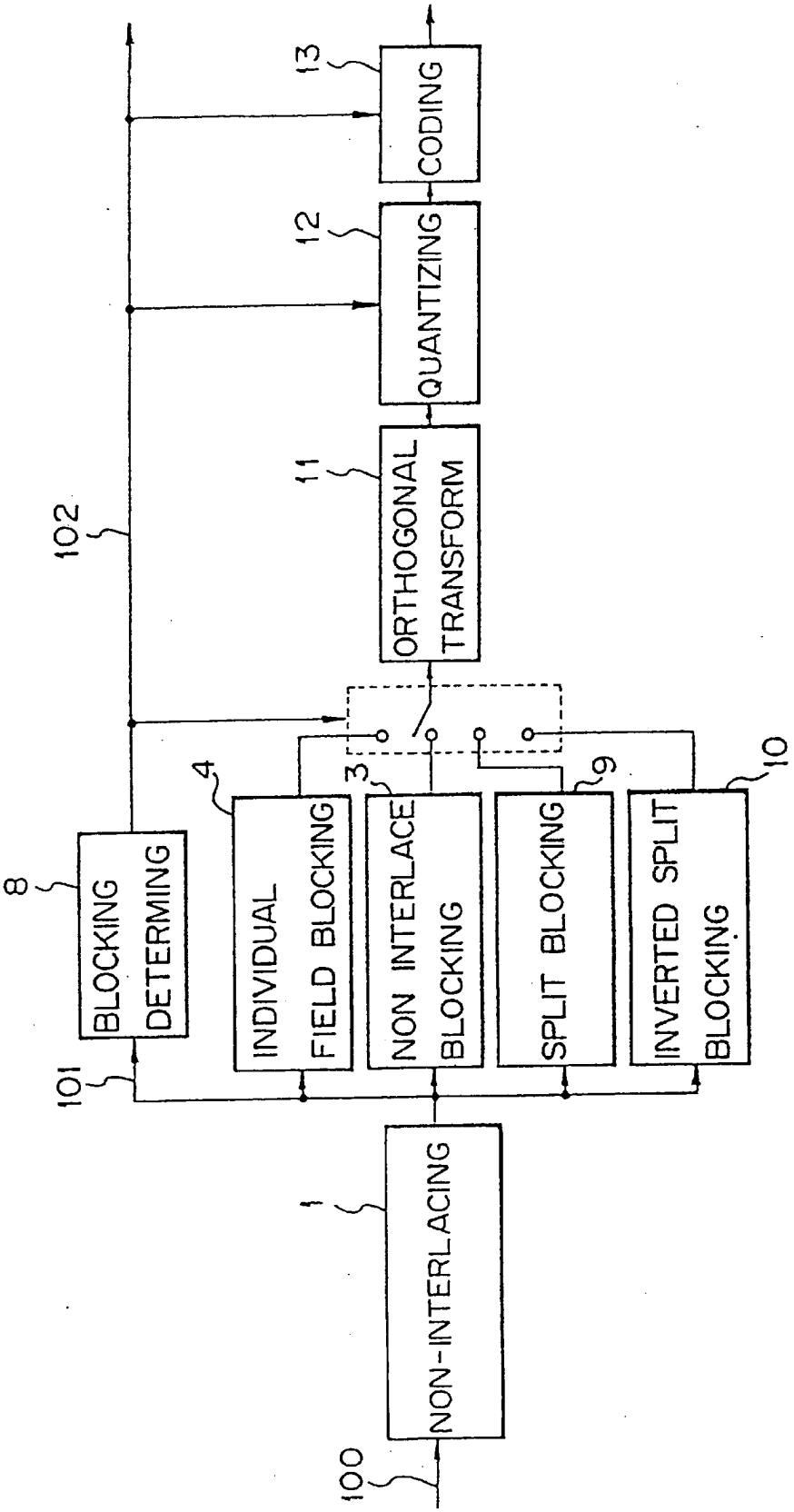


Fig. 4 (PRIOR ART)

Fig. 5


NON-INTERLACING
1
100
BLOCKING DETERMINING
8
101
INDIVIDUAL FIELD BLOCKING
4
NON INTERLACE BLOCKING
3
SPLIT BLOCKING
9
INVERTED SPLIT BLOCKING
10
102
ORTHOGONAL TRANSFORM
11
QUANTIZING
12
CODING
13

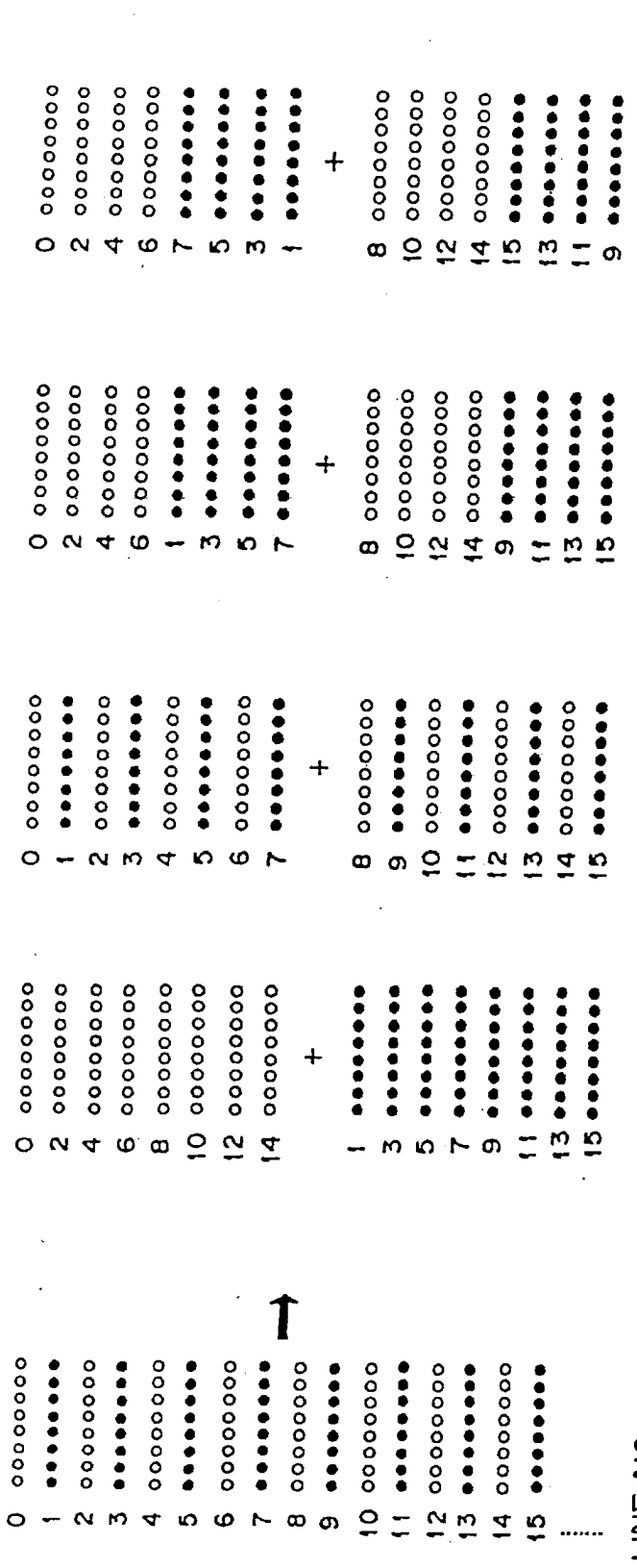


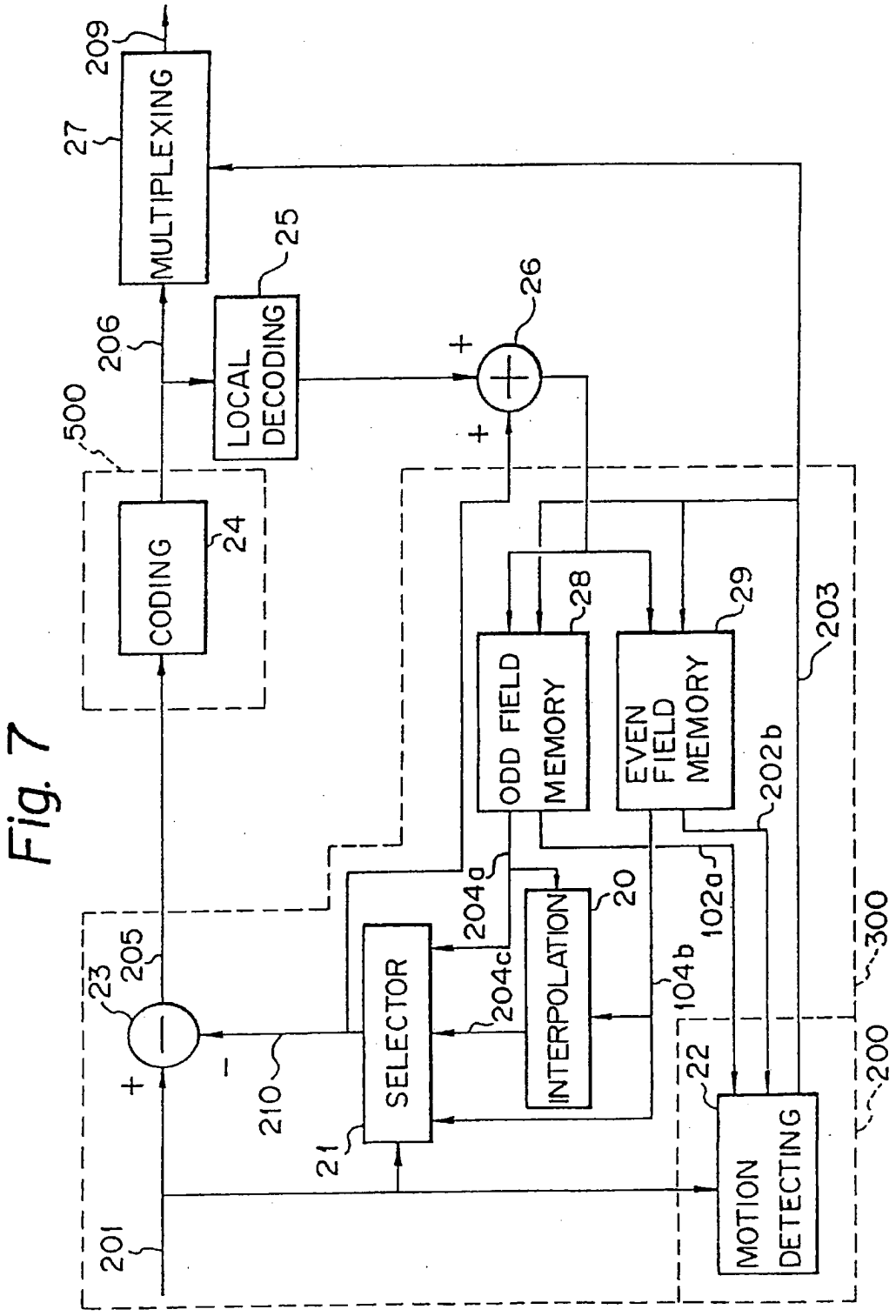
Fig. 6

Fig. 6(A)

Fig. 6(B)

Fig. 6(C)

Fig. 6(D)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MULTIPLEXING
27
25
LOCAL DECODING
26
206
500
CODING
24
28
ODD FIELD MEMORY
29
EVEN FIELD MEMORY
203
202b
204a
20
INTERPOLATION
102a
104b
204c
SELECTOR
23
205
210
21
22
MOTION DETECTING
300
200
201

Fig. 7

Fig. 8

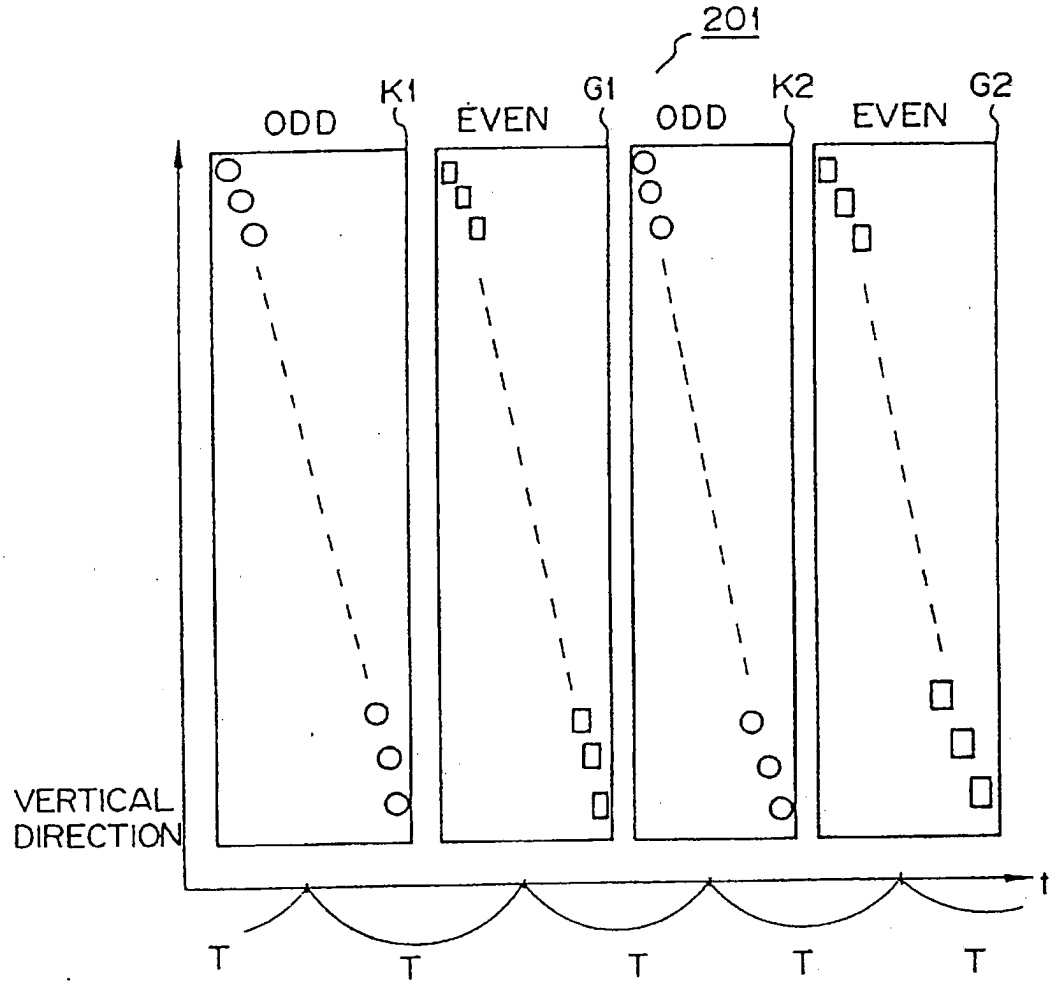
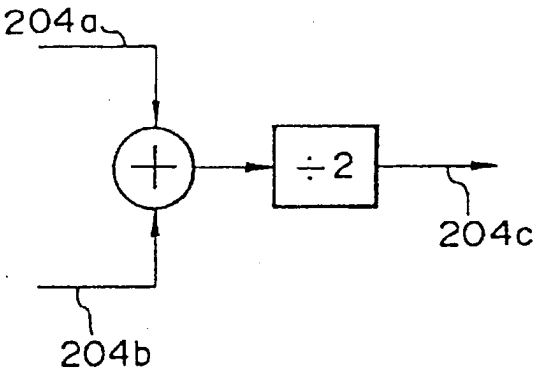


Fig. 9



INTERPOLATION SECTION

Fig. 10(A)

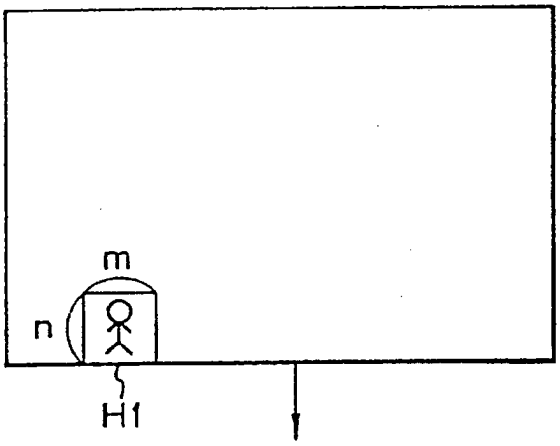


Fig. 10(B)

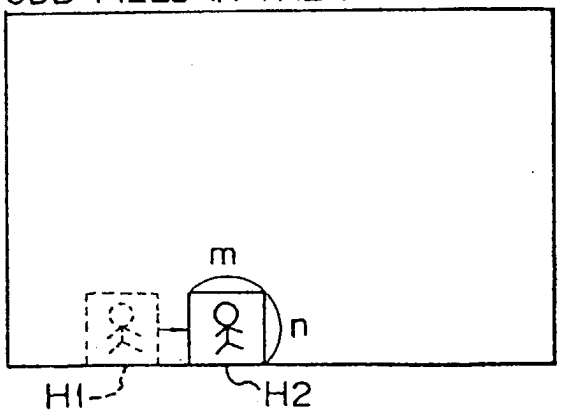
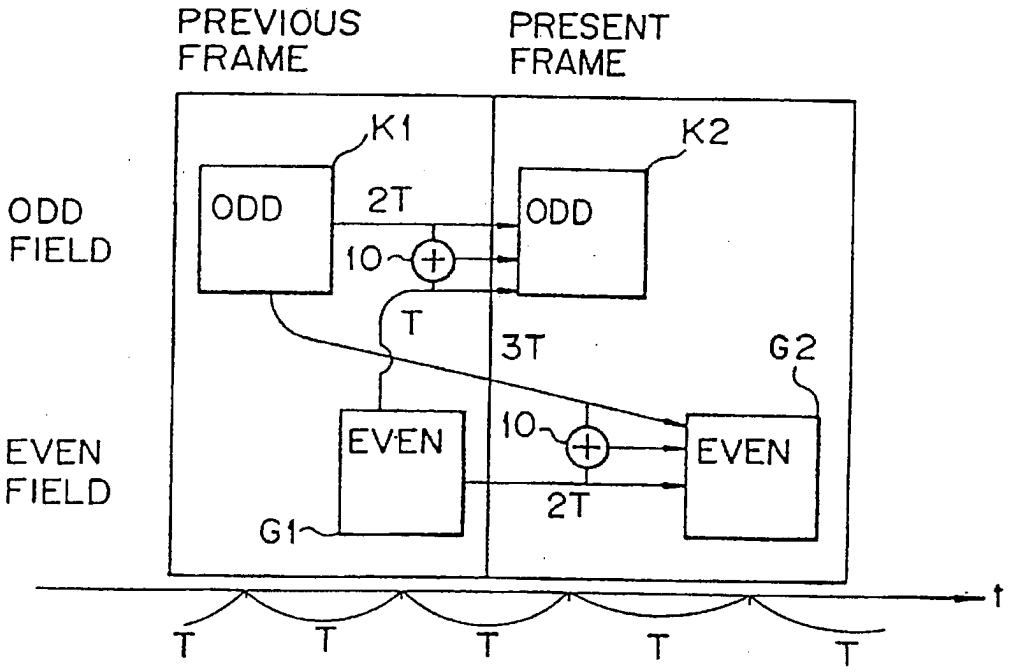


Fig. 11


PREVIOUS FRAME
PRESENT FRAME
K1
K2
ODD FIELD
ODD
2T
ODD
10
T
3T
G2
EVEN FIELD
EVEN
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EVEN
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G1
t
T
T
T
T
T

Fig. 12

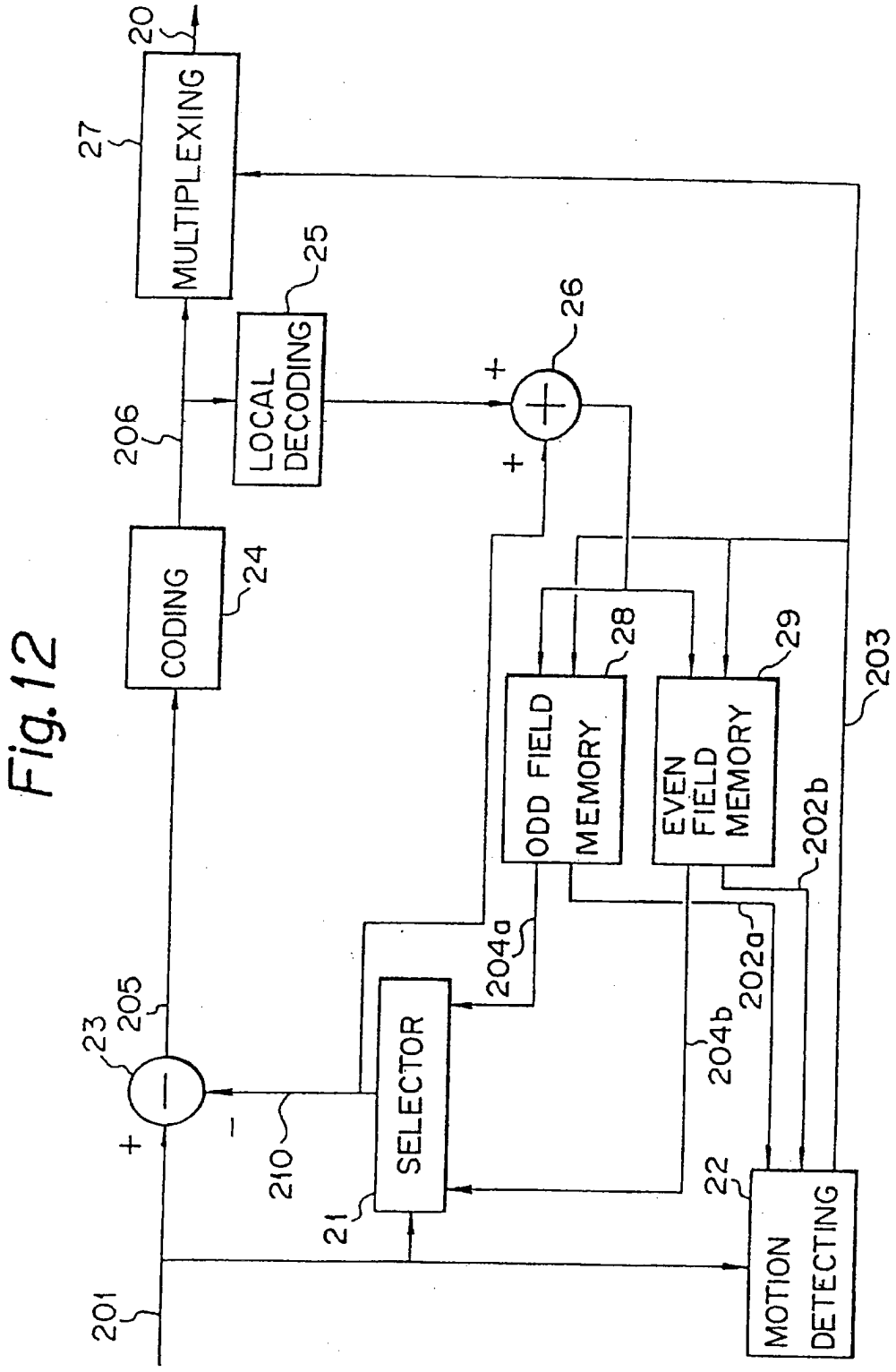
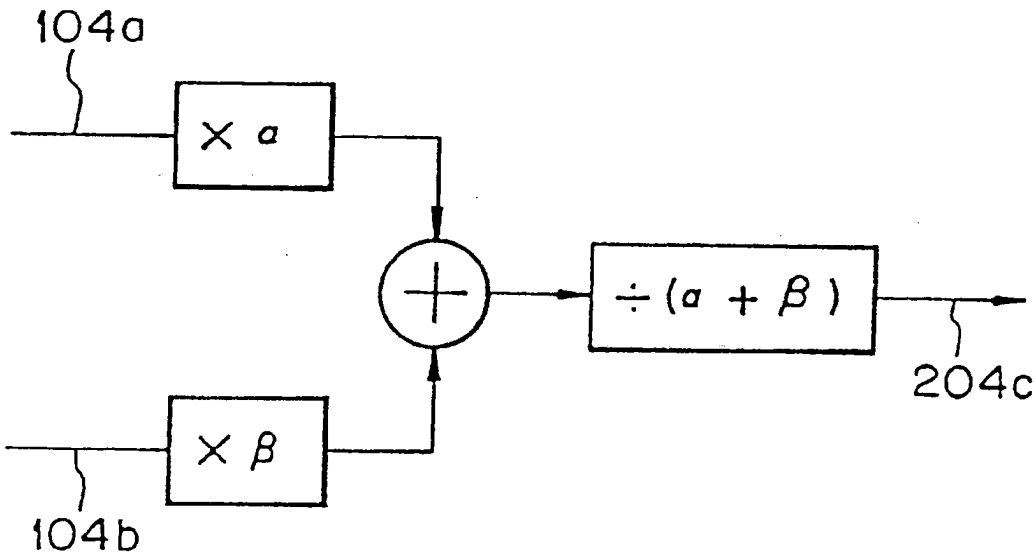

20
MULTIPLEXING
27
25
LOCAL DECODING
26
+
+
206
CODING
24
28
ODD FIELD MEMORY
29
EVEN FIELD MEMORY
203
202b
204a
202a
204b
205
23
+
−
210
SELECTOR
21
22
MOTION DETECTING
201

Fig. 13



INTERPOLATION SECTION

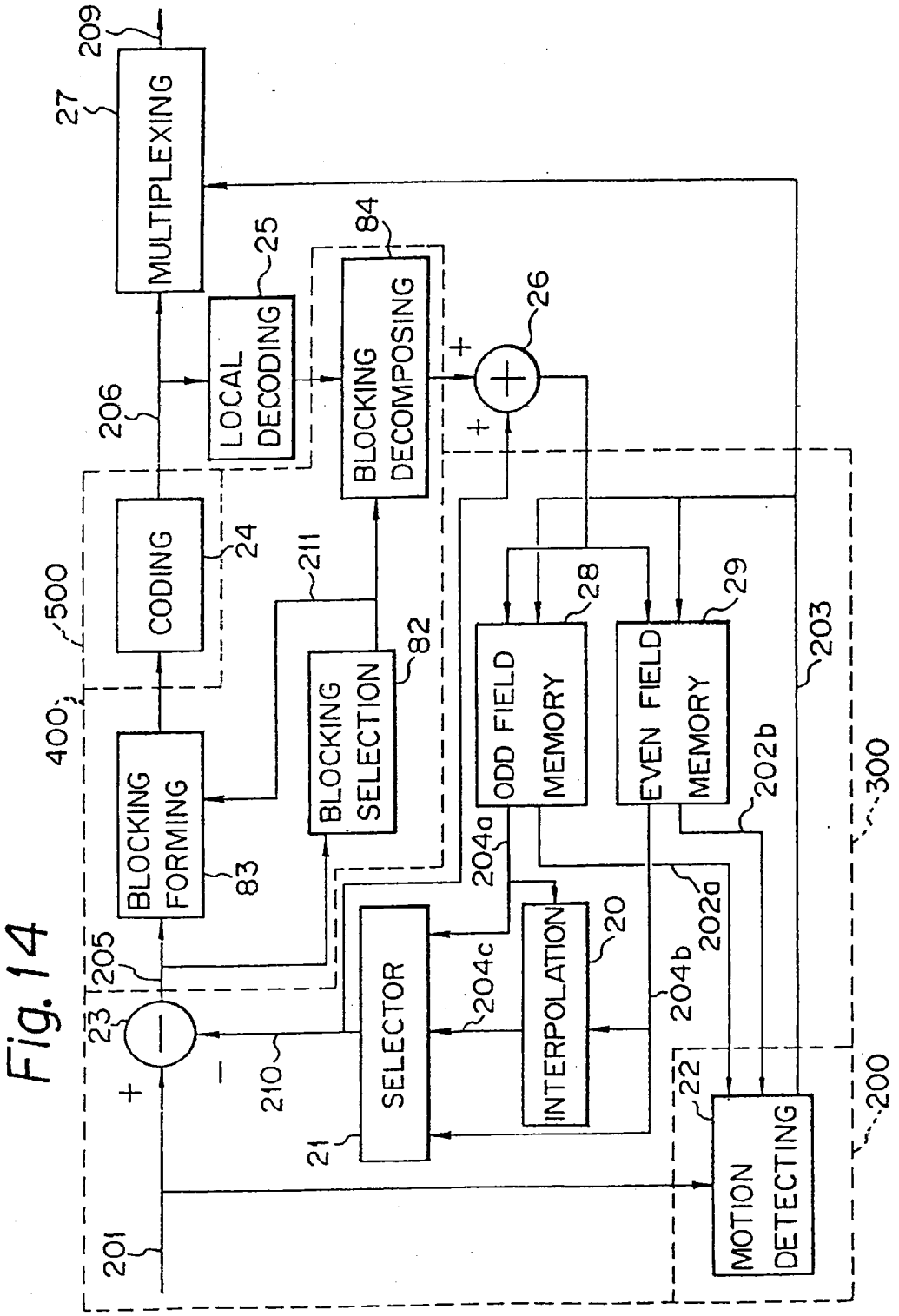

MULTIPLEXING
27
209
LOCAL DECODING
25
BLOCKING DECOMPOSING
84
26
206
CODING
24
211
500
400
BLOCKING FORMING
83
BLOCKING SELECTION
82
ODD FIELD MEMORY
28
EVEN FIELD MEMORY
29
203
202b
300
204a
202a
205
23
210
SELECTOR
204c
INTERPOLATION
20
204b
22
MOTION DETECTING
200
21
201

Fig. 14

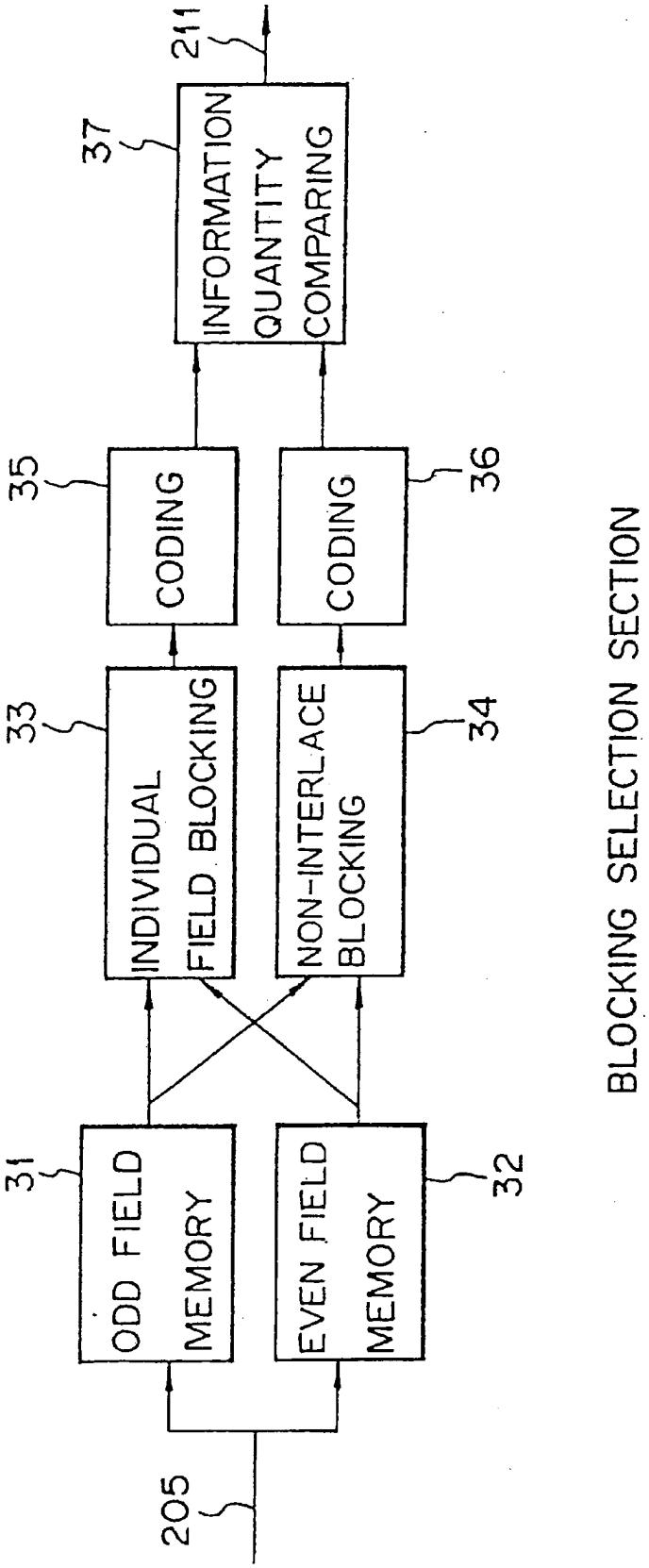

211
37
INFORMATION QUANTITY COMPARING
35
CODING
36
CODING
33
INDIVIDUAL FIELD BLOCKING
34
NON-INTERLACE BLOCKING
31
ODD FIELD MEMORY
32
EVEN FIELD MEMORY
205
BLOCKING SELECTION SECTION

Fig. 15

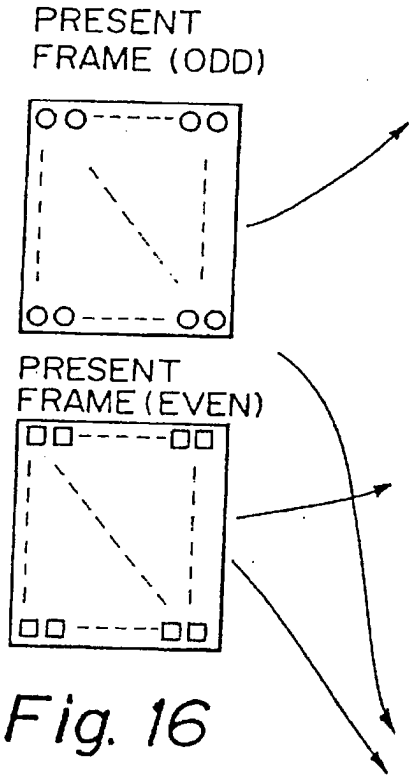


Fig. 16

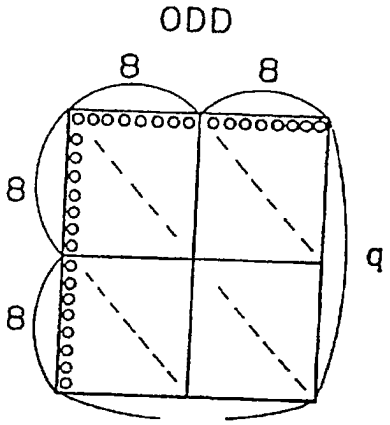


Fig. 16(A)

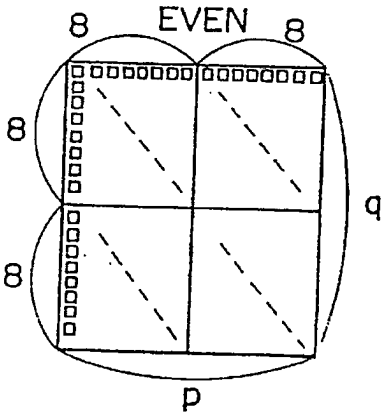


Fig. 16(B)

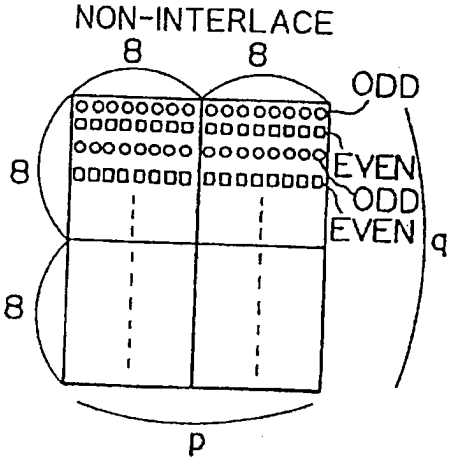
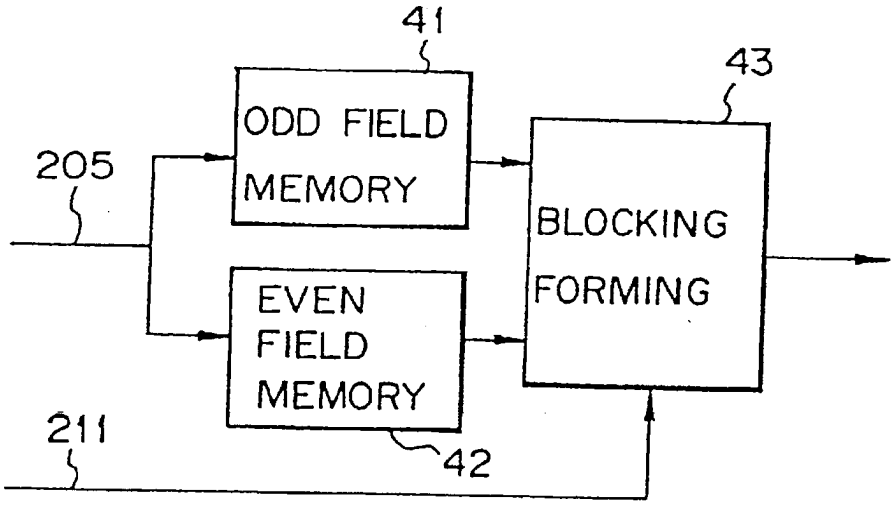


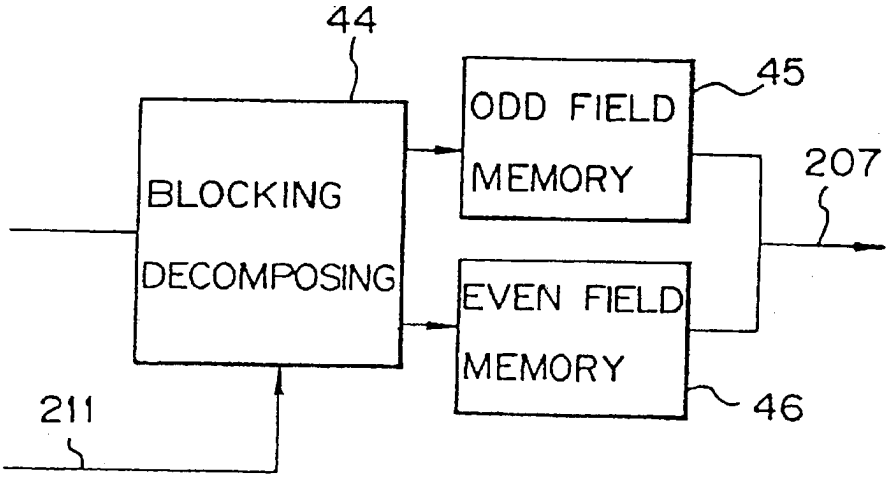
Fig. 16(C)

Fig. 17



BLOCKING FORMING SECTION

Fig. 18



BLOCKING DECOMPOSING SECTION

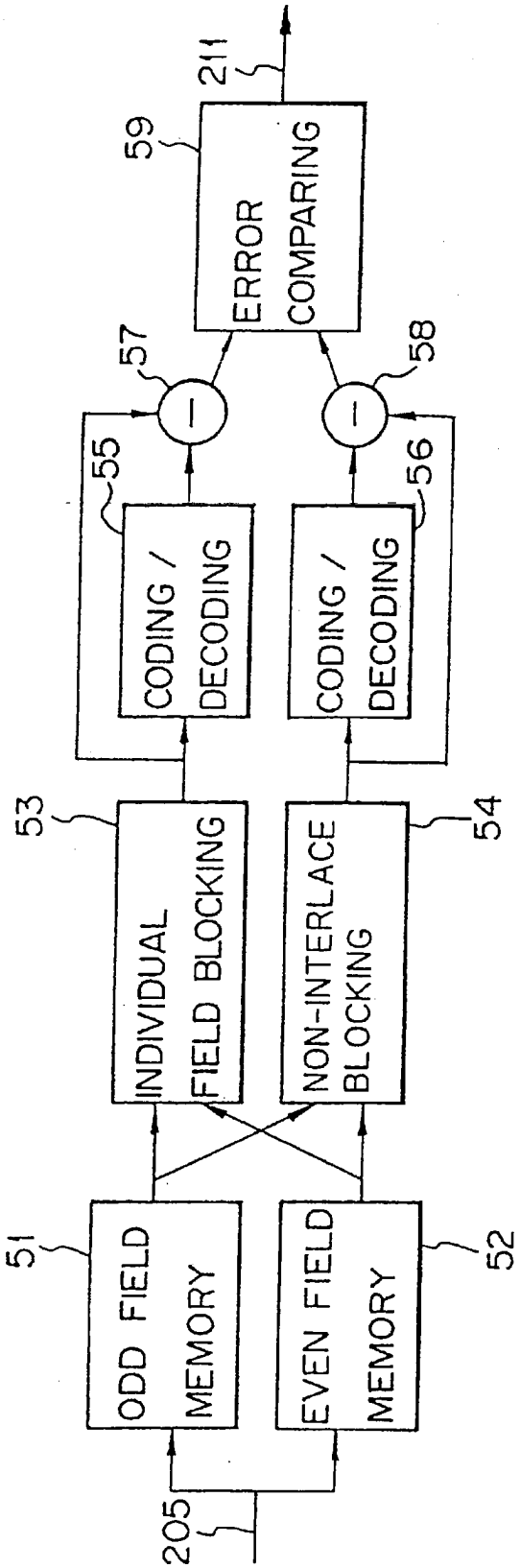
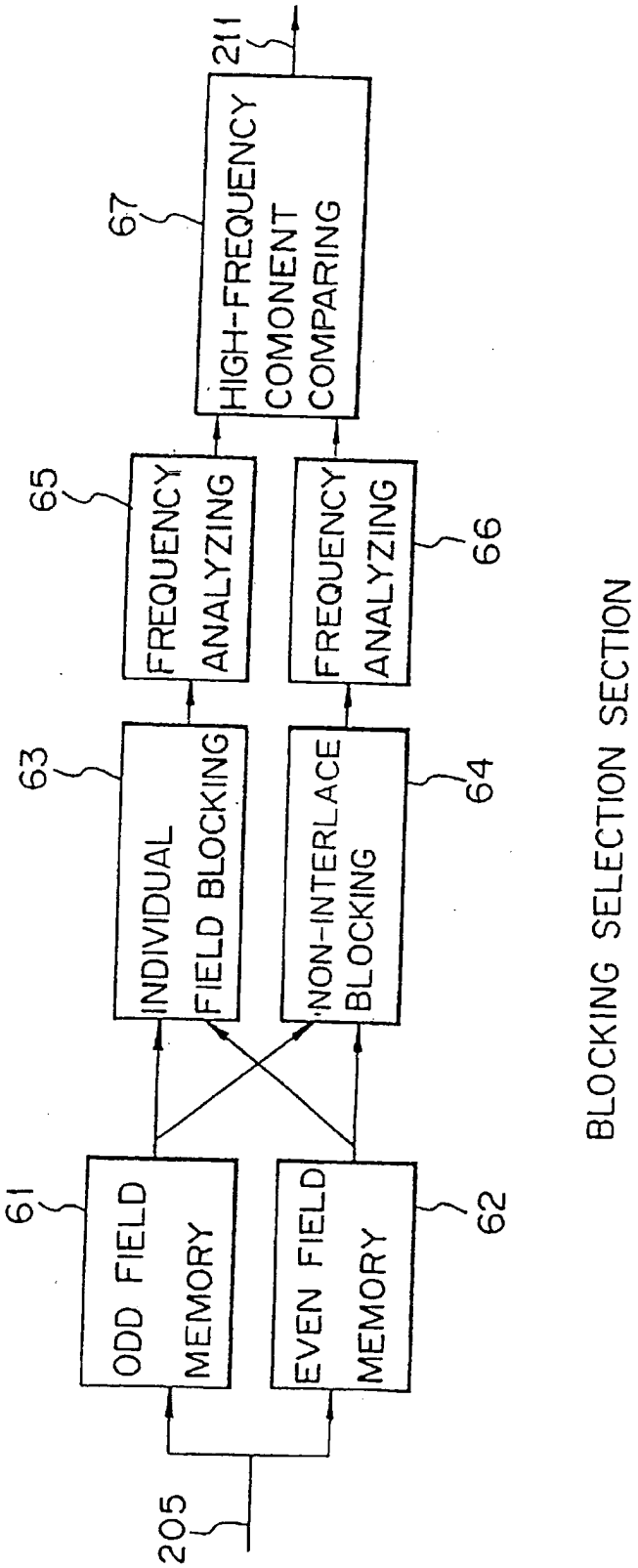

211
59
ERROR COMPARING
57
58
55
56
CODING / DECODING
CODING / DECODING
53
54
INDIVIDUAL FIELD BLOCKING
NON-INTERLACE BLOCKING
51
52
ODD FIELD MEMORY
EVEN FIELD MEMORY
205

Fig. 19

Fig. 20


211
67
HIGH-FREQUENCY COMONENT COMPARING
65
FREQUENCY ANALYZING
66
FREQUENCY ANALYZING
63
INDIVIDUAL FIELD BLOCKING
64
NON-INTERLACE BLOCKING
61
ODD FIELD MEMORY
62
EVEN FIELD MEMORY
205
BLOCKING SELECTION SECTION

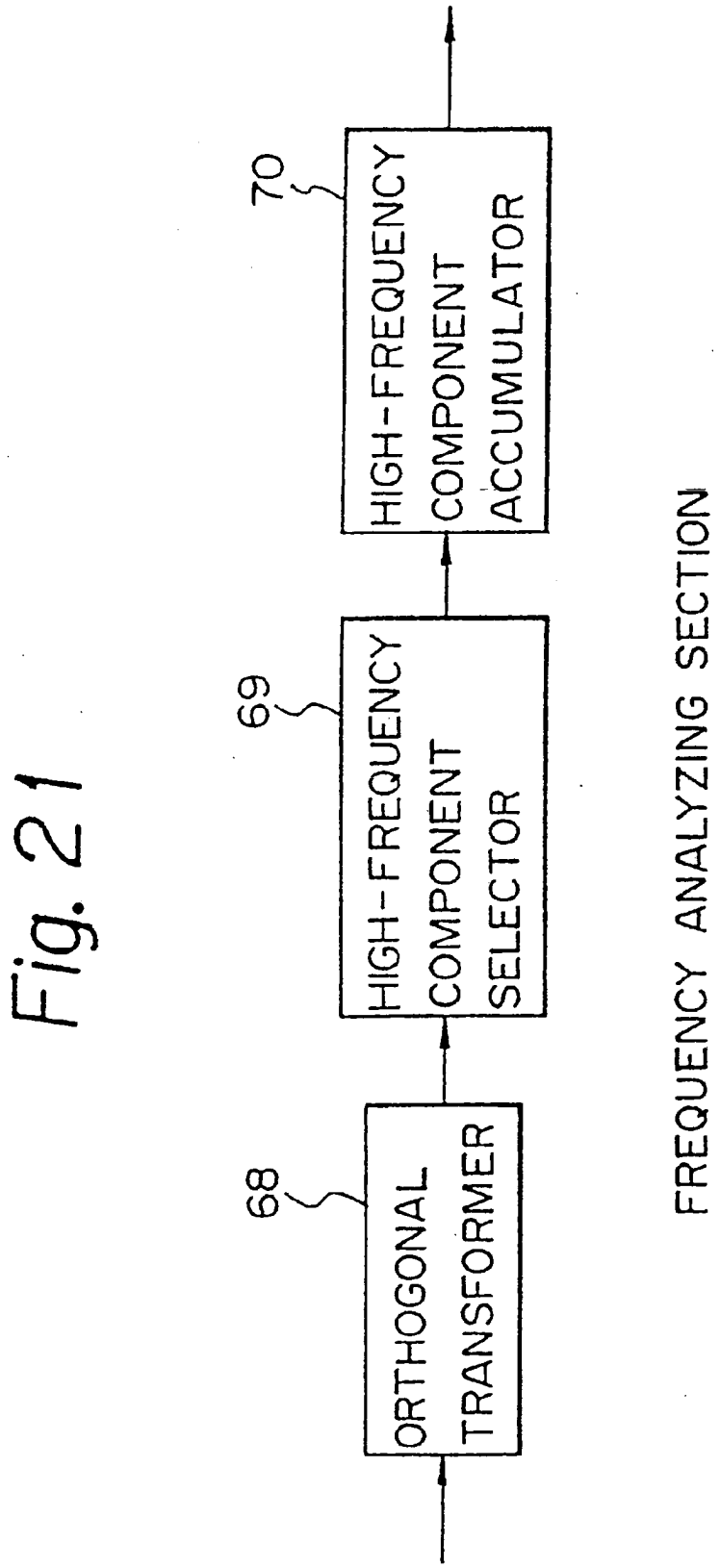
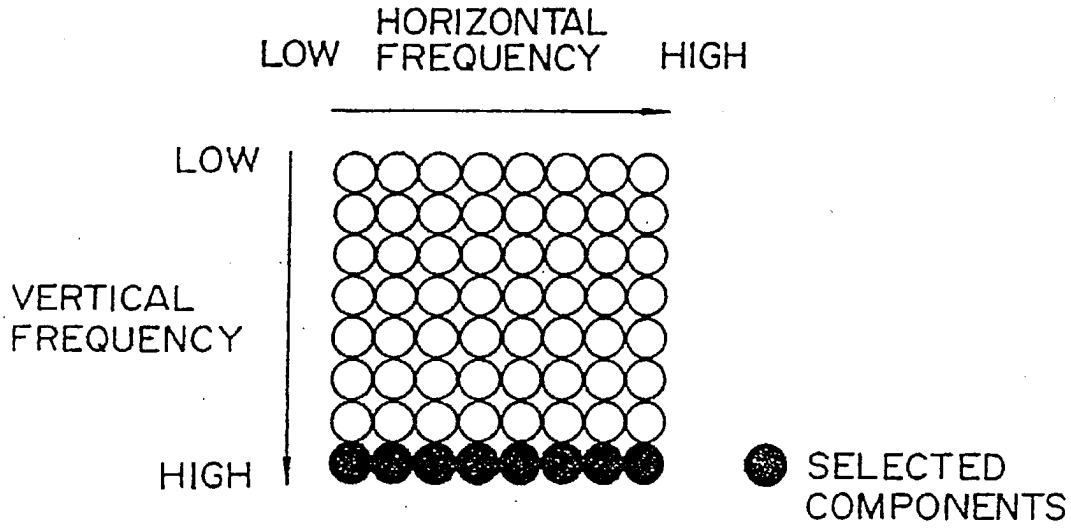

FREQUENCY ANALYZING SECTION
68
ORTHOGONAL TRANSFORMER
69
HIGH-FREQUENCY COMPONENT SELECTOR
70
HIGH-FREQUENCY COMPONENT ACCUMULATOR

Fig. 21

Fig. 22



ACCUMULATED FREQUENCY COMPONENTS

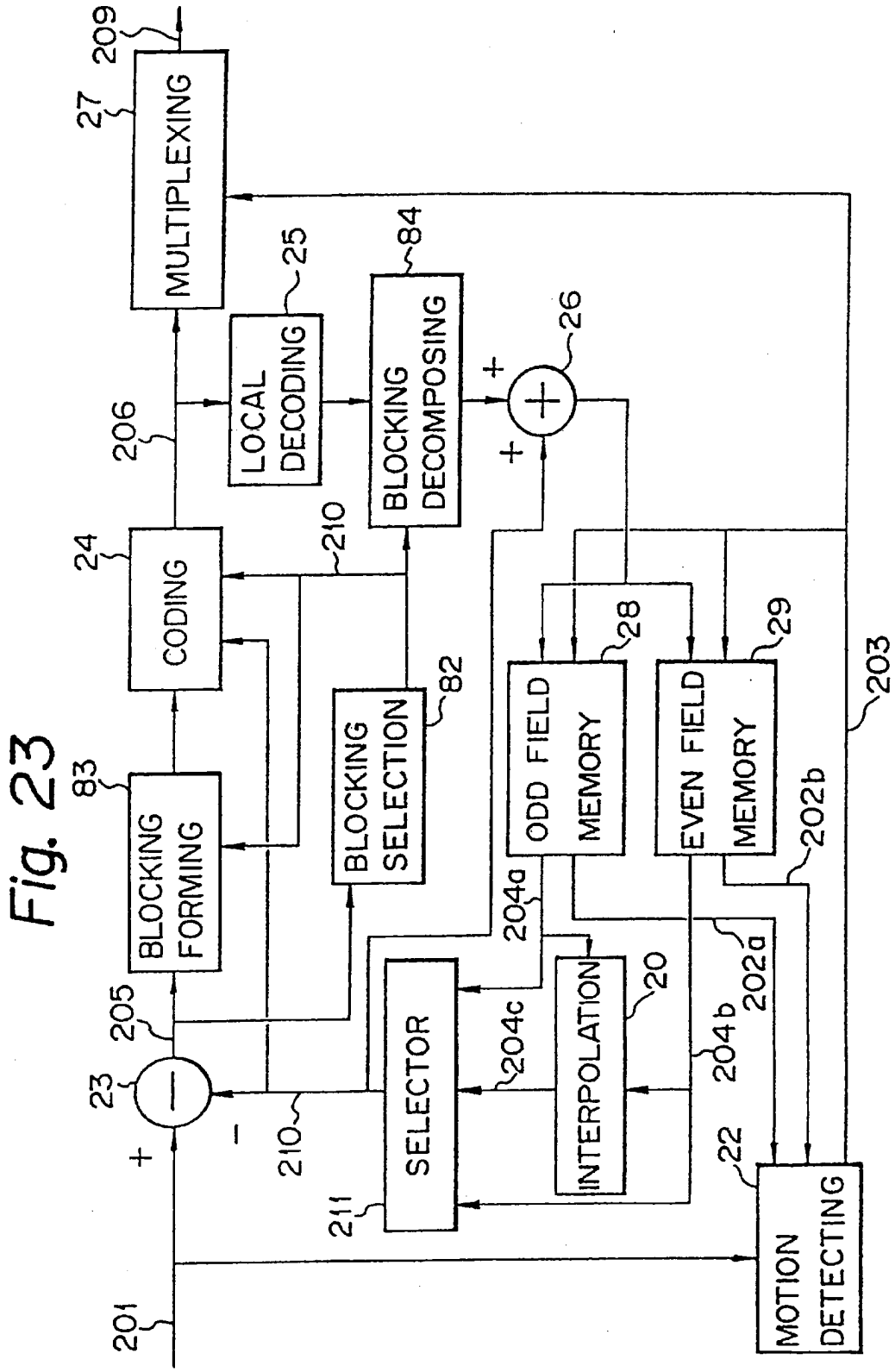

MULTIPLEXING
27
209
LOCAL DECODING
25
BLOCKING DECOMPOSING
84
26
206
CODING
24
210
BLOCKING FORMING
83
BLOCKING SELECTION
82
ODD FIELD MEMORY
28
EVEN FIELD MEMORY
29
203
202b
204a
202a
204b
204c
SELECTOR
INTERPOLATION
20
205
23
210
211
22
MOTION DETECTING
201

Fig. 23

IMAGE SIGNAL CODING SYSTEM

This application is a divisional of application Ser. No. 09/207,919, filed on Dec. 9, 1998, now U.S. Pat. No. 5,990,960, which is a divisional of application Ser. No. 08/803,235, filed on Feb. 20, 1997, now U.S. Pat. No. 5,867,220, which is a continuation of application Ser. No. 08/121,293, filed on Sep. 13, 1993, now U.S. Pat. No. 5,638,127, which is a divisional of application Ser. No. 07/962,299, filed on Oct. 16, 1992, now U.S. Pat. No. 5,274,442, the entire contents of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an image coding system for coding an image signal with high efficiency.

2. Description of the Prior Art

As is known in the art, means for eliminating redundant components included in an image signal is used for coding an image signal. A typical approach to image coding is the transform coding method wherein an image is divided into blocks, an orthogonal transform is carried out for each of the blocks, and the transform coefficients are encoded.

In the case of television signals such as an NTSC signal, interlaced scanning is used whereby an image signal of one frame is scanned twice, once in the odd field and once in the even field. The two fields scan different but complementary spaces of an image. The fields have image information at different times but there is a relatively strong correlation therebetween because the scanned lines of the two fields are alternate and adjacent. There is a technique in which coding is carried out after combining the fields and dividing them into blocks when coding an image signal produced by the interlaced scanning.

FIG. **1** is a block diagram showing the structure of an embodiment of "High Efficiency Image Coding System" described in the Japanese Patent Public Disclosure No. 1688/1991. In FIG. **1**, the coding system includes a non-interlacing section **1**, a motion detecting section **2**, a non-interlace blocking section **3**, an individual field blocking section **4**, an orthogonal transform section **5**, a quantizing section **6** for quantizing a conversion coefficient at the output of the orthogonal transform section **5**, and coding section **7**.

In operation, a series of input image signals **100**, which are produced by the interlaced scanning method and applied to each field, are converted to a non-interlaced signal **101** in the non-interlacing section **1** as indicated in FIG. **2**(C). As shown, the pixels belonging to the odd field and the pixels belonging to the even field appear alternately in every other line.

When an object is stationary and the correlation between adjacent lines is high, it is effective to use a non-interlaced signal and to code the image signal in a block including components from both fields. FIG. **3**(A) shows an example of such a condition. On the other hand, When an object is moving, the correlation between adjacent lines is lowered and it is considered to be effective to execute the coding in units of individual fields. This is because a non-interlaced signal is used for the moving object results in discontinuation as shown in FIG. **3**(B), causing a power to be generated in high frequency coefficients during the transform coding. In this case, the blocking as indicated in FIG. **3**(C) is adequate.

Thus, the motion detector **2** detects the motion of an object and changes the operation when the object is detected as being stationary by a signal **103** indicating motion, to conduct the blocking shown in FIG. **3**(A) (hereinafter, this arrangement of FIG. **3**(A) is called the non-interlace blocking) in the non-interlace blocking circuit **3**. If the object is detected to be moving, the motion detector **2** changes the operation to conduct the blocking shown in FIG. **3**(C) (hereinafter, this arrangement of FIG. **3**(C) is called the individual field blocking) in the individual field blocking circuit **4**.

The blocks obtained by changing the blocking as explained above are subjected to the discrete cosine transformation (DCT) in the orthogonal transform section **5**. The transform coefficients obtained as described above are quantized in the quantizing section **6**, and a variable length code is assigned in the coding section **7** in accordance with the occurrence probability of respective events.

Since a conventional image coding system has been structured as described above, it has been difficult to realize the blocking utilizing the correlation between fields when an object is moving. Moreover, such a system has not utilized the property of different intensities in power distribution of the coefficients after conversion caused by the difference in arrangement of pixels within the block. In addition, there is the difference in power between the stationary blocks and moving blocks, the moving blocks having a high signal power which has not been utilized.

FIG. **4** is a block diagram of another conventional inter-frame predictive coding system described, for example, in the transactions on the 3rd HDTV International Work Shop, "A Study on HDTV Signal Coding with Motion Adaptive Noise Reduction" (Vol 3, 1989). In FIG. **4**, this system comprises a frame memory **21**, a motion detecting section **22**, a subtracter **23**, a coding section **24**, a local decoding section **25**, an adder **26** and a multiplexing section **27**. Although omitted in this figure, the encoded data is decoded at a receiving side in order to reproduce the transmitted signal.

In operation, the motion of an object between the current field and the field of the same type of the preceding frame is detected block by block, the block consisting of a plurality of pixels of an input image signal **201** which is provided by the interlaced scanning method and formed of frames, each frame having both odd and even fields. The motion between odd fields is detected in the motion detecting section **22** by searching the block which has the most distinctive resemblance to the currently processing block among the already encoded blocks **202**, adjacent to the position corresponding to the currently processing block in the odd fields stored within the frame memory **21**. The degree of resemblance is evaluated by using an absolute sum of differential values or a square sum of differential values of the corresponding pixels in both blocks. The amount of motion in both horizontal and vertical directions between the current block and the block determined to be the most similar is provided as a motion vector **203**. The frame memory **21** outputs a motion compensated prediction signal **204** corresponding to this motion vector **203**.

A prediction error signal **205** obtained In the subtracter **23** by subtracting the motion compensated prediction signal **204** from the input signal **201** is applied to the coding circuit **24** in which the spatial redundancy is removed. Since low frequency components of an image signal generally occupy a greater part of the power thereof, information can be compressed by quantizing high power portions with a large number of bits and quantizing low power portions with a small number of bits. According to an example of this

information compression method, the frequency conversion is carried out for an 8×8 pixels block by conducting an orthogonal transform such as a discrete cosine transform to scalar-quantized the transform coefficients. The scalar-quantized coding data **206** is sent to the local decoding section **25** and to the multiplexing section **27**. The multiplexing section **27** conducts multiplexing and encoding for the coding data **206** and the motion vector **203** to output these signals to a transmission line **209**.

Meanwhile, the local decoding circuit **25** executes the inverse operation of the operation in the coding section **24**, namely the inverse scalar quantization and inverse orthogonal transform to obtain a decoded error signal **207**. The motion compensated prediction signal **204** is added to the decoded error signal **207** in the adder **26** and stored in the frame memory **21** to detect motion of the odd field of the next frame.

In addition, the motion of the even fields of the input image signal **201** with respect to the alread encoded field of the frame memory **21** is also detected for the coding of the motion compensated prediction error signal. As described above, in the conventional interframe predictive coding system, redundancy with respect to time included in moving image signals is removed by the motion compensated prediction coding and redundancy with respect to space is removed by the orthogonal transform.

Since the conventional interframe predictive coding system is structured to individually encode both the odd field and even field by predicting the current (present) odd field from the odd field of the already encoded frame and predicting the current even field from the even field of the already encoded frame, the encoding efficiency is low because the spatial correlation existing between the continuous fields, produced by the interlaced scanning method, is not used.

SUMMARY OF THE INVENTION

The present invention has been proposed to overcome the problems in the prior art. Therefore it is an object of the present invention not only to adaptively discriminate between a block which is effective for non-interlace blocking and a block which is effective for individual field blocking, but also to enhance coding efficiency by adding a class of blocking so that field correlation is used even for a moving image, the quantization accuracy is controlled and the scanning sequence of transform coeffecients is changed in accordance with switching of the blocking.

It is another object of the present invention to provide a coding system for searching motion from both odd and even fields of the frame which is already encoded in order to predict each present field.

It is a further object of the present invention to provide a coding system for enabling highly efficient coding by realizing blocking for adaptively switching the field and frame in the block coding of prediction errors.

According to the first aspect of the present invention, an adaptive blocking image coding system encodes an input image signal obtained by interlaced scanning in a unit of the block of M pixels×N lines. More specifically, the adaptive blocking image coding system comprises blocking means for selectively forming a first type block including only the pixels of M pixels×N lines belonging to the odd field of the input image signal or the pixels of M pixels×N lines belonging to the even field thereof, a second type block wherein the pixels of the M pixels×N/2 lines belonging to the odd field and the pixels of the N/2 lines belonging to the even field are arranged alternately in every other line corresponding to scanning positions on a display screen, a third type block wherein the pixels of M pixels×N/2 lines belonging to the odd field are arranged in the upper or lower half of the block and the pixels of M pixels×N/2 lines belonging to the even field are arranged in the remaining half of the block, and a fourth type block wherein the pixels of M pixels×N/2 lines belonging to the odd field are arranged in the upper or lower half of the block, the pixels of M pixels×N/2 lines belonging to the even field are arranged in the remaining half of the block and the pixels of either field are inverted upside down in the vertical direction with respect to the display screen. The system further includes blocking determining means for determining the type of blocking by the blocking means, a transform means for orthogonally transforming the block formed by the blocking means, quantizing means for quantizing the transform coefficient obtained by the transform means, and coding means for encoding the quantized index obtained by the quantizing means.

With the structure described above, the block of the M pixels×N lines if obtained by one blocking selected from the non-interlace blocking where the pixels of M pixels×N/2 lines belonging to the odd field and the pixels of M pixels×N/2 lines belonging to the even field are arranged in every other line corresponding to the scanning positions on the display screen, an arrangement (hereinafter, called split blocking) where the pixels of M pixels×N/2 lines belonging to the odd number field are arranged in the upper half or lower half block and the pixels of M pixels×N/2 lines belonging to the even field are arranged in the remaining half block, and an arrangement (hereinafter, called inverted split blocking) where the pixels of M pixels×N/2 lines belonging to the odd field are arranged in the upper or lower half block, the pixels of M pixels×N/2 lines belonging to the even field are arranged in the remaining half block and the pixels of either field are inverted in the vertical direction With respect to the display screen. The obtained block is orthogonally transformed the transform coefficients are quantized, and then the quantization index is encoded.

According to the second aspect of the present invention, the quantizing means for quantizing the transform coefficient in the adaptive blocking image coding system variably controls the quantization accuracy in accordance with the type of arrangement blocking-processed by the blocking means.

More specifically, one of the arrangements including individual field blocking, non-interlace blocking, split blocking, or inverted split blocking is orthogonally transformed, the transform coefficient is quantized and the quantizing index is encoded with the quantizing accuracy in accordance with the information, indicating the selected blocking.

According to the third aspect of the present invention, the coding means for encoding the quantizing index produced when quantizing the transform coefficient in the adaptive blocking image coding system determines the scanning sequence (path) for quantizing the transform coefficient in accordance with the type of arrangement to be blocking-processed by the blocking means.

More specifically, one of the arrangements to be blocking-processed by the individual field blocking, non-interlace blocking, split blocking, or inverted split blocking is orthogonally transformed, the transform coefficient is quantized, and the quantizing index is encoded with the quantization accuracy and the scanning sequence in accordance with the information indicating the selected blocking.

According to the fourth aspect of the present invention, the adaptive blocking image coding system comprises blocking determining means for selecting the type of arrangement to be blocking-processed in accordance with the value obtained by multiplying a predetermined weighting coefficient with the pixels of each line included in the block and then totaling such multiplied values.

More particularly, one of the arrangements to be blocking-processed by individual field blocking, non-interlace blocking, split blocking, or inverted split blocking is selected by the value obtained by multiplying the predetermined weighting coefficient with the pixels of each line included in the block and then totaling such multiplied values. The selected block is orthogonally transformed, the transform coefficient is quantized and the quantizing index is encoded.

According to the fifth aspect of the present invention, the adaptive blocking image coding system also comprises a blocking determining means for selecting the type of arrangement which has the minimum coefficient power of a predetermined high frequency component among the transform coefficients obtained by discrete cosine transform of the block.

In other words, one of the arrangements to be blocking-processed by individual field blocking, non-interlace blocking, split blocking, or inverted split blocking is selected in such a manner that the coefficient power of the predetermined high frequency element component is the minimum among the transform coefficients obtained t)y discrete cosine transform of the block. The determined block is orthogonally transformed, the transform coefficient is quantized, and the quantizing index is encoded.

According to the sixth aspect of the present invention, there is provided a coding system which individually searches the motion from both odd and even fields of the already encoded frame in order to predict tile field to be encoded, the system comprising the following elements:

(a) input means for inputting an input signal to be encoded;

(b) a field memory for storing signals based on the input signal by dividing it into a plurality of fields such as the odd field and even field;

(c) predictive signal output means for outputting predictive signals of a plurality of types predicting the change of input signal on the basis of signal stored in the field memory;

(d) a selector for selecting a predictive signal from the predictive signals provided by the predictive signal output means; and

(e) coding means for encoding the input signal using the relationship between the predictive signal selected by the selector and the input signal from the input means.

With such an arrangement, the coding system can provide stabilized prediction efficiency regardless of motion of an object by making reference to both fields of the already encoded frame for the purpose of prediction.

According to the seventh aspect of the present invention, the coding system is structured to realize adaptive prediction from the searched two kinds of motion compensated predictive signals and a plurality of predictive signals combining interpolation signals of these motion compensated predictive signals.

Since the coding system as constructed utilizes a predictive signal produced by interpolating the predictive signals from both fields of the already encoded frame, motion at the intermediate point of time and space of the two fields used for the prediction can be considered. Moreover, this coding system also functions as a low-pass filter, whereby the prediction efficiency can be improved and the encoded image is stabilized.

According to the eighth aspect of the present invention, the coding system executes the encoding, for example encoding prediction error signals, by adaptively switching the encoding operation from blocking of the pixels of only the odd field or even field of the frame for encodement to blocking of both odd and even fields for encodement, the system comprising the following elements:

(a) input means for inputting an input signal to be encoded by dividing into a plurality of fields such as an odd field and even field;

(b) a blocking selection section for selecting, at the time of blocking and encoding the signal from the input means, a block suitable for the encoding between the block consisting of the signal of only one kind of field and the block consisting of the signal combining signals of a plurality of fields;

(c) a block forming section for forming a block selected by the blocking selection section; and

(d) coding means for encoding a block formed by the block forming section.

The coding system having such a structure provides high efficiency encoding by selecting the blocking method most suitable for the encoding, i.e., blocking the pixels of only either of the odd field or even field, or blocking the pixels of both odd and even fields.

According to the ninth aspect of the present invention, the coding system also comprises a concrete selecting means for adaptively switching the block selection. This selecting means includes any one of the following selecting mans:

(a) selecting means for selecting the block with the least amount of encoding information from a plurality kinds of block;

(b) selecting means for selecting the block with the least amount of encoding errors from a plurality kinds of block; and

(c) selecting means for selecting the block with the least amount of high-frequency components in the signal to be encoded from a plurality kinds of block.

The coding system having such a structure enables adaptive switching of the blocking by selecting the blocking with less encoding information, the blocking with less encoding errors, or the blocking with less high frequency components included in the signal to be encoded, from the blocking of the pixels of one of only the odd or even field or the blocking of the pixels of both odd and even fields.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be more fully understood from the following detailed description and the accompanying drawings in which:

FIG. **1** is a block diagram of an image coding system in the prior art;

FIG. **2** is a diagram for explaining non-interlace blocking;

FIG. **3** is a diagram for explaining an adaptive blocking of the prior art;

FIG. **4** is a block diagram showing the structure of another coding system of the prior art;

FIG. **5** is a block diagram of an embodiment of the present invention;

FIG. **6** is a diagram for explaining adaptive blocking in the embodiment shown in FIG. **5**;

FIG. 7 is a block diagram showing the structure of an adaptive field/frame coding system of another embodiment of the present invention;

FIG. 8 is a diagram showing an exemplary input image signal;

FIG. 9 is a block diagram showing an example of the structure of an interpolating section shown in FIG. 7;

FIG. 10 is a diagram for explaining the operation of a motion detecting circuit

FIG. 11 is a diagram for explaining the operation for using a motion compensated predictive signal in the embodiment shown in FIG. 7;

FIG. 12 is a block diagram showing the structure of an adaptive field/frame coding system according to another embodiment of the present invention;

FIG. 13 is a block diagram showing another example of the interpolating section;

FIG. 14 is a block diagram showing an adaptive field/frame coding system according to embodiment of the present invention:

FIG. 15 is a block diagram showing an example of the structure of the blocking selection section;

FIG. 16 is a diagram showing a structural example of the block selected by the blocking selecting section;

FIG. 17 is a block diagram showing a structural example of the blocking forming section;

FIG. 18 is a block diagram showing a structural example of the blocking decomposing section;

FIG. 19 is a block diagram showing another structural example of the blocking selecting section;

FIG. 20 is a block diagram showing another structural example of the blocking selecting section;

FIG. 21 is a block diagram showing a structural example of the frequency analyzing section;

FIG. 22 is a diagram showing an example of the accumulated frequency components; and

FIG. 23 is a block diagram showing another structural example of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. **5**, an embodiment of the present invention is shown as an adaptive blocking image coding system. In FIG. **5**, the image coding system comprises a non-interlacing section **1** for conducting non-interlace processing; a blocking determination section **8**; an individual field blocking section **4**; a non-interlace blocking section **3**; a split blocking section **9**; an inverted split blocking section **10**; an orthogonal transform section **11**; a quantizing section **12** and coding section **13**. Such various types of blocking are shown in FIG. **6**. FIGS. **6A–6D** show individual field blocking non-interlace blocking, split blocking and inverted split blocking, respectively.

The operation will be explained with reference to FIG. **5** and FIGS. **6A–6D**. The input image signal series **100** which is scanned by the interlace scanning method and is inputted field by field is converted into a non-interlaced signal **101** in the non-interlace section **1**.

FIG. **2** shows a profile of non-interlace processing in the prior art similar to the non-interlace processing in the present invention. When (A) is defined as an input image signal from the odd field and (B) as an input image signal of the even field, the non-interlaced signal **101** shown in (C), alternately combining the lines from respective fields, can be obtained.

The individual field blocking section **4** executes, as shown in FIG. **6**(A), blocking in which the fields are processed individually. This blocking is effective when the correlation between the fields is not available because of quick motion.

The non-interlace blocking section **3** executes the blocking shown in FIG. **6**(B). In the case of a stationary or still image, a continuous image can be obtained by non-interlaced processing of the fields. The wavelength of the signal thereby becomes substantially longer, resulting in power being concentrated on low frequency components in the successive transform coding.

The split blocking section **9** conducts the blocking as shown in FIG. **6**(C). This blocking is effective in the case where the correlation between the fields exists but the fields are noncontinuous when non-interlace blocking is carried out.

The inverted split blocking section **10** conducts the blocking shown in FIG. **6**(D). This blocking is also effective in the case where the correlation between fields exists but the fields are noncontinuous when non-interlace blocking is carried out. This blocking prevents discontinuation at the center of the block when the split blocking method is used.

The blocking determinating section **8** determines the optimum blocking from a plurality of blockings as explained above and outputs a blocking arrangement selecting signal **102** for selecting the determined blocking. Here, it is important to enhance the concentration of power, on the low frequency coefficients in the transform coding. For this purpose, it is effective to evaluate the amplitude of high frequency components in each blocking and select the blocking having the minimum amplitude.

In one of the evaluation methods, a weight is multiplied with the pixels of each line and the obtained values are then totaled. For example, the weight of +1 is given to the lines 0, 2, 4, 6 using the line numbers shown in FIG. **6**, and the weight of −1 is given to the lines 1, 3, 5, 7. Thereafter, the obtained values are totaled to obtain the absolute value of the sum. Moreover, the weight +1 is given to the lines 8, 10, 12, 14, and the weight −1 is given to the lines 9, 11, 13, 15. The obtained values are then totaled to also obtain the absolute values of the sum. Both absolute values are totaled. Thus, the weighting is inverted alternately for respective lines and it is equivalent to the evaluation of the maximum frequency component when non-interlace blocking has been conducted.

Further, the weight +1 is given to the lines 0, 4, 8, 12 and the weight −1 to the lines 2, 6, 10, 14. The obtained values are totaled to obtain the absolute value of the sum. In addition, the weight +1 is given to the lines 1, 5, 9, 13 and the weight −1 to the lines 3, 7, 11, 15. The obtained values are then totaled to obtain the absolute value of the sum. These absolute values are also totaled to evaluate the maximum frequency component of the individual field blocking.

In addition, the weight +1 is given to the lines 0, 4, 1, 5 and the weight −1 to the lines 2, 6, 3, 7. The obtained values are totaled to obtain the absolute value of the sum. The weight +1 is also given to the lines 8, 12, 9, 13 and the weight −1 to the lines 10, 14, 11, 15. The obtained values are totaled to obtain the absolute value of the sum. Both absolute values are then totaled to evaluate the maximum frequency component of the split blocking.

The weight +1 is given to the lines 0, 4, 7, 3 and the weight −1 to the lines 2, 6, 5, 1. The obtained values are totaled to obtain the absolute value of the sum. Moreover, the weight +1 is given to the lines 8, 12, 15, 11 and the weight −1 to the lines 10, 14, 13, 9. The obtained values are

totaled to obtain the absolute value of the sum. These absolute values are totaled to evaluate the maximum frequency component of the inverted split blocking.

In another method for evaluation of each blocking, the number of orthogonal transformed coefficients having an amplitude larger than a predetermined threshold value for the respective blockings is counted, and the blocking having the minimum number is selected.

The orthogonal transform section **11** carried out the orthogonal transform of the selected block to obtain the transform coefficients. The obtained transform coefficients are quantized in a fixed sequence by the quantizing section **12**. In this case, some difference lies in the power of the coefficients depending on the type of blocking. In general, non-interlace blocking tends to be selected for a stationary region and the power is comparatively small.

Meanwhile, since the correlation between fields becomes small in a quick motion area, individual field blocking is often selected and the power is large. Moreover, split blocking and inverted split blocking are considered to be intermediate to the above two blockings. Therefore, efficiency can be improved by variably controlling quantization accuracy in accordance with the type of blocking.

The quantizing accuracy can also be controlled variably in accordance with not only the type of blocking but also the combination of actual signal power and quantization error power. In this case, it is also possible to execute variable length coding by combining the information indicating type of blocking and the information indicating quantization accuracy.

Indexes obtained by quantizing the coefficients are encoded in the coding section **13**. In this case, the coefficients are scanned from those having a larger coefficient power to those having a smaller one in order to enhance the efficiency of encoding. For the coefficients having a poster lower than a certain specified value, the encoding may cease. Therefore, it is very convenient if the power distribution can be anticipated. There is a tendency with respect to the distribution of power of the coefficients that the power is increased as the frequency is lower. However, if the blocking is adaptively changing, as in the present invention, the coefficients having lower power do not always correspond to low frequency components. Then, the coding efficiency can be improved by changing the scanning sequence or path in accordance with the type of blocking.

Since the present invention is structured as explained above, the following effects can be obtained.

The coding efficiency of transform coding is improved by switching the blocking of an image signal scanned by the interlaced scanning method into an adapted blocking. Moreover, the efficient assignment of information quantity can be realized by variably controlling the quantizing accuracy of transform coefficients correspondingly to the switching of the blocking. In addition, the encoding efficiency can also be improved in transform coding by changing the scanning sequence of the transform coefficients within the block.

Referring now to FIG. **7**, a structural diagram of an adaptive field/frame coding system according to another embodiment of the present invention is shown. The system includes an odd field memory **28** for storing local decoded signals of odd fields, an even field memory **29** for storing local decoded signals of even fields, an interpolation section **20** for interpolating a predictive signal with motion compensated from the two fields, and a selector **21** for selecting a predictive signal which gives the optimum prediction from three signals of the signals predicted from the odd and even fields and the interpolated predictive signal. In FIG. **7**, sections **200**, **300** and **500** enclosed by a broken line respectively denote motion detecting means, predicting error signal output means and coding means.

FIG. **8** shows a profile of input image signals **201** which are scanned by the interlaced scanning method, wherein the odd and even fields are alternately applied. FIGS. **8** shows the fields in the coordinates where time is plotted on the horizontal axis and vertical direction on the vertical axis. In FIG. **8**, K1 indicates an odd field of the first frame, while G1, an even field of the first frame. In the same manner, K2 is an odd field of the second frame, while G2, an even field of the second frame.

FIG. **9** is a block diagram of an example of the interpolating section **20**. A simple arithmetic mean of the motion compensated prediction signal **204***a* from the inputted odd fields and the motion compensated prediction signal **204***b* from the inputted even fields is obtained and is used as an interpolation predictive signal **204***c*.

The operation will be explained with reference to FIGS. **7**, **8** and **9**. Motion of the odd fields and even fields of the present frame in relation to the preceding frame is detected in units of blocks including pixels (n×m) in response to the input image signal **201** which is scanned by the interlace scanning method and includes the odd and even fields alternately. The motion of the odd fields between the present and the preceding frames is detected by searching, in the motion detecting section **22**, the block which most resembles the currently processed block in the image signal **201** from the blocks adjacent **202***a* to the position corresponding to the currently encoded object in the already encoded odd fields stored within the odd field memory **28**.

As shown in FIG. **10**, for example, it is assumed that image H1 exists within one block unit (n×m) in the preceding frame, and the image moves to position H2 from position H1 in the present input image signal. The motion detecting section **22** outputs a motion vector **203** which indicates the block has moved horizontally to **112** from H1. In this case, since motion is not detected in the vertical direction, the motion vector **203** has the value of 0 with regard to vertical direction. The motion in the horizontal and vertical directions thus obtained is outputted as the motion vector **203**.

The odd field memory **28** outputs a motion compensated prediction signal **204***a* corresponding to this motion vector **203**. Similarly, compensation for motion of the even fields in the preceding frame is carried out in the motion detecting section **22**, by searching the block resembling the currently processed block from the adjacent blocks **202***b* within the even field memory **29** and outputting the result as the motion vector **203**. The motion compensated prediction signal **204***b* corresponding to this motion vector **203** is outputted from the even field memory **29**.

The interpolation processing is carried out in the interpolating section **20** shown in FIG. **9**, by using the motion compensated prediction signals **204***a* and **204***b* to generate the interpolation predictive signal **204***c*, signal **204***a* being generated by motion compensated in accordance with the motion vector **203** and provided from the odd field memory **28**, and motion compensated predictive signal **204***b* being generated by motion compensated in accordance with the motion vector **203** and provided from the second field memory **9**. A predictive signal having the minimum error signal power with respect to the currently encoding object block of the input image signal **201** is selected by the selector **21** from among the motion compensated prediction

signal **204***a* obtained from the odd field, the motion compensated prediction signal **204***b* obtained from the even field, and the interpolated motion compensated prediction signal **204***c*, and then the predictive signal **210** is produced.

FIG. **11** is a diagram showing the operation explained above. It is assumed that the odd field memory **28** shown in FIG. **7** stores an odd field K1 of the preceding (previous) frame, while the even field memory **29** of FIG. **7** stores an even field G1 of the preceding frame. Here, the case where an odd field K2 and an even field G2 are included in the current (present) frame of the input image signal **201** will be discussed. First, when the odd field K2 is inputted, the motion compensated prediction signal **204***a* from the odd field K1 of the preceding frame stored in the odd field memory **28** is provided to the selector **21**. In the same manner, the even field G1 of the preceding frame stored in the even field memory **29** is provided to the selector **21** as the motion compensated prediction signal **204***b*. Then, the data of K1 and G1 are applied to the interpolating section **20** and tile interpolation processing as shown in FIG. **9** is conducted. Thereafter, such data is supplied to the selector **21** as the motion compensated prediction signal **204***c*. The selector **21** compares these three kinds of motion compensated prediction signals **204***a*, **204***b*, **204***c* and the input image signal **201** to select the prediction signal which has the minimum error signal power.

In the same manner, the selector **21** is responsive to the even field G2 of the current frame to receive the prediction signal **204***a* based on the odd field K1 stored in the odd field memory **28**, the motion compensated prediction signal **204***b* based on the even field G1 stored in the even field memory **29**, and the motion compensated prediction signal **204***c* obtained by the interpolation process on the basis of these motion compensated prediction signals **204***a*, **204***b* based on both fields, and to select the prediction signal which has the minimum error signal power.

In this embodiment (FIG. **7**), the interpolation section is provided to conduct the interpolation processing based on the motion compensated prediction signals **204***a*, **204***b* from the odd field memory **28** and even field memory **29** and thereby motion compensated prediction signal **204***c* is produced. However, it is also possible that the interpolation section **20** is not used as shown in FIG. **12**. In this case, the motion compensated prediction signal is generated in the selector **21** on the basis of the preceding odd field K1 stored in the odd field memory **28** and the preceding even field G1 stored in the even field memory **29** and the selector **21** selects the prediction signal minimizing the error signal power in these two kinds of motion compensated prediction signals **204***a*, **204***b*.

Further, in the embodiment shown in FIG. **7**, the simple arithmetic mean has been used for the interpolation section, but coding ensuring higher prediction efficiency can be realized by utilizing a weighted arithmetic mean taking into consideration field distance, as will be explained hereunder with reference to FIG. **13**.

FIG. **13** is a block diagram of an example of the interpolation circuit **20**. The motion compensated prediction signal **204***a* from the odd field is multiplied by a weight α based on the distance to the field to be encoded, and the motion compensated prediction signal **204***b* from the even field is multiplied by a weight β based on the distance to the field to be encoded. Thereafter, the arithmetic mean of these values is obtained and the output thereof is used as interpolation predictive signal **204***c*.

The practical value of the weighting by the interpolation section **20** in relation to the embodiment shown in FIG. **13** will be explained with reference to FIG. **11**.

As shown in FIG. **11**, when T is considered a unit of time for inputting an odd field or an even field, there is a time difference of 2T between odd field K1 and odd field K2. On the other hand, there is a time difference of T between even field G1 and odd field K2. Thus, the weights α and β can be determined by utilizing such time differences. For example, since the odd field K1 has a time distance of 2T, the weight α is set to 1. Also, since even field G1 has a time distance of T from odd field K2, the value of weight can be increased for the field having the lesser time distance by setting the value of β to 2. In the same manner, odd field K1 has a time distance of 3T from even field G2 and even field G1 has a time difference of 2T. Thus, it is possible to give the value of weight which is proportional to the time difference by setting α to 2 and β to 3 for weighting even field G2.

In the embodiment shown in FIG. **13**, the weights α and β are determined in the interpolating section on the basis of time distance. However, it is also possible that the Weight a to be given to the odd field is always set, for example, larger or smaller than weight β to be given to the even field regardless of the time distance. Further, in this embodiment, weights α and β used for the odd fields are different from those used for the even fields but the weights for the odd fields may be equal to those for the even fields. In addition, in this embodiment only weights α and β are used, but the weights may be determined in accordance with the other coefficients, for example, a coefficient having a quadratic function or another function having particular characteristics. Moreover, weights α and β do not have to be restricted only to one kind of value; it is possible that several kinds of weights α and β are prepared and selected in accordance with the kind of input signal or the characteristic of input signal.

Another embodiment of the present invention will be explained with reference to FIG. **14**.

The embodiment shown in FIG. **14** comprises a blocking selection section **82** for selecting between an individual blocking of a prediction error signal for the odd and even fields and a non-interlace blocking including both odd and even fields; a blocking forming section **83** for conducting the blocking in accordance with the output of the blocking selection section **82**; and a blocking decomposing section **84** for decomposing the blocking to form the original field in accordance with the block selection output. Section **400** enclosed by a broken line denotes blocking means and the other sections **200**, **300**, **500** are similar to those shown in FIG. **7**.

FIG. **15** is a block diagram of an example of the blocking selection section **82**. The prediction error signal **205** is stored in the odd field memory **31** for the odd field and in the even field memory **32** for the even field. As shown in FIG. **16**(*a*) and **16**(*b*), a block of p=16, q=16 is considered. The individual field blocking section **33** executes the blocking including the pixels of either of the odd or even field within the block of (p pixels×q lines), and these pixels are encoded in a coding section **35**. As shown in FIG. **16**(*c*), a non-interlace blocking section **34** executes the blocking of (p pixels×q lines) included in the block by alternately arranging the pixels of both odd and even fields, and these pixels are encoded in a coding circuit **36**. The information quantity comparing section **37** compares the quantity of data encoded in the coding section **35** and the coding circuit **36**, and outputs a blocking selection signal **211** indicating the blocking having the least amount of information.

FIG. **17** is a block diagram of an example of the blocking forming section **83**. The prediction error signal **205** is stored

in the odd field memory **41** for the odd field and in the even field memory **42** for the even field. In accordance with the blocking selection signal **211** supplied from the blocking selection section **82**, the blocking forming section **43** selects the blocking of the prediction error signals stored in the odd field memory **41** and even field memory **42** from the blocking including pixels of either of the odd or even field within the block of (p pixels×q lines) and the blocking including pixels of both odd and even fields within the block of (p pixels×q lines), and then outputs the blocked prediction error signal.

FIG. **18** is a block diagram of an example of the blocking decomposing section **84**. The data decoded by a local decoding circuit **25** is applied to the blocking decomposing section **44** in which the blocking is decomposed in accordance with the blocking selection signal **211** from the blocking selecting section **82**, and the decomposed block is then stored in the individual field memories **45, 46**. The stored data is supplied as a decoded error signal **207**.

The operation of this embodiment is explained hereunder.

The prediction error signal **205** obtained by subtracting the prediction signal **210** from an input signal **201** in a difference circuit **23** is sent to the blocking forming section **83** shown in FIG. **17** and to the blocking selection section **82** shown in FIG. **15**. The blocking selection section **82** produces the blocking selection signal **211** for selecting the blocking including the pixels of either the odd or even field in the block of (p pixels×q lines), or the blocking including the pixels of both odd and even fields in the block of (p pixels×q lines). The blocking forming section **83** conducts individual field blocking or non-interlace blocking in units of (p×q) blocks in accordance with the blocking selection signal **211**. The blocked signal is applied to the coding circuit **24**. The coding section **24** execute the orthogonal transform and sends the encoded data **206** which is a scalar-quantized transform coefficient to both the local decoding section **25** and the multiplexing section **28**.

After the inverse scalar-quantization and inverse orthogonal transform by the local decoding section **25**, the data is decomposed into the odd and even fields in the blocking decomposing-section shown in FIG. **18** which decomposes the blocking into the fields in accordance with the blocking selection signal **211** in order to obtain the decoded difference signal **207**. The local decoded signal **208** obtained by adding a predictive signal **210** to the decoded difference signal **207** in the adder **207** is stored in the first field memory **28** when it is the odd field or in the second field memory **29** when it is the even field, to detect the motion of each field of the next frame.

In this embodiment, a unit of blocks is formed of p=16, q=16, but it is desirable that the values of p and q have the following relationship with the block size n×m used by the motion detecting section **22** as explained in the embodiment shown in FIG. **7**:

$$p=n,\ q=2m$$

Since DCT transform is often carried out in the block unit of 8 pixels×8 lines, the size of 16 pixels×16 lines combining four block units is selected as the values of p and q in the blocking forming section. In this example, since P=n, n=16 pixels. Also, since q=2m, m=8. Thus, it is desirable that the number of lines be reduced to **8** because the motion detecting section **22** detects motion for both the odd and even fields. Meanwhile, since it is possible to employ the blocking combining the odd field and even field in the blocking forming section, it is desirable to form a block of 16 lines including the odd and even fields.

In the embodiment shown in FIG. **14**, the blocking has been selected by comparing the quantity of information generated as showman in FIG. **15**, but coding based on the quality of encoding can be realized by selecting the blocking on the basis of the comparison of encoding quality as shown in FIG. **19**.

FIG. **19** is a block diagram of an example of the blocking selection section **82**. The predicting error signal **205** is stored in the odd field memory **51** for the odd field and in the even field memory **52** for the even field. The individual field blocking section **53** realizes the blocking including the pixels of either the odd field or the even field within the block of (p pixels×q lines), and the coding/decoding section **55** enables encoding/decoding. At the same time, the non-interlace blocking section **54** realizes the blocking including the pixels of both fields within the block of (p pixels×q lines), and the coding/decoding circuit **56** enables coding/decoding. The difference between the encoded/decoded data of the individual field blocking and the data just before the encoding is compared with the difference between the encoded/decoded data of the combined field blocking and the data just before the encoding, by the error comparator **59** in order to select the blocking with less errors and to provide an output as the blocking selection signal **211**.

In the embodiment shown in FIG. **14**, the quantity of generated information has been compared for the selection of the block, while in the embodiment shown in FIG. **19**, the encoding errors have been compared. However, encoding with higher efficiency can be realized when conducting encoding utilizing the orthogonal transform, by selecting the blocking on the basis of the comparison of frequency components produced by the difference of blocking as shown in FIG. **20**.

FIG. **20** is a block diagram of an example of the blocking selection circuit **82**. The predicting error signal **205** is stored in the odd field memory **61** for the odd field and in the even field memory **62** for the even field. The individual field blocking section **63** executes the blocking including the pixels of only either the odd field or even field within the block of (p pixels×q lines), and a frequency analyzing section **65** such as that shown in FIG. **21** executes the frequency analysis. The non-interlace blocking circuit **64** executes the blocking including pixels of both fields within the block of (p pixels×q lines), and a frequency analyzing circuit **66** such as that shown in FIG. **21** executes the frequency analysis. The blocking with fewer high-frequency components is selected from the individual field blocking and the combined field blocking to output the blocking selection signal **211**.

FIG. **21** is a block diagram of an example of the frequency analyzing sections **65** and **66**. The signal obtained by individually blocking the odd and even fields from the individual field blocking circuit **63**, and the signal obtained by blocking the pixels of both odd and even fields from the non-interlace blocking section **64**, are supplied to sections **65** and **66**. These signals are converted to a signal in the frequency domain from a signal in the pixel domain using the orthogonal transform **68**. The high-frequency components are extracted from the converted signal in the frequency domain by a high-frequency component selector **69** and the extracted high-frequency components are totaled by a high-frequency component accumulator **70**. The accumulated high-frequency components are compared in a high-frequency component comparing section **67** to select the blocking with fewer amount high-frequency components.

FIG. **22** shows an example of the components accumulated by the high-frequency component adder **70** from the

orthogonal transformed frequency domain signal. Here, eight components, for example, having the maximum frequency, component in the vertical frequency component, are selected.

In this embodiment, the coding section **24** does not use the selection information of predictive signals or the selection information of blocking, but according to another embodiment shown in FIG. **23**, finer control is possible and high encoding quality can be realized by inputting an output of the selector **11** as the selection signal for the predictive signal and the blocking selection signal as the selection signal for the blocking to the coding section **24** and by controlling the encoding characteristic with the selected prediction signal and the information of the selected blocking.

As explained above, the embodiment of FIG. **7** relates to a system for realizing predictive coding of an input image signal obtained by the interlaced scanning method with the motion compensation. The system includes motion detecting means for obtaining, for the odd or even field of the input image signal, the amount of displacement, in order to carry out the individual motion compensated prediction, in units of the block of (n pixels×m lines) (n and m: positive integer) from both the odd and even fields of the already encoded frame, and the prediction error signal output means for selecting, with a selector **21**, the predictive signal indicating the optimum prediction from signals including a first predictive signal **204***a* obtained by the motion compensation from the odd field, a second predictive signal **204***b* obtained by the motion compensation from the even field, and a third predictive signal **204***c* obtained by interpolating the first and second predictive signals in order to obtain the difference from the field of the input signal and output the result as the prediction error signal.

Moreover, the embodiment of FIG. **7** is an adaptive field/frame coding system characterized in that the interpolation means for obtaining the third predictive signal is the simple arithmetic mean of the first predictive signal and the second predictive signal.

Thus, the hardware can be minimized in size and encoding with higher prediction efficiency can be realized by generating an interpolation signal of the predictive signal by simply obtaining the arithmetic mean of both predicted odd and even fields with motion compensation.

Further, the embodiment of FIG. **13** is an adaptive field/frame coding system characterized in that the interpolation means for obtaining the third predictive signal is the weighted arithmetic mean of the first predictive signal and the second predictive signal, also considering the time distance of the field used for the prediction and the field to be encoded.

Thus, encoding ensuring very high prediction efficiency can be realized by generating the interpolation signal from the weighted arithmetic mean of both predicted odd and even fields with the motion compensation, while considering the time distance of the field used for the prediction and the field to be encoded.

The embodiment shown in FIG. **14** is an adaptive field/frame coding system comprising means for enabling encoding by selecting blocking including the pixels of either the odd field or even field within the block of (p pixels×q lines), or blocking including the pixels of both odd and even fields within the block of (p pixels×q lines), in order to encode the prediction error signal for the odd and even fields of the input image signal in units of the block of (p pixels×q lines) (p and q: positive integer).

Moreover, the embodiment shown in FIG. **14** is an adaptive field/frame coding system characterized in that the blocking means for enabling encoding while selecting the blocks comprises selecting means for selecting the blocking with less information for encoding from blocking including the pixels of only one of the odd field and even field within the block of (p pixels×q lines), and blocking including the pixels of both odd and even fields within the block of (p pixels×q lines).

The embodiment shown in FIG. **19** is an adaptive field/frame coding system characterized in that the blocking means for enabling encoding while selecting the blocks comprises means for selecting the blocking smith less encoding error from blocking including the pixels of only one of the odd field and even field within the block of (p pixels×q lines), and blocking including the pixels of both odd and even fields within the block of (p pixels×q lines)

The embodiment shown in FIG. **20** is an adaptive field/frame coding system characterized in that the blocking means for enabling encoding while selecting the blocks comprises selecting means for selecting the blocking with less high-frequency components included in the signal to be encoded from blocking including the pixels of only one of the odd field and even field within the block of (p pixels×q lines), and blocking including the pixels of both odd and even fields within the block of (p pixels×q lines).

In addition, the embodiment shown in FIG. **23** is an adaptive field/frame coding system characterized by enabling encoding while selecting the quantization characteristic of the transform coefficient in accordance with the selected predictive signal and the selected blocking, in the case of employing the orthogonal transformer and carrying out encoding by the quantization of transform coefficient in the coding section for the encoding in units of the block of (p pixels×q lines).

In the above embodiments, an input image signal **201** is formed of the frame including the odd field and even field. However, the use of the odd field and even field is intended to show only an example, and the field is not restricted to the odd or even field. The present invention can be useful whenever one frame is divided into fields, the odd field and even field being only examples of such fields of a frame. For instance, the present invention can also be applied to a case of storing data by dividing the frame into two fields every two lines by, for example defining the first field as the 1st and 2nd lines and the second field as the 3rd and 4th lines, and defining the first field as the 5th and 6th lines and the second field as the 7th line and 8th line. etc. Moreover, in addition to dividing a frame into two kinds of fields, such as the odd field and the even field or the first field and the second field, the present invention can also be applied to the case of dividing a frame into more than two fields, for example, three or four kinds of fields. In such a case, the number of field memories corresponds to the number of kinds of fields, and the processing explained above is carried out for each field.

In the above embodiments, the blocking selection section selects the blocking from two kinds of blocking, including the blocking of the pixels of only one of the odd field and even field and the blocking of the pixels of both odd and even fields. However, the blocking may include various combinations when two or more fields are prepared in addition to the odd and even fields. The blocks shown in FIGS. **16**(*a*), (*b*), (*c*) are only examples and various block forming methods may be used to form the block other than the blocks of FIG. **16**.

In the above embodiments, the blocking means shown in FIG. **14** is used with the prediction error signal output means and motion detecting means. Even if the sections other than the blocking means **400** are replaced with conventional means, the 8th and 9th aspects explained above can be provided.

According to the 6th and 7th aspect explained above, a stable encoded image with high efficiency can be obtained by individually searching the motion from each field of the already encoded frame to predict each field and by conduct-

ing adaptive prediction from the searched motion compensated predictive signals (and interpolation signals). In addition, according to the 8th and 9th aspects explained above, a stable encoded image with high efficiency can also be obtained by adaptively selecting the encoding from the blocking of the pixels of only one of the fields of the frame to be encoded, and the encoding after conducting the blocking of the pixels of the respective fields when encoding the prediction error signal.

What is claimed is:

1. A video signal encoder for encoding a first motion video signal representative of sequential video images including first and second video images into a second motion video signal comprising:

a predictive error signal generator for generating a predictive error signal representative of the error in the second video image based on a prediction formed at least in part from the first video image;

a coder for transform coding the predictive error signal to produce a coded predictive error signal, said coder varying the scanning sequence of the transform coefficients thereof;

a local decoder detecting the scanning sequence of transform coefficients used in transform coding, and decoding the transform coefficients of the coded predictive error signal to produce information representative of the first motion video signal including the first video image;

a combiner, operatively connected to said local decoder, and combining the predictive error signal with a predictive signal;

an image data memory, operatively connected to said combiner, for storing information representative of the first video image as image data;

a predictive signal generator, operatively connected to said image data memory, and supplying the predictive signal from the image data stored in said image data memory to said predictive error signal generator and said combiner;

wherein a signal representative of the second video image of the first motion video signal is assembled from the predictive error signal developed from a difference between the first video image and the second video image;

wherein the coded predictive error signal from said coder is output as the second motion video signal.

2. The encoder of claim 1 wherein said coder varies the scanning sequence used in transform coding based on encoding efficiency.

3. The encoder of claim 1 wherein:

said predictive error signal generator includes a subtracter, operatively connected to said predictive signal generator, and subtracting the predictive signal from a signal representative of the second video image of the first motion video signal to form the predictive error signal; and

a block former, operatively connected to said subtracter, and forming the predictive error signal into blocks;

said coder being operatively connected to said block former, and encoding the blocked predictive error signal to form the coded predictive error signal.

4. A video signal conversion system for converting between a first motion video signal representative of sequential video images including first and second video images and a second motion video signal comprising:

a decoder detecting the scanning sequence of transform coefficients used in transform coding, and decoding the transform coefficients to produce information representative of the first and second video images;

an image data memory for storing information representative of the first video image as image data;

a predictive signal generator, operatively connected to said image data memory, and supplying a predictive signal from the image data stored in said image data memory;

wherein a signal representative of the second video image is assembled from a predictive error signal output from said decoder and developed from a difference between the first video image and the second video image; and

a combiner, operatively connected to said image data memory, and combining the signal representative of the second video image with the predictive signal produced by said predictive signal generator.

5. The video signal conversion system of claim 4 wherein the scanning sequence used in transform coding the transform coefficients is determined based on coding efficiency.

6. The video signal conversion system of claim 4 wherein the conversion system converts from the first motion video signal to the second video signal.

7. The video signal conversion system of claim 4 wherein said image data memory stores said image data and said predictive signal generator supplies plural predictive signals from the image data, said predictive signal generator including,

an interpolator, operatively connected to said image data memory, interpolating at least some of the plurality of predictive signals and generating an interpolated predictive signal which is different from any of the plurality of predictive signals supplied by said predictive signal generator, and

a selector, receiving the plural predictive signals and the interpolated predictive signal, and selecting a predictive signal from the plurality of predictive signals and the interpolated predictive signal.

8. The video signal conversion system of claim 7 wherein said combiner includes an adder, said adder adding the predictive error signal and the interpolated signal produced by said interpolator and supplying the output thereof to said image data memory.

9. The video signal conversion system of claim 7 further comprising:

a subtracter, operatively connected to said selector, and subtracting one of the plural predictive signals including the interpolative predictive signal from a signal representative of the second video image of the first motion video signal to form the predictive error signal; and

an encoder, operatively connected to said subtracter, and encoding the predictive error signal to form an encoded predictive error signal, wherein said encoder varies the scanning sequence used in transform coding the transform coefficients;

said decoder being operatively connected to said encoder, for decoding the encoded predictive error signal for supply to said combiner.

10. The video signal conversion system of claim 7 wherein the interpolator produces the interpolated predictive signal by computing the arithmetic mean of at least some of the plural predictive signals.

* * * * *

Exhibit 8

US005654706A

United States Patent [19]

Jeong

[11] Patent Number: 5,654,706

[45] Date of Patent: *Aug. 5, 1997

[54] **SYSTEM FOR VARIABLE LENGTH DECODING DIGITAL TRANSMISSION DATA WHICH HAS BEEN COMPRESSED BY SELECTING A SCANNING PATTERN**

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[73] Assignee: **Samsung Electronics Co., Ltd.**, Kyungki-do, Rep. of Korea

[*] Notice: The term of this patent shall not extend beyond the expiration date of Pat. No. 5,602,549.

[21] Appl. No.: **768,468**

[22] Filed: **Dec. 18, 1996**

Related U.S. Application Data

[63] Continuation of Ser. No. 532,987, Sep. 22, 1995, Pat. No. 5,602,549, which is a continuation of Ser. No. 95,468, Jul. 23, 1993, Pat. No. 5,497,153.

[30] **Foreign Application Priority Data**

Jul. 23, 1992 [KR] Rep. of Korea 92-13171

[51] **Int. Cl.**[6] **H03M 7/40**

[52] **U.S. Cl.** **341/67**; 348/408

[58] **Field of Search** 341/67; 348/404

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,754,336	6/1988	Nishizawa	348/415
4,821,119	4/1989	Gharavi	348/402
4,908,862	3/1990	Kaneko et al.	348/409
4,972,260	11/1990	Fujikawa .	
5,021,891	6/1991	Lee .	
5,134,396	7/1992	Sirat et al.	341/51
5,227,878	7/1993	Puri et al.	348/416
5,367,629	11/1994	Chu et al.	348/403
5,424,778	6/1995	Sugiyama	348/403

FOREIGN PATENT DOCUMENTS

0301712	2/1989	European Pat. Off. .
62-145988	6/1987	Japan .
3 266564	11/1991	Japan .

OTHER PUBLICATIONS

Mutsima Ohta, et al., "A Comparison of Various Entropy Coding Methods for MCT/DCT Hybrid Coding", Mar. 19, 1987, pp. 17–24.

Primary Examiner—Howard L. Williams
Attorney, Agent, or Firm—Sughrue, Mion, Zinn, Macpeak & Seas

[57] **ABSTRACT**

A system for variable-length-coding and variable-length-decoding digital data divided into a block unit of a predetermined size which includes variable-length-coding each block data according to various scanning patterns, accumulating the various lengths of variable-length-coded data, selecting a scanning pattern corresponding to a minimum accumulated length, transmitting the variable-length-coded data according to the selected scanning pattern and scanning the transmitted data according to the same scanning pattern as applied to variable-length-coding process, thereby the scanned data being variable-length-decoded. As a result, data compression can be improved efficiently by means of utilizing an optimized scanning pattern for variable-length-coding and variable-length-decoding of the block data.

45 Claims, 4 Drawing Sheets

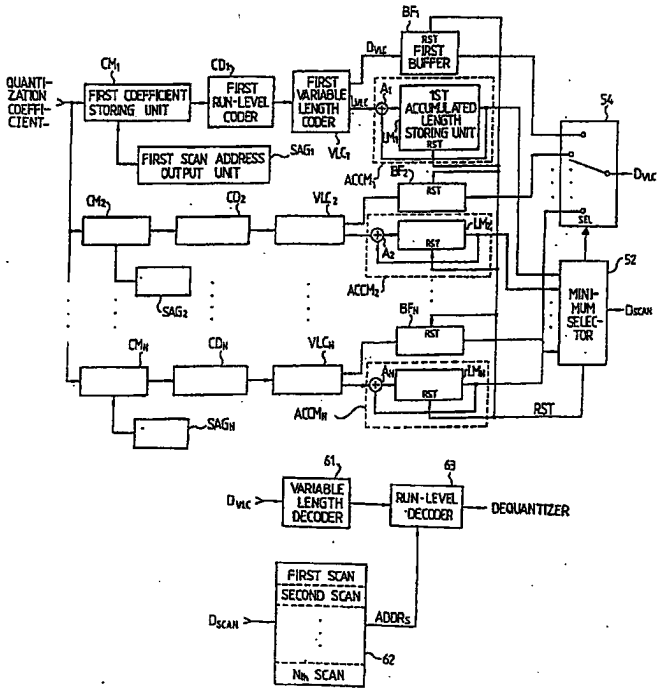


FIG . 1 (PRIOR ART)

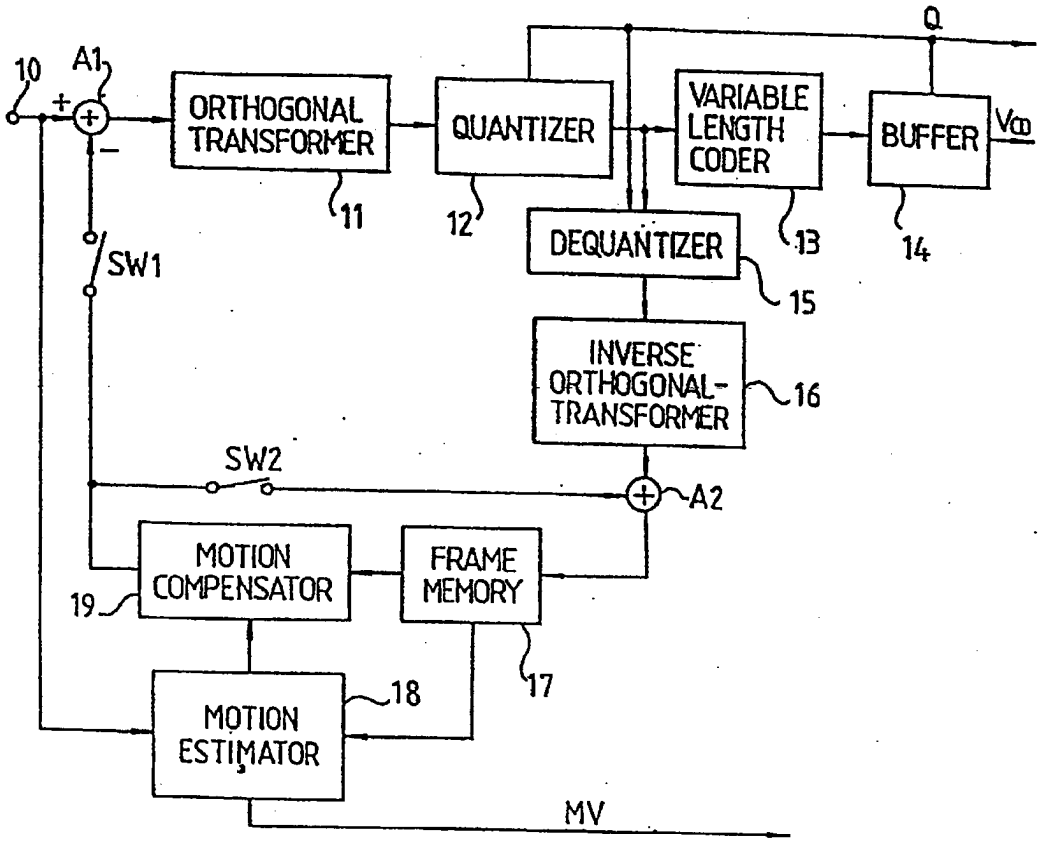


FIG . 2 (PRIOR ART)

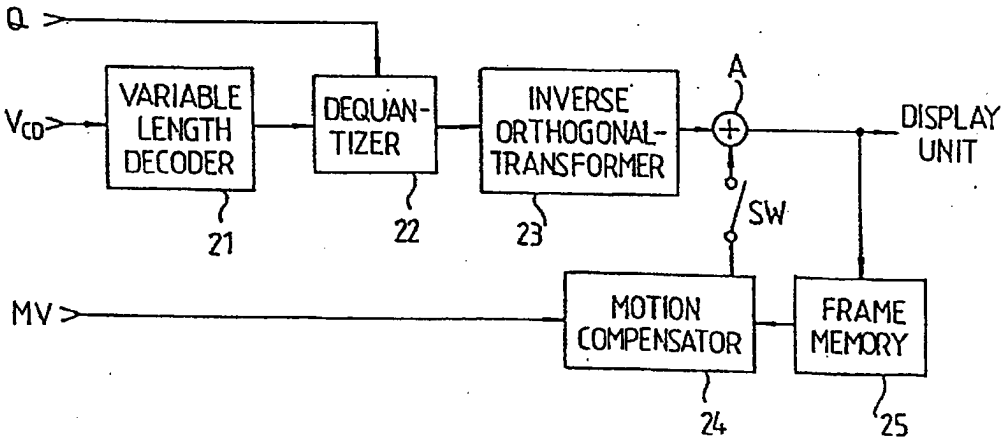
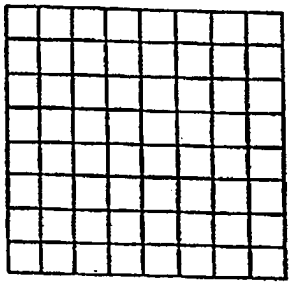
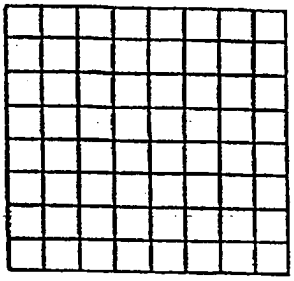


FIG. 3A (PRIOR ART)



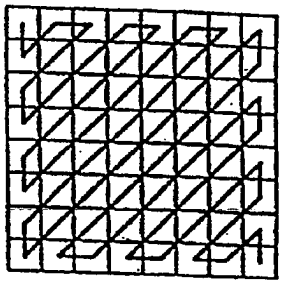
8×8 BLOCK DATA

FIG. 3B (PRIOR ART)



8×8 QUANTIZATION COEFFICIENTS

FIG. 3C (PRIOR ART)



[RUN·LEVEL] CODING WITH ZIGZAG SCANNING PATTERN

FIG. 4 (PRIOR ART)

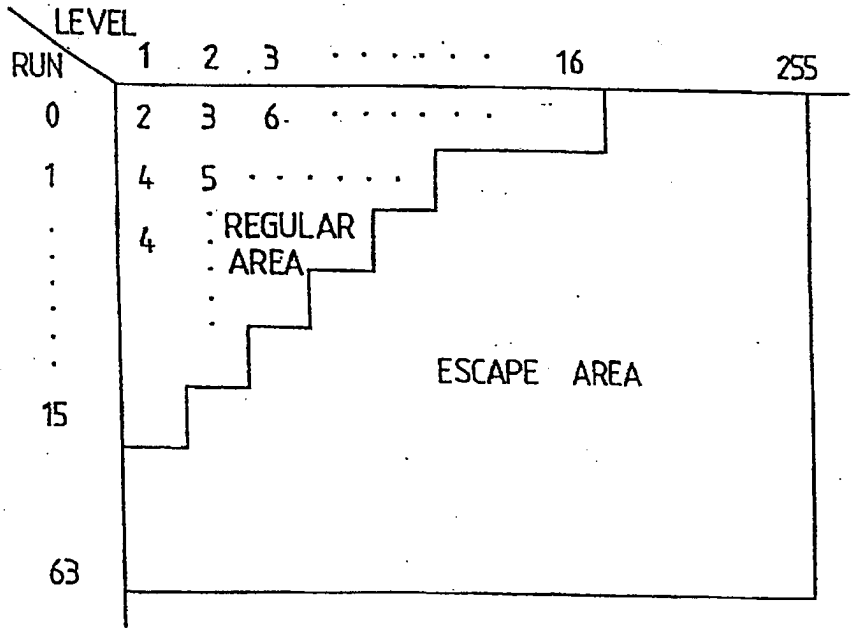


FIG. 5

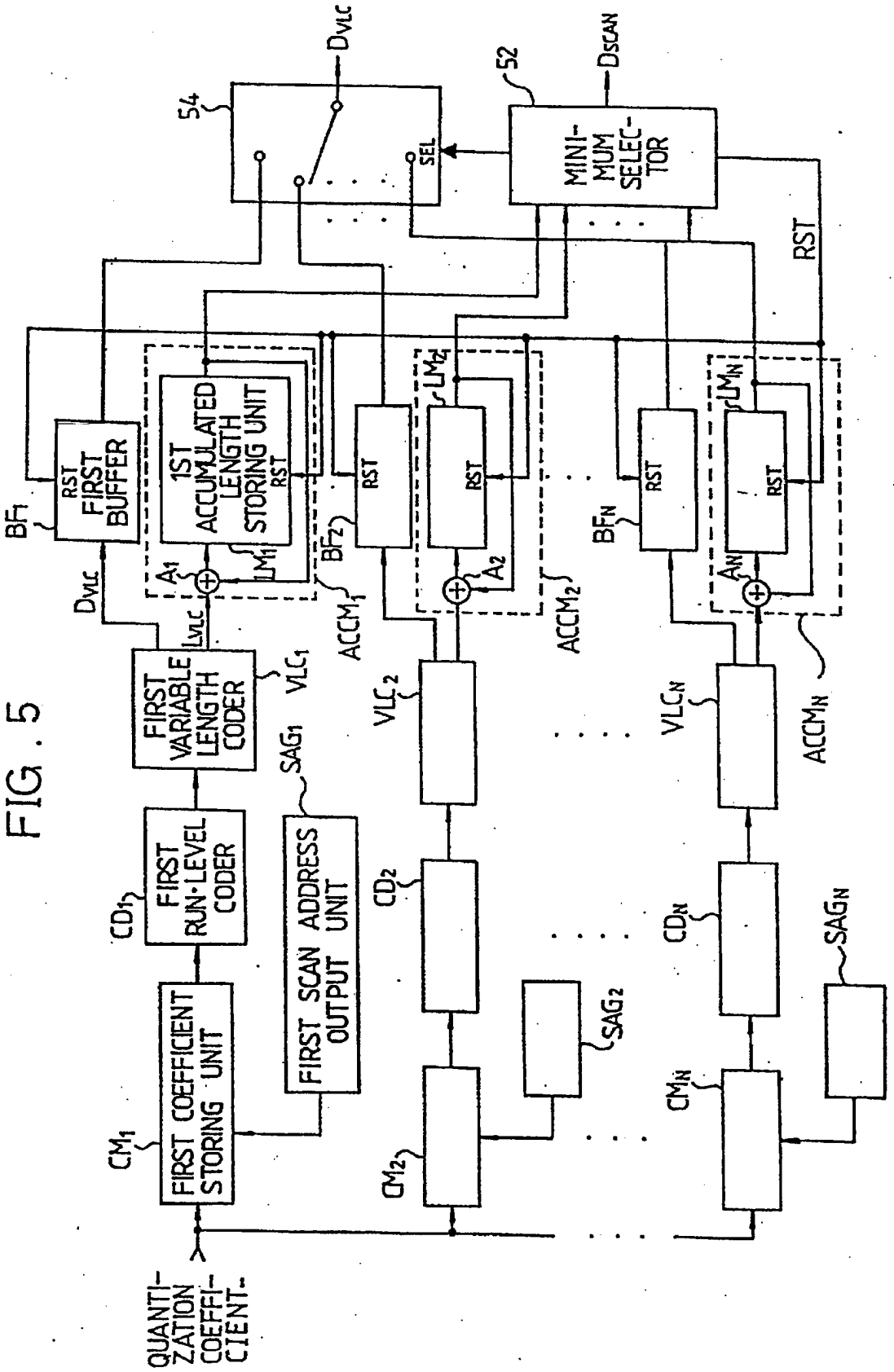

DVLC
DSCAN
52
54
SEL
MINI-MUM SELEC-TOR
RST
BF1
RST FIRST BUFFER
1ST ACCUMULATED LENGTH STORING UNIT
RST
LM1
A1
ACCM1
BF2
RST
LM2
A2
ACCM2
BFN
RST
LMN
AN
ACCMN
DVLC
LVLC
FIRST VARIABLE LENGTH CODER
VLC1
VLC2
VLCN
SAG1
CD1
FIRST RUN-LEVEL CODER
CD2
CDN
SAGN
FIRST SCAN ADDRESS OUTPUT UNIT
SAG2
CM1
FIRST COEFFICIENT STORING UNIT
CM2
CMN
QUANTI-ZATION COEFFI-CIENT-

FIG . 6

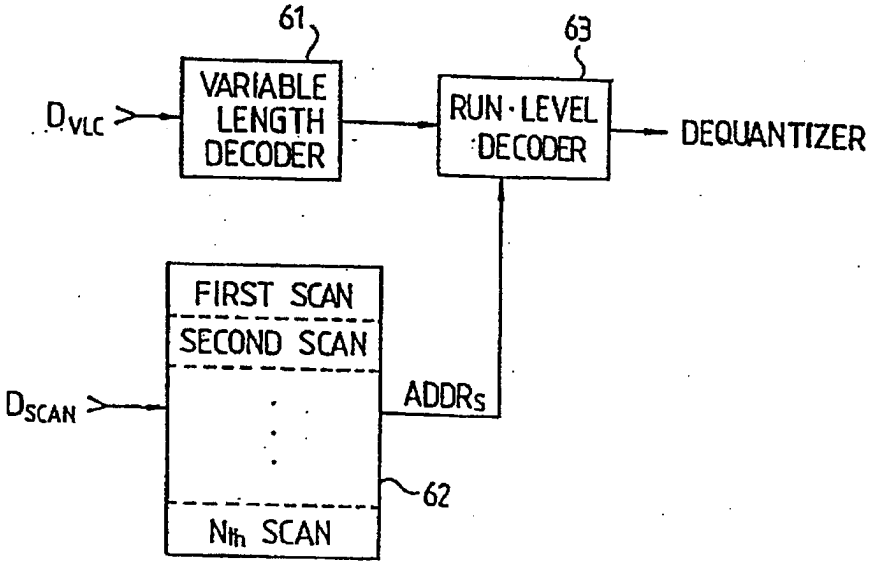


FIG . 7A

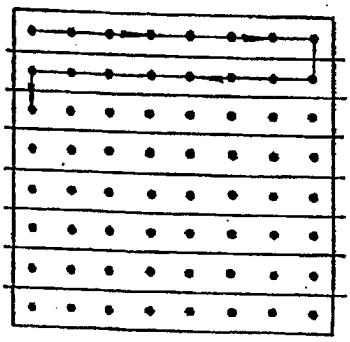


FIG . 7B

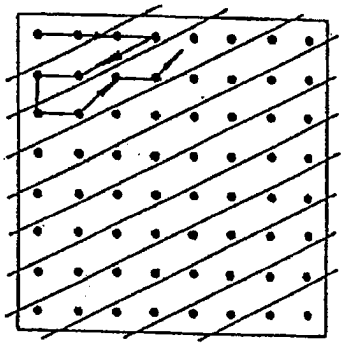
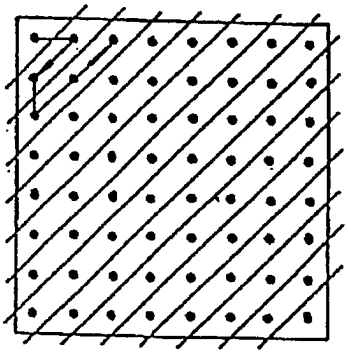


FIG . 7C



SYSTEM FOR VARIABLE LENGTH DECODING DIGITAL TRANSMISSION DATA WHICH HAS BEEN COMPRESSED BY SELECTING A SCANNING PATTERN

This is a continuation of application Ser. No. 08/532,987 filed Sep. 22, 1995, now U.S. Pat. No. 5,602,549 which is a Continuation Application of prior application Ser. No. 08/095,468, Jul. 15, 1993, now U.S. Pat. No. 5,497,153.

FIELD OF THE INVENTION

The present invention relates to a system for coding and decoding digital data, and more particularly to a coding and decoding system for variable-length-coding the digital data of a predetermined size with an optimized scanning pattern among various scanning patterns and decoding the variable-length-coded data, thereby improving further a compression of transmission data. The present disclosure is based on the disclosure of Korean Patent Application No. 92-13171 filed Jul. 23, 1992, which disclosure is incorporated herein by reference.

BACKGROUND OF THE INVENTION

Recently, a method for coding a video and audio signal into digital data so as to be transmitted or stored in a storing unit, and decoding the coded digital data so as to be reproduced has been used in a system for transmitting and receiving a video and audio signal. However, there is needed a technique for compressing further the quantity of transmission data so as to optimize a transmission efficiency of data in such a coding and decoding system. There have been a transformation coding method, a Differential Pulse Code Modulation (DPCM) method, a vector quantization method and a variable-length-coding method, etc., as methods for coding such transmitted or stored digital data. The coding methods compress a total quantity of data, by removing redundancy data which is included in the transmitted or stored digital data.

The video data of each frame is divided into a block unit of a predetermined size and data-processed in a coding and decoding system for transmitting and receiving the video signal. Each block data or differential data between block data is orthogonal-transformed, so that the video data is transformed into transformation coefficients in the frequency domain. There-have been a Discrete Cosine Transform (DCT), a Walsh-Hadamard Transform (WHT), a Discrete Fourier Transform (DFT) and a Discrete Sine Transform (DST), etc., as block data transformation methods. The transformation coefficients obtained by such transformation methods are coded properly according to the characteristic of coefficient data, so that compressed data is gained or increased. Since one's sight is more sensitive to the low frequency than the high frequency, the data in the high frequency is reduced under data-processing. Accordingly, the quantity of the coded data can be decreased.

FIG. 1 represents a schematic block diagram of a conventional coding apparatus of a video data. First, an input terminal **10** is input with N×N blocks (which is generally represented as $N_1 \times N_2$, and which for the convenience of explanation, is assumed as $N_1=N_2=N$). The block data input through the input terminal **10** is added to a predetermined feedback data in a first adder A1, thereby calculating differential data between the two data (i.e., between the input data and the feedback data). An orthogonal transformer **11** discrete-cosine-transforms input differential data, thereby

causing the differential data to be transformed into coefficients in the frequency domain. A quantizer **12** changes coefficients transformed through a predetermined quantizing process into representative values of various levels. Then, the quantizer **12** variably quantizes the output data from the orthogonal transformer **11** according to a quantization level (Q) input from a buffer **14**. A variable length coder **13** variable-length-codes the block data taking statistical characteristics of the quantization coefficients into consideration, thereby transmitting Compressed data (V_{CD}). A variable-length-coding procedure with respect to the video data will be described hereinafter. The buffer **14** is input with a compression data from the variable length coder **13** and outputs the data to a transmission channel at a constant speed. Then, the quantization level (Q) is output for controlling the quantity of input data, so as to prevent an overflow or an underflow in transmission data.

Generally, there are similar patterns between adjacent frames in the video data. Accordingly, in case of slight movement of an image, the motion of the image is estimated by comparing a present frame with previous frames. A motion vector (MV) is calculated as a result of the motion estimation. A motion compensation is achieved from previous frames with a motion vector. The quantity of differential data between block data obtained from motion compensation and block data input to the input terminal **10** is very small, so that the data can be further compressed in the above coding process. A feedback loop for performing the motion estimation and motion compensation includes a dequantizer **15**, an inverse orthogonal-transformer **16**, a frame memory **17**, a motion estimator **18** and a motion compensator **19**. The dequantizer **15** and inverse orthogonal-transformer **16** dequantizes and inversely discrete-cosine-transforms the quantization coefficients output from the quantizer **12**, and transforms them into video data in the spatial domain. A second adder A2 adds the video data output from the inverse orthogonal-transformer **16** to the feedback data input via a second switch SW2, thereby outputting a resultant block data. The block data output from the second adder A2 is sequentially stored in the frame memory **17**, thereby reconstructing a frame. A motion estimator **18** catches the block data, which is the most similar data in pattern with the block data input via the input terminal **10**, from the frame data stored in the frame memory **17**, and calculates the motion vector MV for estimating the motion of images from the two block data. The motion vector MV is transmitted to a receiver and the motion compensator **19**, in order to be used in a decoding system. The motion compensator **19** reads out the block data corresponding to the motion vector MV from the frame data in the frame memory **17**, and inputs the read data to the first adder A1. As described above, the first adder A1 calculates a differential data between the block data input from the input terminal **10** and the block data input from the motion compensator **19**, then the differential data is coded, and the coded data is transmitted to the receiver. Moreover, the two switches SW1 and SW2 in FIG. **1** are refresh switches for refreshing the data in the unit of a frame or block of a predetermined size, in order to prevent the difference between coded data of frames and unprocessed data of frames due to the accumulation of the differential data. The coded video data (V_{CD}) is transmitted to the receiver and input to a decoder such as is shown in FIG. **2**. A variable length decoder **21** decodes the input video data (V_{CD}) via an inverse process of variable-length-coding. A dequantizer **22** decodes quantization coefficients input from the variable length decoder **21**, thereby outputting transformation coef-

ficients in the frequency domain. An inverse orthogonal-transformer **23** transforms the transformation coefficients in the frequency domain, which are input from the quantizer **22**, into the video data in the spatial domain. The motion vector MV output from the motion estimator **18** of the coder is input to a motion compensator **24** of the decoder. The motion compensator **24** reads out the block data corresponding to the motion vector MV from the frame data stored in a frame memory **24**, and inputs the read data to an adder A. The adder A adds the differential data output from the inverse orthogonal-transformer **23** to the block data input from the motion compensator **24**, thereby outputting resultant reconstructed block data. A switch SW connected to an output terminal of the motion compensator **24** plays the same role with the refresh switches as the above described coder in FIG. **1**.

There has been used a Huffman Code for variable-length-coding in a conventional coding system. Huffman Coding allocates different codes in length according to a probability of a predetermined symbol in the input data. That is, the higher the probability is, the shorter a code is allocated, and the lower the probability is, the longer a code is allocated. In coding by means of Huffman algorithm, in the case where there are multiforms of symbols in abundance, and numbers of symbols have low probabilities, when long codes are allocated for a plurality of rare symbols by the Huffman algorithm, data-processing comes to be further complicated in the process of coding and decoding. In order to solve these problems, in the case that a code with a predetermined fixed length is allocated for a distribution area of a plurality of rare symbols (which is hereinafter assumed as an escape area), the complexity of the data-processing is greatly reduced, even if an average code length can be increased more than an average value of original Huffman codes.

FIG. **3**A shows a two-dimensional 8×8 block of data, FIG. **3**B shows a two-dimensional 8×8 block of quantization coefficients which transform the block data into data in the frequency domain and quantize the transformed data, and FIG. **3**C shows the zigzag scan of the quantization coefficients from low frequency to high frequency, and codes the scanned coefficients into [run·level] symbols, considering that most quantization coefficients are "0" in the low frequency domain. The run means the number of 0's being between coefficients not "0", the level represent absolute values of coefficients not "0". In the case of the 8×8 data of FIGS. **3**A–**3**C, the run can have values from "0" to "63". In the case that the quantization output is an integer value from "–255" to "255" the level is a value from "1" to "255" and the sign is separately indicated.

FIG. **4** shows an escape area and a regular area classified according to probabilities of [run level] symbols. A probability of symbols with a large value of run and/or level in [run level] symbols is very low statistically. A distribution area of symbols with a low probability, is allocated as an escape area, in which the symbols are represented by an escape sequence of fixed length, and a regular Huffman code is allocated for the other area (regular area). For example, in the case of 8×8 block data, the escape sequence consists of 6-bit escape symbols, 6-bit runs for representing from "0" to "63", 8-bit levels for showing from "1" to "255" and a sign bit of 1-bit. Accordingly, the escape sequence has the fixed length of 21 bits.

A conventional variable-length-coding system has utilized a zigzag scanning pattern (described in FIGS. **3**A–**3**C) for N×N quantization coefficients in variable-length-coding the video data, because energies of the video signal are concentrated at the low frequency domain centering around

DC components. However, the energy of the video signal can be more widely distributed to frequency components of a horizontal orientation or a vertical orientation according to the pattern of the video signal. Therefore, a conventional zigzag scanning pattern is not an optimized scanning pattern for variable-length-coding the video data. Accordingly, the scanning pattern which can be adaptably changed to a horizontal orientation or a vertical orientation according to the distribution characteristics of the video data, are desirable for variable-length-coding and variable-length-decoding.

SUMMARY OF THE INVENTION

Therefore, to solve the above problems, it is one object of the present invention to provide a variable-length-coding system which adopts an optimized scanning pattern in accordance with data distribution characteristics for every block data and variable-length-codes every block data, in variable-length-coding the digital data which are partitioned into blocks of a predetermined size.

It is another object of the present invention to provide a variable-length-decoding system which variable-length-decodes a corresponding block data according to the same optimized scanning pattern as selected in the process of variable-length-coding for every block data.

The one object of the present invention, in a method for variable-length-coding the digital data which are divided into the block unit of a predetermined size, is achieved by the following steps. The method comprises the steps of scanning the block data according to various scanning patterns, and coding the scanned data to [run level] symbols in accordance with each of the scanning patterns; variable-length-coding respectively diverse [run level] symbols coded according to the various scanning patterns; accumulating separately the various lengths of data which are variable-length-coded at the variable-length-coding steps according to the various scanning patterns; selecting a scanning pattern corresponding to a minimum value among accumulated values of lengths of variable-length-coded data obtained at the accumulating steps according to the various scanning patterns; and selecting as transmission data, that data which is variable-length-coded during the variable-length-coding step according to the scanning pattern selected at the selecting step.

Another object of the present invention, in a method for variable-length-decoding the data which are variable-length-coded in a block unit of a predetermined size, is achieved by the following steps. The method comprises the steps of inputting variable-length-coded data by means of the above variable-length-coding method and scanning pattern data corresponding to the selected scanning pattern; variable-length-decoding the input variable-length-coded data; outputting a predetermined scan address corresponding to the input scanning pattern data; decoding variable-length-decoded [run level] symbols at variable-length-decoding step according to the scan address, thereby transforming the symbols into predetermined coefficients.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects and features of the present invention will become more apparent from the consideration of the following detailed description taken in conjunction with the accompanying drawings in which:

FIG. **1** is a block diagram showing an embodiment of a conventional coder.

FIG. **2** is a block diagram showing an embodiment of a conventional decoder.

FIGS. 3A–3C are diagrams for explaining a conventional scanning pattern and a coding process.

FIG. 4 is a diagram for explaining a distribution state of variable-length-coded data.

FIG. 5 is a block diagram showing an embodiment of a variable-length-coder in accordance with the present invention.

FIG. 6 is a block diagram showing an embodiment of a variable length decoder in accordance with the present invention.

FIGS. 7A—7C are diagrams for explaining the scanning patterns in the apparatus of FIGS. 5 and 6.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The preferred embodiment of the present invention will be described below with reference to the accompanying drawings.

FIG. 5 shows a variable length coder in accordance with an embodiment of the present invention. The coder of FIG. 5 comprises N coefficient storing units (CM1-CM_N) for respectively storing the quantization coefficients of quantized block data; N scan address output units (SAG_1-SAG_N) for inputting different scan addresses to each of the coefficient storing units; N [run level] coders (CD_1-CD_N) for [run level] coding coefficients in each of the coefficient storing units according to respective scanning patterns; N variable length coders (VLC_1-VLC_N) for variable-length-coding [run level] symbols output from each of the [run-level] coders according to a variable-length-coding map; N buffers (BF_1-BF_N) for storing the variable-length-coding data of each of the variable length coders; N accumulators ($ACCM_1$-$ACCM_N$) for separately accumulating the lengths of variable-length coded data output from each of the variable length coders; a minimum selector 52 for selecting a minimum value among accumulated lengths in N accumulators; and a selecting switch 54 for selecting and transmitting the buffer output of variable-length coding channels selected in the minimum selector.

First, the quantization coefficients which are quantized in a block unit of a predetermined size, are stored in each of the N coefficient storing units (CM1-CM_N). The first, second, and N coefficient storing units are respectively input the first, second, and N scan addresses which are separately output from the first, second, and N scan address output units. Described below is a coding channel for the first coefficient storing unit (CM_1) among N coefficient storing units which are scanned by each of the N scan addresses.

The quantization coefficients stored in the first coefficient storing unit (CM_1) are scanned toward a predetermined scanning orientation by the first scan address, and coded to a [run level] symbol in the first [run level] coder (CD_1). The first variable length coder (VLC_1) variable-length-codes the [run-level] symbol input from the first [run level] coder (CD_1) according to a predetermined variable-length-coding map, and respectively outputs variable-length-coded data (D_{VLC}) and the length of the variable-length-coded data (L_{VLC}). The variable-length-coded data (D_{VLC}) output from the first variable length coder (VLC_1) is stored in the first buffer (BF_1), and the length of the variable-length-coded data (L_{VLC}) is input and accumulated to the first accumulator ($ACCM_1$) which accumulates the lengths of code that are coded by the first unit (VLC_1). The first accumulator ($ACCM_1$) consists of an adder (A1) and an accumulated length storing unit (LM_1). The length of the variable-length-coded data (L_{VLC}) which is input from the first variable length coder (VLC_1) is added to accumulated lengths which are feedback from the first accumulated length storing unit (LM_1) in the adder (A1). The first accumulated length storing unit (LM_1) restores an update accumulated length output from the adder (A1). A series of such coding channels are applied to the quantization coefficients of the second, third, and N coefficient storing units (CM_2, CM_3, CM_N). However, patterns for scanning the quantization coefficients in a block unit which are respectively stored in N coefficient storing units, are different from each other. FIG. 7 shows an embodiment of each other's different scanning patterns. A scanning pattern of FIG. 7A has a scanning orientation of 0 degrees, FIG. 7B shows a scanning pattern having a scanning orientation of 30 degrees, and FIG. 7C is a scanning pattern having a scanning orientation of 45 degrees. In channels of variable-length-coding with various scanning patterns, N accumulators ($ACCM_1$-$ACCM_N$) respectively provide the accumulated length data stored in each of the accumulated length storing units, to N input terminals of the minimum selector 52 for a minimum value of accumulated lengths. Each of the output terminals of N buffers (BF_1-BF_N), which stores the variable-length-coded data according to N types of scanning patterns, are separately connected to N input terminals of the selecting switch 54. The minimum selector 52 selects a minimum value among the accumulated length data input from each of the N accumulated length storing units (LM_1-LM_N). The minimum selector 52 outputs a scanning pattern data (D_{SCAN}) which represents scanning patterns of variable-length-coding channels with a selected minimum value of accumulated lengths, and provides a predetermined selecting control signal (SEL) corresponding to the selected minimum value of accumulated lengths to the selecting switch 54. The selecting switch 54 selects and outputs a variable-length-coded data (D_{VLC}) with the minimum value of accumulated lengths among the input data which are respectively input to N input terminals.

Whenever a minimum value is selected, that is, the variable-length-coding of every block data is completed, the minimum selector 52 generates a reset signal (RST), thereby resetting the N buffers (BF_1-BF_N) and the N accumulated length storing units (LM_1-LM_N). The variable-length-coded data (D_{VLC}) and the scanning pattern data (D_{SCAN}), which are output from the variable length coder, are transmitted to the receiver and supplied to a decoder.

FIG. 6 shows an embodiment of a variable length decoder in accordance with the present invention. Referring to FIG. 6, the input variable-length-coded data (D_{VLC}) are input to a variable length decoder 61 are transformed to the [run level] symbol according to a variable-length-decoding map. Moreover, the scanning pattern data (D_{SCAN}) transmitted from the coder are input to a scanning pattern selector 62 which stores each of the scanning addresses corresponding to various scanning patterns (1, N scans). The scanning pattern selector 62 selects and outputs scan addresses ($ADDR_S$) corresponding to the input scanning pattern data (D_{SCAN}). A run level decoder 63 transforms the [run level] symbols input from the variable length decoder 61 into a two-dimensional array of quantization coefficients according to the scan addresses (ADD_S) input from the scanning pattern selector 62. Then, the quantization coefficients are provided to a dequantizer.

As described above, the variable-length-coding system in accordance with the present invention variable-length-codes every block data according to diverse scanning patterns, and then transmits both a scanning pattern which minimizes the length of variable-length-coded data and variable-length-coded data according to the scanning pattern. At that time,

the variable-length-decoding system in accordance with the present invention variable-length-decodes the transmitted variable-length-coded data according to the same scanning pattern as utilized in the process of variable-length-coding. As a result, the system for variable-length-coding and variable-length-decoding can further compress the transmission data.

While the present invention has been illustrated and described in connection with two-dimensional data, the present invention can be applied to a coding and decoding system which utilizes multi-dimensional data.

What is claimed is:

1. A method of decoding data, comprising the steps of:

transforming variable length coded data into symbol data;

converting said symbol data into quantization coefficients by run level decoding said symbol data; and

scanning said quantization coefficients in accordance with a specific scanning pattern selected from a plurality of scanning patterns in response to scan pattern data.

2. The method of decoding data according to claim 1, wherein the step of scanning comprises transforming said quantization coefficients into two-dimensional quantization coefficients.

3. The method of decoding data according to claim 2, wherein said two-dimensional quantization coefficients are quantization coefficients stored at memory locations based on said specific scanning pattern such that said quantization coefficients stored at said memory locations correspond to a two-dimensional array of said quantization coefficients.

4. The method of decoding data according to claim 1, further comprising the step of dequantizing said quantization coefficients after said scanning step.

5. The method of decoding data according to claim 1, wherein said scan pattern data indicates one of a plurality of scanning patterns including a zigzag scanning pattern and another scanning pattern.

6. The method of decoding data according to claim 5, wherein said another scanning pattern is an alternate scanning pattern.

7. A decoding apparatus comprising:

a variable length decoder for transforming variable length coded data into symbol data; and

a run level decoder for converting said symbol data into quantization coefficients and for scanning said quantization coefficients in accordance with a specific scanning pattern selected from a plurality of scanning patterns in response to scan pattern data.

8. The decoding apparatus as recited in claim 7, wherein said run level decoder transforms said quantization coefficients into two-dimensional quantization coefficients when scanning said quantization coefficients.

9. The method of decoding data according to claim 8, wherein said two-dimensional quantization coefficients are quantization coefficients stored at memory locations based on said specific scanning pattern such that said quantization coefficients stored at said memory locations correspond to a two-dimensional array of said quantization coefficients.

10. The decoding apparatus as recited in claim 7, further comprising:

a dequantizer for dequantizing said coefficients after said coefficients are scanned.

11. The decoding apparatus as recited in claim 7, further comprising:

a storage device for storing a plurality of scanning patterns; and

means for outputting a scanning order in accordance with said specific scanning pattern among said plurality of scanning patterns.

12. The decoding apparatus as recited in claim 11, wherein said plurality of scanning patterns includes a zigzag scanning pattern and an alternate scanning pattern.

13. A decoding apparatus comprising:

means for transforming variable length coded data into symbol data;

means for converting said symbol data into quantization coefficients by run level decoding said symbol data; and

means for scanning said quantization coefficients in accordance with a specific scanning pattern selected from a plurality of scanning patterns in response to scan pattern data.

14. The decoding apparatus as recited in claim 13, wherein said means for scanning said quantization coefficients transforms said quantization coefficients into two-dimensional quantization coefficients.

15. The method of decoding data according to claim 14, wherein said two-dimensional quantization coefficients are quantization coefficients stored at memory locations based on said specific scanning pattern such that said quantization coefficients stored at said memory locations correspond to a two-dimensional array of said quantization coefficients.

16. The decoding apparatus as recited in claim 13, further comprising:

means for dequantizing said quantization coefficients after said quantization coefficients are scanned.

17. The decoding apparatus as recited in claim 13, further comprising:

a storage means for storing a plurality of scanning patterns; and

means for outputting a scanning order in accordance with said specific scanning pattern among said plurality of scanning patterns.

18. The decoding apparatus as recited in claim 17, wherein said plurality of scanning patterns includes a zigzag scanning pattern and an alternate scanning pattern.

19. A method of decoding data, comprising the steps of:

transforming variable length coded data into symbol data by variable length decoding said data, said symbol data having a run value and a level value; and

transforming quantization coefficients in accordance with a specific scanning pattern selected from a plurality of scanning patterns in response to scan pattern data, wherein the values of said quantization coefficients are determined in accordance with said run value and said level value of said symbol data.

20. The method of decoding data according to claim 19, wherein said transforming step is accomplished with a run level decoder.

21. The method of decoding data according to claim 19, wherein said transformed quantization coefficients are two-dimensional quantization coefficients.

22. The method of decoding data according to claim 21, wherein said two-dimensional quantization coefficients are quantization coefficients stored at memory locations based on said specific scanning pattern such that said quantization coefficients stored at said memory locations correspond to a two-dimensional array of said quantization coefficients.

23. The method of decoding data according to claim 19, further comprising the step of dequantizing said quantization coefficients after said transforming step.

24. The method of decoding data according to claim 19, wherein said scan pattern data indicates one of a plurality of scanning patterns including a zigzag scanning pattern and another scanning pattern.

25. The method of decoding data according to claim 24, wherein said another scanning pattern is an alternate scanning pattern.

26. A method of decoding data, comprising the steps of;

transforming variable length coded data into symbol data by variable length decoding said data, each of said symbol data having a run value and a level value; and

transforming quantization coefficients in accordance with a specific scanning pattern selected from a plurality of scanning patterns in response to scan pattern data;

wherein the value of each of said quantization coefficient is determined in accordance with said run value and said level of said symbol data.

27. A method of decoding data, comprising the steps of:

transforming variable length coded data into symbol data by variable length decoding said data, each of said symbol data having a run value and a level value;

determining quantization coefficients in accordance with said run value and said level value; and

transforming quantization coefficients in accordance with a specific scanning pattern selected from a plurality of scanning patterns in response to scan pattern data.

28. A decoding apparatus comprising:

a variable length decoder for transforming variable length coded data into symbol data, said symbol data having a run value and a level value; and

a transforming device for transforming quantization coefficients in accordance with a specific scanning pattern selected from a plurality of scanning patterns in response to scan pattern data, wherein the values of said quantization coefficients are determined in accordance with said run value and said level value of said symbol data.

29. The decoding apparatus as recited in claim 28, wherein said transforming device transforms said quantization coefficients into two-dimensional quantization coefficients.

30. The method of decoding data according to claim 29, wherein said two-dimensional quantization coefficients are quantization coefficients stored at memory locations based on said specific scanning pattern such that said quantization coefficients stored at said memory locations correspond to a two-dimensional array of said quantization coefficients.

31. The decoding apparatus as recited in claim 28, further comprising:

a dequantizer for dequantizing said coefficients after said coefficients are transformed.

32. The decoding apparatus as recited in claim 28, further comprising:

a storage device for storing a plurality of scanning patterns; and

means for outputting a scanning order in accordance with said specific scanning pattern among said plurality of scanning patterns.

33. The decoding apparatus as recited in claim 32, wherein said plurality of scanning patterns includes a zigzag scanning pattern and an alternate scanning pattern.

34. A decoding apparatus comprising:

means for transforming variable length coded data into symbol data, said symbol data having a run value and a level value; and

means for transforming quantization coefficients in accordance with a specific scanning pattern selected from a plurality of scanning patterns in response to scan pattern data, wherein the values of said quantization coefficients are determined in accordance with said run value and said level value of said symbol data.

35. The decoding apparatus as recited in claim 34, wherein said transformed quantization coefficients are two-dimensional quantization coefficients.

36. The method of decoding data according to claim 35, wherein said two-dimensional quantization coefficients are quantization coefficients stored at memory locations based on said specific scanning pattern such that said quantization coefficients stored at said memory locations correspond to a two-dimensional array of said quantization coefficients.

37. The decoding apparatus as recited in claim 34, further comprising:

means for dequantizing said coefficients after said coefficients are transformed.

38. The decoding apparatus as recited in claim 34, further comprising:

means for storing a plurality of scanning patterns; and

means for outputting a scanning order in accordance with said specific scanning pattern among said plurality of scanning patterns.

39. The decoding apparatus as recited in claim 38, wherein said plurality of scanning patterns includes a zigzag scanning pattern and an alternate scanning pattern.

40. A method of decoding data, comprising the steps of:

converting variable length coded data into symbol data;

transforming said symbol data into quantization coefficients by run level decoding said symbol data; and

scanning said quantization coefficients in accordance with a specific scanning pattern selected from a plurality of scanning patterns in response to scan pattern data.

41. The method of decoding data according to claim 40, wherein the step of scanning comprises transforming said quantization coefficients into two-dimensional quantization coefficients.

42. The method of decoding data according to claim 41, wherein said two-dimensional quantization coefficients are quantization coefficients stored at memory locations based on said specific scanning pattern such that said quantization coefficients stored at said memory locations correspond to a two-dimensional array of said quantization coefficients.

43. The method of decoding data according to claim 40, further comprising the step of dequantizing said quantization coefficients after said scanning step.

44. The method of decoding data according to claim 40, wherein said scan pattern data indicates one of a plurality of scanning patterns including a zigzag scanning pattern and another scanning pattern.

45. The method of decoding data according to claim 44, wherein said another scanning pattern is an alternate scanning pattern.

* * * * *

Exhibit 9

US006680975B1

(12) **United States Patent**
Jeong et al.

(10) **Patent No.: US 6,680,975 B1**
(45) **Date of Patent: *Jan. 20, 2004**

(54) **SIGNAL ENCODING AND DECODING SYSTEM AND METHOD**

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(73) Assignee: **Samsung Electronics Co., Ltd.**, Kyonggi-Do (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 376 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **09/703,649**

(22) Filed: **Nov. 2, 2000**

Related U.S. Application Data

(63) Continuation of application No. 08/024,305, filed on Mar. 1, 1993, now Pat. No. 6,263,026.

(30) **Foreign Application Priority Data**

Feb. 29, 1992 (KR) 92-3398

(51) **Int. Cl.**[7] **H04N 7/12**
(52) **U.S. Cl.** **375/240.23**
(58) **Field of Search** 375/240.23, 240.24, 375/240.25, 240.26, 240.62, 246, 253; 348/400.1, 423.1; 382/245–246

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,144,547	A		3/1979	Stoffel 358/133
4,754,336	A		6/1988	Nishizawa 358/133
4,821,119	A		4/1989	Gharavi 348/402
4,985,766	A		1/1991	Morrison et al. 358/136
5,045,938	A		9/1991	Sugiyama 358/133
5,057,917	A		10/1991	Shalkauser et al. 358/135
5,073,820	A		12/1991	Nakagawa et al. 358/133
5,107,345	A		4/1992	Lee 358/136
5,136,371	A		8/1992	Savatier et al. 358/135
5,218,435	A	*	6/1993	Lim et al. 375/240.16
5,227,878	A		7/1993	Puri et al. 348/416
5,253,055	A	*	10/1993	Civanlar et al. 375/240.24
5,260,781	A	*	11/1993	Soloff et al. 375/240.11
5,276,525	A	*	1/1994	Gharavi 382/245
5,321,776	A	*	6/1994	Shapiro 382/240
5,414,780	A	*	5/1995	Carnahan 382/276
5,757,973	A	*	5/1998	Wilkinson et al. 382/246

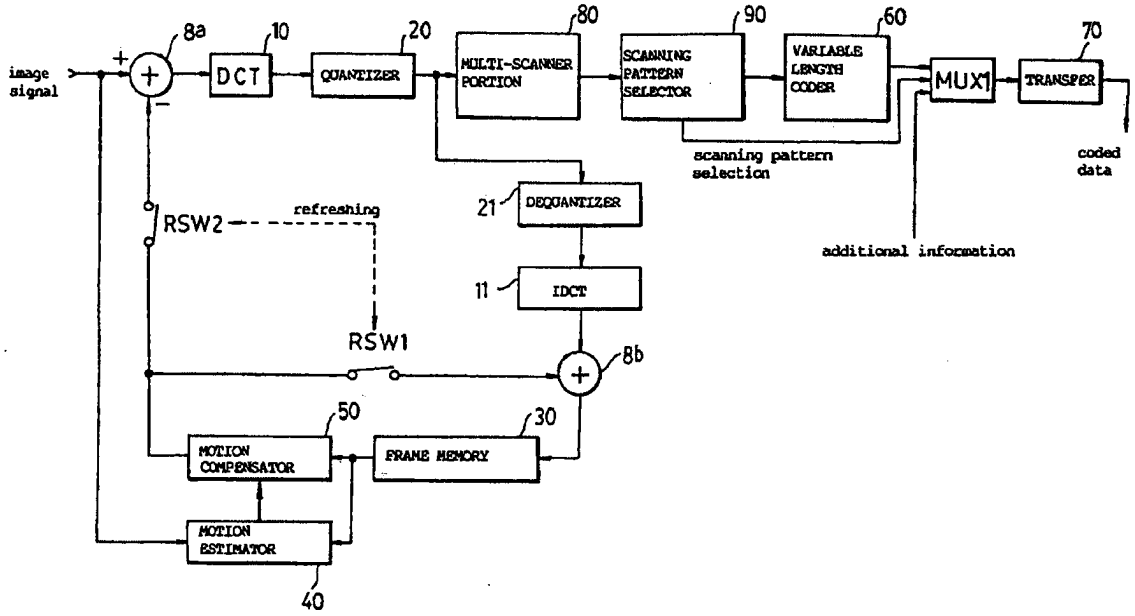
* cited by examiner

Primary Examiner—Vu Le
(74) *Attorney, Agent, or Firm*—Sughrue Mion, PLLC

(57) **ABSTRACT**

A multi-scanner scans a signal according to several different patterns. A scanning pattern selector determines which scanning pattern produced the most efficient coding result, for example, for runlength coding, and outputs a coded signal, coded most efficiently, and a selection signal which identifies the scanning pattern found to be most efficient.

93 Claims, 4 Drawing Sheets



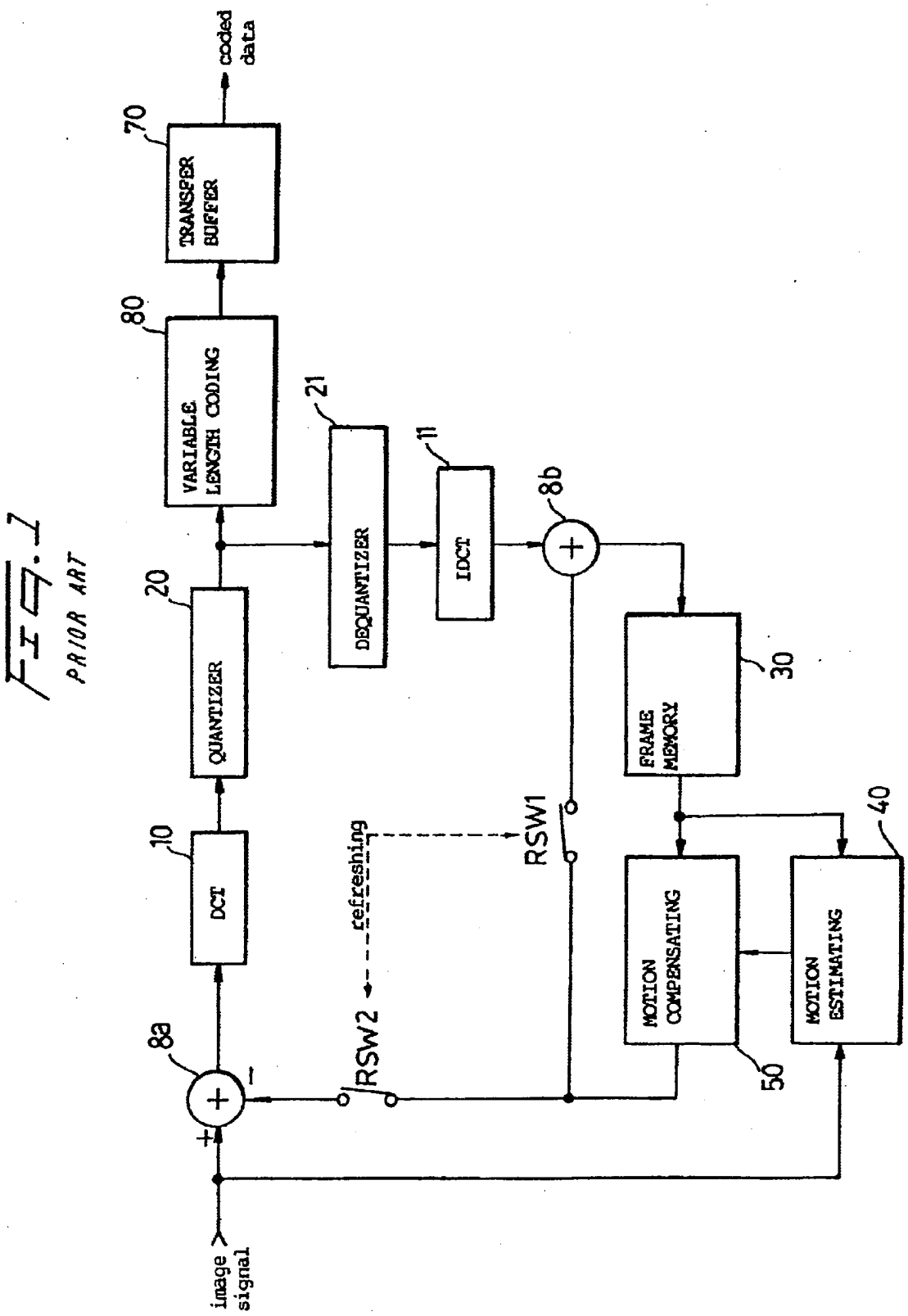


FIG. 1
PRIOR ART

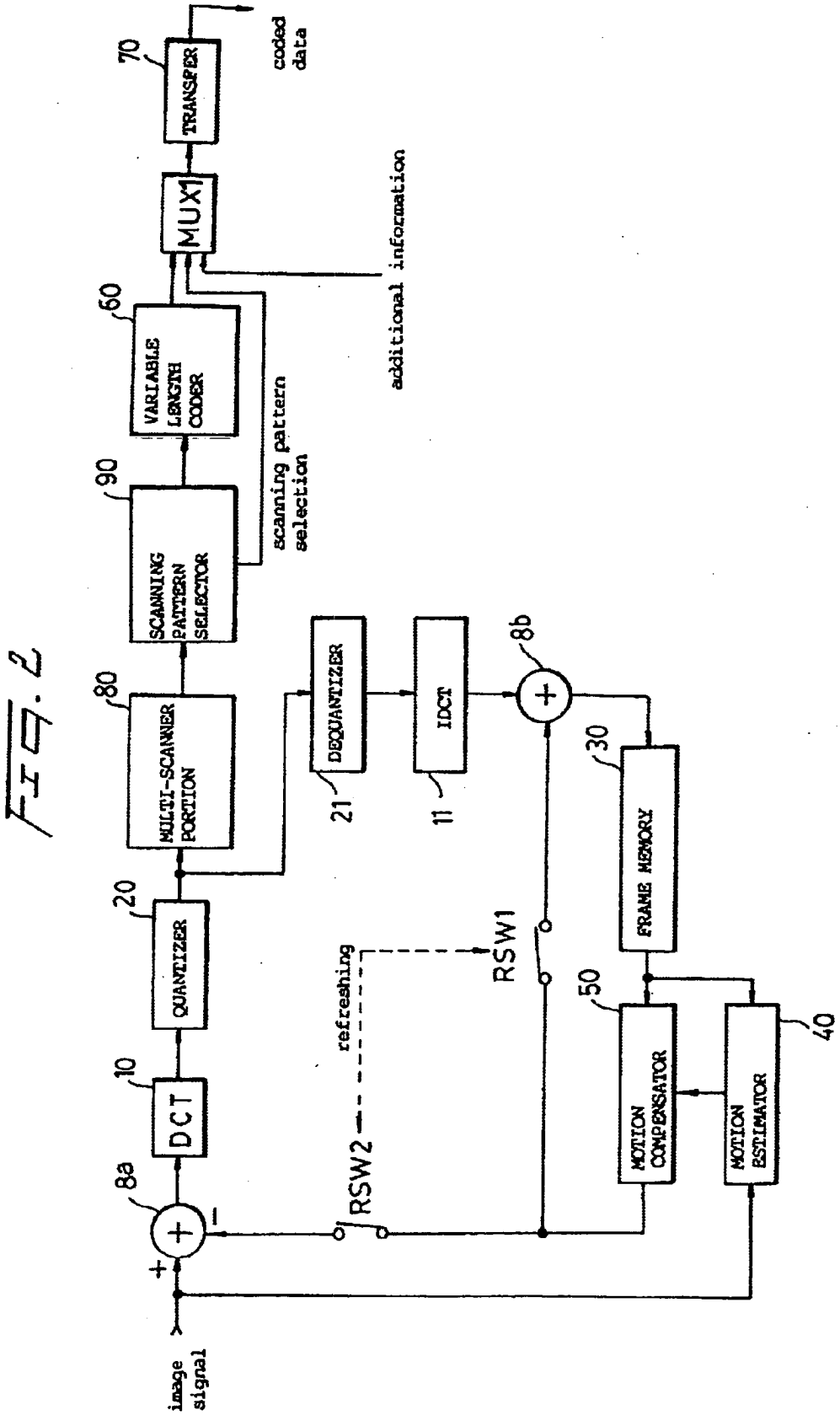

coded data
70
TRANSFER
MUX
additional information
60
VARIABLE LENGTH CODER
scanning pattern selection
90
SCANNING PATTERN SELECTOR
80
MULTI-SCANNER PORTION
DEQUANTIZER
21
IDCT
11
8b
30
FRAME MEMORY
20
QUANTIZER
RSW1
refreshing
RSW2
50
MOTION COMPENSATOR
40
MOTION ESTIMATOR
10
DCT
8a
image signal

FIG. 2

FIG. 3A

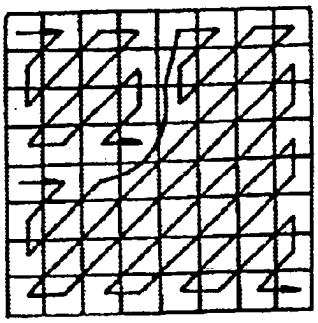


FIG. 3B

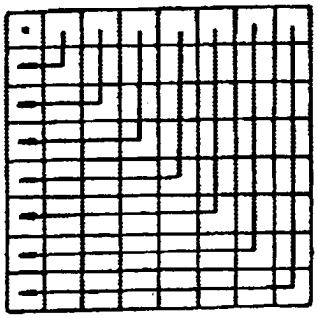


FIG. 3C

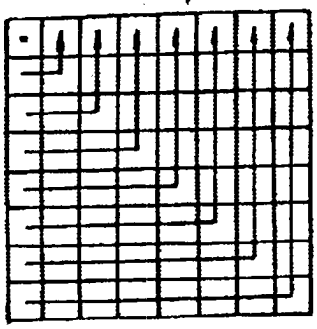


FIG. 3D

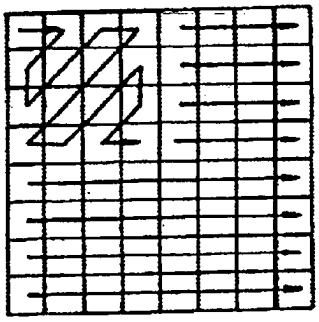


FIG. 3E

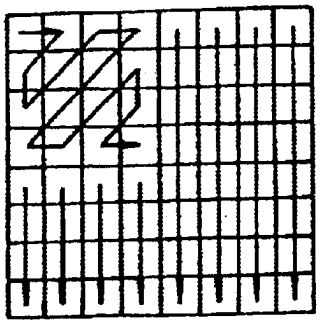


FIG. 3F

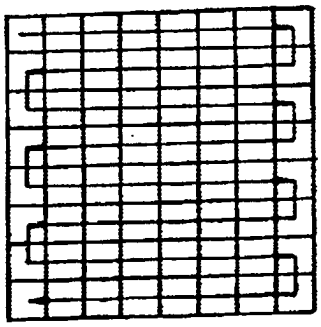


FIG. 3G

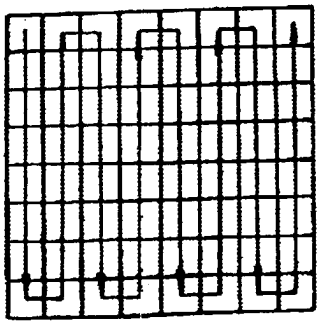
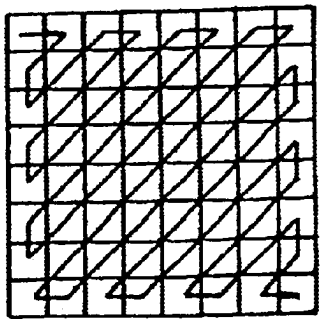


FIG. 3H



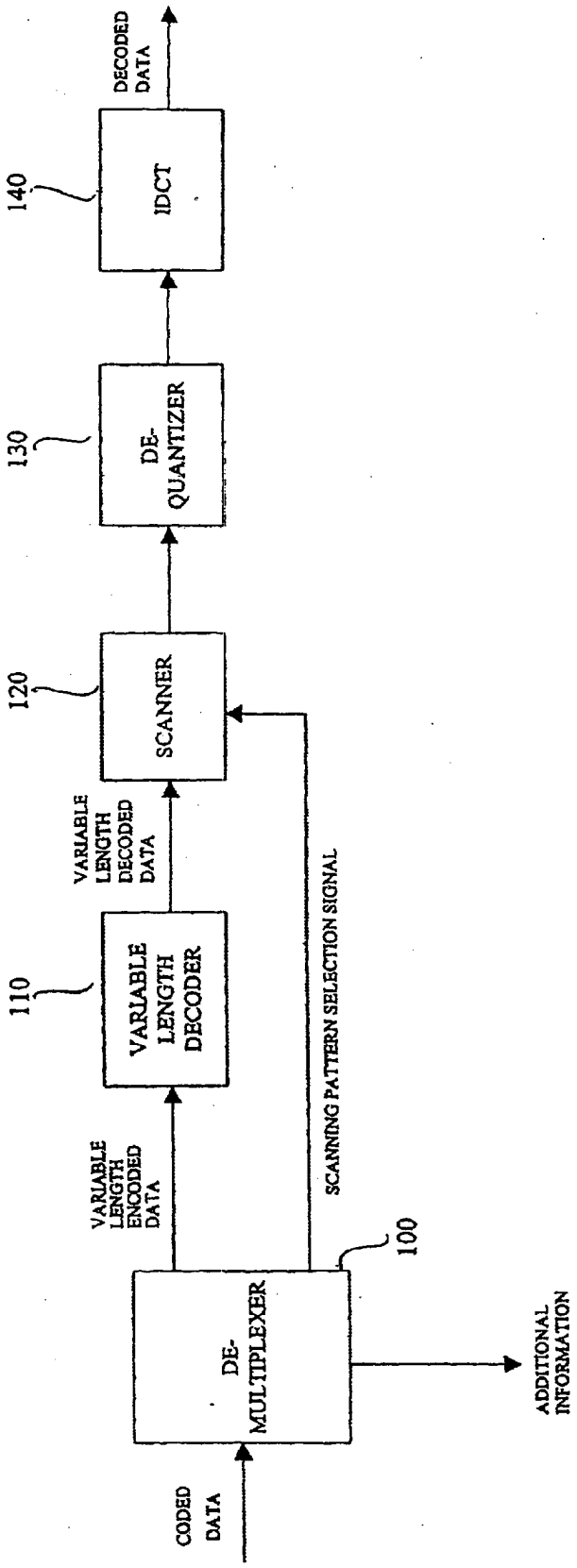

DECODED DATA
140
IDCT
130
DE-QUANTIZER
120
SCANNER
VARIABLE LENGTH DECODED DATA
110
VARIABLE LENGTH DECODER
VARIABLE LENGTH ENCODED DATA
SCANNING PATTERN SELECTION SIGNAL
100
DE-MULTIPLEXER
ADDITIONAL INFORMATION
CODED DATA

FIGURE 4

SIGNAL ENCODING AND DECODING SYSTEM AND METHOD

This is a Continuation of application Ser. No. 08/024,305 filed Mar. 1, 1993 now U.S. Pat. No. 6,263,026, the disclosure of which is incorporated herein by reference.

FIELD OF THE INVENTION

The present invention relates to a signal compressing system. A system according to the present invention is particularly suited for compressing image signals. The present disclosure is based on the disclosure in Korean Patent Application No. 92-3398 filed Feb. 29, 1992, which disclosure is incorporated herein by reference.

BACKGROUND OF THE INVENTION

Image signals may be compressed by motion-compensated interframe discrete cosine transform (DCT) coding such as is defined by a MPEG (Moving Picture Expert Group) international standard. This form of signal compression has attracted much attention in the field of high definition television (HDTV).

FIG. 1 is a block diagram of such a conventional motion-compensated interframe DCT coder. In the shown coder, an image signal is divided into a plurality of sub-blocks. The sub-blocks are all of the same size, for example 8×8, 16×16, ... A motion estimator **40** produces a motion vector, defined by the difference between the current image signal and a one-frame delayed image signal, output by a frame memory **30**. The motion vector is supplied to a motion compensator **50** which compensates the delayed image signal from the frame memory **30** on the basis of the motion vector. A first adder **8***a* serves to produce the difference between the present frame and the delayed, motion compensated frame. A discrete cosine transform portion **10** processes the difference signal, output by the first adder **8***a*, for a sub-block. The motion estimator **40** determines the motion vector by using a block matching algorithm.

The discrete cosine transformed signal is quantized by a quantizer **20**. The image signal is scanned in a zig-zag manner to produce a runlength coded version thereof. The runlength coded signal comprises a plurality of strings which include a series of "0"s, representing the run length, and an amplitude value of any value except "0".

The runlength coded signal is dequantized by a dequantizer **21**, inversely zig-zag scanned and inversely discrete cosine transformed by an inverse discrete cosine transforming portion **11**. The transformed image signal is added to the motion-compensated estimate error signal by a second adder **8***b*. As a result the image signal is decoded into a signal corresponding to the original image signal.

Refresh switches RSW1, RSW2 are arranged between the adders **8***a*, **8***b* and the motion compensator **40** so as to provide the original image signal free from externally induced errors.

The runlength coded signal is also supplied to a variable length coder **60** which applies a variable length coding to the runlength coded image signal. The variable length coded signal is then output through a FIFO transfer buffer **70** as a coded image signal.

In motion-compensated adaptive DCT coding, the interframe signal can be easily estimated or coded by way of motion compensation, thereby obtaining a high coding efficiency, since the image signal has a relatively high correlation along the time axis. That is, according to the afore-mentioned method, the coding efficiency is high because most of the energy of a discrete cosine transformed signal is compressed at the lower end of its spectrum, resulting in long runs of "0"s in the runlength coded signal.

However, the scanning regime of the afore-mentioned method does not take account of differences in the spectrum of the motion-compensated interframe DCT signal with time.

A method is known wherein one of a plurality of reference modes is previously selected on the basis of the difference between the present block and that of a previous frame and the image signal is scanned by way of a scanning pattern under the selected mode and suitably quantized. With such a method, however, three modes are employed to compute the energies of the intermediate and high frequency components of the image signal in accordance with the interframe or the intraframe modes in order to determine the appropriate mode. This mode determining procedure is undesirable complicated.

SUMMARY OF THE INVENTION

According to the present invention, there is provided a signal compressing system, comprising coding means for scanning an input signal according to a plurality of different scanning patterns to provided coded versions thereof and selection means for selecting a said scanning pattern which produces efficient coding according to a predetermined criterion and outputting a scanning pattern signal identifying the selected scanning pattern.

Preferably, the input signal is an inherently two-dimensional signal, for example, an image signal.

Preferably, the coding means codes the input signal according to a runlength coding regime.

Preferably, the system includes a variable length coder to variably length code the coded signal, produced by scanning according to the selected scanning pattern.

Preferably, the system includes discrete cosine transformer means to produce said input signal. The transformer means may be a motion-compensated interframe adaptive discrete cosine transformer.

BRIEF DESCRIPTION OF THE DRAWINGS

An embodiment of the present invention will now be described, by way of example, with reference to FIGS. **2** and **3** of the accompanying drawings, in which:

FIG. **1** is a block diagram of a conventional adaptive interframe DCT coding system employing a motion compensating technique;

FIG. **2** is a block diagram of a coding system embodying the present invention; and

FIGS. **3**A–**3**H show various possible scanning patterns according to the present invention.

FIG. **4** is a block diagram of a decoding system according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. **2**, an input signal is divided into equal-sized sub-blocks, for example, 8×8, 16×16, ... A motion estimator **40** determines a motion vector by comparing the current frame and a one frame delayed signal from a frame memory **30**.

The motion vector is supplied to a motion compensator **60** which, in turn, compensates the delayed frame signal for

movement. A first adder **8***a* produces a difference signal representing the difference between the present frame and the delayed, motion-compensated frame. A DCT coder **10** DCT-codes the difference signal. The DCT coded image signal is quantized by a quantizer **20** and then dequantized by a dequantizer **21**. The dequantized signal is supplied to a second adder **8***b*, via IDCT **11**, which adds it to the output of the motion compensator **11**. This produces a signal corresponding to the original image signal.

The output of the motion compensator **50** is applied to the adders **8***a*, **8***b* by refresh switches RSW2 and RSW1, respectively.

The quantized image signal is also supplied to a multi-scanner **80** which scans it according to a plurality of predetermined patterns.

A scanner pattern selector **90** selects the scanning pattern which produces the minimum number of bits to represent the current sub-block. The scanning pattern selector also produces selection data which identifies the selected scanning pattern.

The image signal output by the scanning pattern selector **90** is variable length coded by a variable length coder **60**. The variable length coder **60** compresses the image signal output by the scanning pattern selector **90**. The variable length coder **60** operates such that a large proportion of the data samples are each represented by a small number of bits while a small proportion of the data samples are each represented by a large number of bits.

When a discrete cosine transformed image signal is quantized and runlength coded, the number of "0"s is increased over all, while the number of "0"s decreases as the magnitude of the signal increases. Accordingly, data compression is achieved because "0"can be represented by only a few bits and "255" can be represented by a relatively large number of bits.

Both the variable length coded signal and the selection data are supplied to a multiplexer MUX1 which multiplexes the variable length coded signal and the selection data, and optionally additional information such as teletext.

Since the variable length coded signal has data words of different lengths, a transfer buffer **70** is employed to temporarily store the multiplexed signal and output it at a constant rate.

The original image signal is reconstructed at a remote station by performing the appropriate inverse scanning of the runlength coded signal in accordance with the multiplexed scanning pattern selection data.

FIG. **4** shows a decoding system at a remote station that receives and extracts the encoded data. In FIG. **4**, demultiplexer **100** receives coded data and, in an operation inverse to that performed at the coding system, extracts the variable length encoded data, the scanning pattern information and the additional information that had been multiplexed together at the coding system. Variable length decoder **110** variable length decodes the variable length encoded data, and scanner **120** receives the variable length decoded data and reconstructs the original sub-block using a scanning pattern indicated by the extracted scanning pattern selection signal. The scanner would necessarily have to select one from a plurality pattern that was available for encoding. Using components having the same margin as dequantizers **21** and 1 DCT **11** in the encoder system, dequantizer **120** dequantizes the signal output from the scanner **120**, and inverse discrete cosine transformer **140** performs an inverse discrete cosine transform function on the output of dequantizer **130**, to output decoded data.

FIGS. **3**A to **3**H show possible scanning patterns employed by the multi-scanner **80**. Additional scanning patterns will be apparent to those skilled in the art. However, if the number of patterns becomes too large, the coding efficiency is degraded as the selection data word becomes longer.

As described above, according to the present invention, the quantized image signal is scanned according to various scanning patterns, and then the most efficient pattern is selected. A suitable measure of efficiency is the number of bits required to runlength code the image signal.

What is claimed is:

1. A video signal compression system, comprising:

a scanner which is operative to simultaneously scan a set of video spatial frequency coefficients of an individual sub-block according to a plurality of different scanning patterns to produce a plurality of sets of reordered coefficients;

a scanning pattern selector operative to select from the plurality of sets of reordered coefficients a set of reordered coefficients which produces the most efficient coding according to a predetermined criterion and to produce a pattern signal indicating the scanning pattern corresponding to the selected set of reordered coefficients; and

an entropy coder operative to entropy encode the selected set of reordered coefficients and output an entropy encoded signal.

2. The video signal compression system according to claim **1**, further comprising a combining unit which combines into one signal the pattern signal produced by said scanning pattern selector and the entropy encoded signal.

3. The video signal compression system according to claim **2** wherein said combining unit is a multiplexer.

4. The video signal compression system according to claim **3**, wherein said multiplexer receives additional information and multiplexes the additional information, the pattern signal and the entropy encoded signal.

5. The video signal compression system according to claim **4**, wherein the additional information is teletext information.

6. The video signal compression system according to claim **1**, wherein said scanner produces the plurality of sets of reordered coefficients according to a runlength coding regime.

7. The video signal compression system according to claim **1**, further comprising a discrete cosine transformer for use in generating the set of video spatial frequency coefficients.

8. The video signal compression system according to claim **1**, wherein said entropy encoder is a variable length coder.

9. A video signal compression system, comprising:

means for simultaneously scanning a set of video spatial frequency coefficients of an individual sub-block according to a plurality of different scanning patterns to produce a plurality of sets of reordered coefficients;

means for selecting a scanning pattern from the plurality of sets of reordered coefficients which produces a set of reordered coefficients having the most efficient coding according to a predetermined criterion and for outputting a pattern signal indicating the scanning pattern corresponding to the selected set of reordered coefficients; and

means for entropy encoding the selected set of reordered coefficients and for outputting an entropy encoded signal.

10. The video signal compression system according to claim 9, further comprising means for combining the pattern signal produced by said scanning pattern selector and the entropy encoded signal.

11. The video signal compression system according to claim 10, wherein said means for combining is a multiplexer.

12. The video signal compression system according to claim 11, wherein said multiplexer receives additional information and multiplexes the additional information, the pattern signal and the entropy encoded signal.

13. The video signal compression system according to claim 12, wherein the additional information is teletext information.

14. The video signal compression system according to claim 9, wherein said means for scanning produces the plurality of sets of reordered coefficients according to a runlength coding regime.

15. The video signal compression system according to claim 9, further comprising discrete cosine transformer means for use in generating the set of video spatial frequency coefficients.

16. The video signal compression system according to claim 9, wherein said means for entropy encoding is a variable length coder.

17. A decoder for decompressing a compressed video signal, the compressed video signal containing entropy encoded data representing a set of video spatial frequency coefficients of an individual sub-block which have been scanned using a selected one of a plurality of different scanning patterns to produce a set of reordered coefficients, and also containing a pattern signal indicating the selected one of the plurality of different scanning patterns, wherein the selected scanning pattern produces the most efficient coding according to a predetermined criterion, the decoder comprising:

an entropy decoder operative to decode the entropy encoded data and to output entropy decoded data; and

a scanner operative to scan the entropy decoded data according to the one selected pattern of the plurality of different scanning patterns as indicated by the pattern signal.

18. A decoder for decoding a coded data signal containing a compressed video signal and a pattern signal, the decoder comprising:

an entropy decoder to which is applied the compressed video signal, the compressed video signal including entropy encoded data representing a set of video spatial frequency coefficients of an individual sub-block which have been scanned using a specific pattern selected from a plurality of different scanning patterns to produce a set of reordered coefficients, wherein the specific scanning pattern produces the most efficient coding according to a predetermined criterion, said entropy decoder being operative to entropy decode the entropy encoded data and to output entropy decoded data; and

a scanner operative to scan the entropy decoded data responsive to the pattern signal, and to output scanned data, wherein the pattern signal indicates the specific scanning pattern.

19. The decoder according to claim 18 wherein the coded data signal further includes additional information.

20. The decoder according to claim 19, wherein the entropy encoded data, the pattern signal and the additional information are multiplexed together as part of the coded data signal, and wherein said decoder further includes a demultiplexer which demultiplexes the entropy encoded data, the pattern signal and the additional information.

21. The decoder according to claim 18 wherein the entropy encoded data and the pattern signal are multiplexed together as part of the coded data signal.

22. The decoder according to claim 18, wherein the entropy encoded data is encoded according to a variable length encoding regime.

23. The decoder according to claim 18, wherein the scanner scans the entropy decoded data according to a runlength decoding regime.

24. The decoder of claim 18, further comprising a dequantizer which dequantizes the scanned data output by said scanner and outputs dequantized data.

25. The decoder of claim 24, further comprising an inverse discrete cosine transformer which inverse discrete cosine transforms the dequantized data output by said dequantizer.

26. A decoder, comprising:

decoding means to which is applied a coded data signal including a compressed video signal, the compressed video signal including entropy encoded data representing a set of video spatial frequency coefficients of an individual sub-block which have been scanned using a selected one of a plurality of different scanning patterns to produce a set of reordered coefficients and, the coded data signal also including a pattern signal indicating the selected one of the plurality of different scanning patterns, wherein the selected scanning pattern produces the most efficient coding according to a predetermined criterion, said decoding means for entropy decoding the entropy encoded data and for outputting entropy decoded data; and

scanning means for scanning the entropy decoded data according to the selected pattern indicated by the pattern signal.

27. The decoder according to claim 26, wherein the coded data signal further includes additional information.

28. The decoder according to claim 26, wherein the entropy encoded data and the pattern signal are multiplexed together as part of the coded data signal, and wherein said decoder further includes a demultiplexing means for demultiplexing the entropy encoded data, the pattern signal and the additional information.

29. The decoder according to claim 26, wherein the entropy encoded data is encoded according to a variable length encoding regime.

30. The decoder according to claim 26, wherein the scanning means scans the entropy decoded data according to a runlength decoding regime.

31. The decoder according to claim 26, further comprising dequantizing means for dequantizing the scanned data output by said scanning means and for outputting dequantized data.

32. The decoder according to claim 31, further comprising inverse discrete cosine transformer means for inverse discrete cosine transforming the dequantized data output by said dequantizing means.

33. A decoding apparatus for decoding a coded data signal which includes entropy encoded data representing a set of video spatial frequency coefficients of an individual sub-block, the set of video spatial frequency coefficients having been reordered from an original order according to a scanning pattern selected from a plurality of scanning patterns, the coded data signal also including a pattern signal indicating the selected scanning pattern, the decoding apparatus comprising:

an entropy decoder which entropy decodes the entropy encoded data to produce entropy decoded data; and

a scanning unit which receives the entropy decoded data and returns the set of video spatial frequency coefficients of an individual sub-block to the original order according to the selected scanning pattern indicated in the pattern signal.

34. The decoding apparatus according to claim 33, wherein the coded data signal further includes additional information.

35. The decoding apparatus according to claim 34, wherein the entropy encoded data, the pattern signal and the additional information are multiplexed together as part of the coded data signal and wherein said decoding apparatus further includes a demultiplexer which demultiplexes the entropy encoded data, the pattern signal and the additional information.

36. The decoding apparatus according to claim 33, wherein the entropy encoded data and the pattern signal are multiplexed together as part of the coded data signal.

37. The decoding apparatus according to claim 33, wherein the entropy encoded data is encoded according to a variable length encoding regime.

38. The decoding apparatus according to claim 33, wherein the scanning unit scans the entropy decoded data according to a runlength decoding regime.

39. The decoding apparatus of claim 3, further comprising a dequantizer which dequantizes the scanned data output by said scanning unit and outputs dequantized data.

40. The decoding apparatus of claim 39, further comprising an inverse discrete cosine transformer which inverse discrete cosine transforms the dequantized data output by said dequantizer.

41. A method of compressing a video signal, comprising:

simultaneously scanning a set of video spatial frequency coefficients of an individual sub-block according to a plurality of different scanning patterns to produce a plurality of sets of reordered coefficients;

selecting a scanning pattern from the plurality of sets of reordered coefficients which produces a set of reordered coefficients having the most efficient coding according to a predetermined criterion and outputting a pattern signal indicating the scanning pattern corresponding to the selected set of reordered coefficients; and

entropy encoding the selected set of reordered coefficients and outputting an entropy encoded signal.

42. The method of claim 41, further comprising a step of multiplexing the pattern signal produced by said scanning pattern selector and the entropy encoded signal.

43. The method of claim 42, wherein said multiplexing step further includes receiving additional information and multiplexing the additional information, the pattern signal and the entropy encoded signal.

44. The method of claim 43, wherein the additional information is teletext information.

45. The method of claim 41, wherein said scanning step produces the plurality of sets of reordered coefficients according to a runlength coding regime.

46. The method of claim 41, wherein the set of video spatial frequency coefficients is generated using a discrete cosine transformer.

47. The method of claim 41, wherein said entropy encoding is variable length coding.

48. A method of decoding a compressed video signal, comprising:

receiving a coded data signal, the coded data signal including a compressed video signal having entropy encoded data representing a set of video spatial frequency coefficients of an individual sub-block which have been scanned using a selected one of a plurality of different scanning patterns to produce a set of reordered coefficients, the coded data signal also including a pattern signal indicating the selected one of the plurality of different scanning patterns, wherein the selected scanning pattern produces the most efficient coding according to a predetermined criterion;

entropy decoding the entropy encoded data and outputting entropy decoded data; and

scanning the entropy decoded data according to the selected pattern indicated by the pattern signal and outputting scanned data.

49. The method of claim 48, wherein the coded data signal further includes additional information.

50. The method of claim 49, wherein the entropy encoded data, the pattern signal and the additional information are multiplexed together as part of the coded data signal and wherein said decoding step further includes demultiplexing the entropy encoded data, the pattern signal and the additional information.

51. The method of claim 48, wherein the entropy encoded data and the pattern signal are multiplexed together as part of the coded data signal.

52. The method of claim 48, wherein the entropy encoded data is encoded according to a variable length encoding regime.

53. The method of claim 48, wherein the scanning step comprises scanning the entropy decoded data according to a runlenth decoding regime.

54. The method of claim 48, further comprising a step of dequantizing the scanned data output by said scanning step and outputting dequantized data.

55. The method of claim 54, further comprising a step of inverse discrete cosine transforming the dequantized data output by said dequantizing step.

56. A method of decoding a coded data signal which includes entropy encoded data representing a set of video spatial frequency coefficients of an individual sub-block, the set of video spatial frequency coefficients having been reordered from an original order according to a scanning pattern selected from a plurality of scanning patterns, the coded data signal also including a pattern signal indicating the selected scanning pattern, the method comprising:

entropy decoding the entropy encoded data to produce entropy decoded data; and

scanning the entropy decoded data and returning the set of video spatial frequency coefficients of an individual sub-block to the original order according to the selected scanning pattern indicated in the pattern signal.

57. The method of claim 56, wherein the coded data signal further includes additional information.

58. The method of claim 57, wherein the entropy encoded data, the pattern signal and the additional information are multiplexed together as part of the coded data signal and wherein the method further comprises demultiplexing the entropy encoded data, the pattern signal and the additional information.

59. The method of claim 56, wherein the entropy encoded data and the pattern signal are multiplexed together as part of the coded data signal.

60. The method of claim 56, wherein the entropy encoded data is encoded according to a variable length encoding regime.

61. The method of claim 56, wherein in said scanning step the entropy decoded data is scanned according to a runlength decoding regime.

62. The method of claim 56, further comprising a step of dequantizing the scanned data output by said scanning step and outputting dequantized data.

63. The method of claim 62, further comprising a step of inverse discrete cosine transforming the dequantized data output by said dequantizing step.

64. A video signal compression system, comprising:

a multi-scanner which is operative to simultaneously scan a set of video spatial frequency coefficients of an individual sub-block according to a plurality of different scanning patterns to produce a plurality of sets of reordered coefficients;

a scanning pattern selector operative to select from the plurality of sets of reordered coefficients a set of reordered coefficients which produces the most efficient coding according to a predetermined criterion and to produce a pattern signal indicating the scanning pattern corresponding to the selected set of reordered coefficients;

an entropy coder operative to entropy encode the selected set of reordered coefficients and to output entropy encoded data;

an entropy decoder operative to decode the entropy encoded data and to output entropy decoded data; and

a scanner which is operative to scan the entropy decoded data according to the scanning pattern corresponding to the selected set of reordered coefficients as indicated by the pattern signal and to output scanned data.

65. The video signal compression system according to claim 64, further comprising:

a combiner which combines additional information with the entropy encoded data and the pattern signal to produce a combined signal; and

a unit which receives the combined signal, extracts the additional information therefrom, and transmits the entropy encoded data to said entropy decoder and the pattern signal to said scanner.

66. The video signal compression system according to claim 65, wherein said combiner is a multiplexer and said unit which receives the combined signal is a demultiplexer.

67. The video signal compression system according to claim 65, wherein the additional information is teletext information.

68. The video signal compression system according to claim 64, wherein said multi-scanner produces the plurality of sets of reordered coefficients according to a runlength coding regime.

69. The video signal compression system according to claim 64, further comprising a discrete cosine transformer for use in generating the set of video spatial frequency coefficients.

70. The video signal compression system according to claim 64, wherein said entropy encoder is a variable length coder.

71. The video signal compression system according to claim 64, wherein the scanner scans the entropy decoded data according to a runlength decoding regime.

72. The video signal compression system according to claim 64, further comprising a dequantizer which dequantizes the scanned data output by said scanner and outputs dequantized data.

73. The video signal compression method according to claim 72, further comprising an inverse discrete cosine transformer which inverse discrete cosine transforms the dequantized data output by said dequantizer.

74. A video signal compression system, comprising:

multi-scanning means for simultaneously scanning a set of video spatial frequency coefficients of an individual sub-block according to a plurality of different scanning patterns to produce a plurality of sets of reordered coefficients;

scanning pattern selecting means for selecting from the plurality of sets of reordered coefficients a set of reordered coefficients which produces the most efficient coding according to a predetermined criterion and for producing a pattern signal indicating the scanning pattern corresponding to the selected set of reordered coefficients;

entropy coding means for entropy encoding the selected set of reordered coefficients and outputting entropy encoded data;

entropy decoding means for decoding the entropy encoded data and outputting entropy decoded data; and

scanning means for scanning the entropy decoded data according to the scanning pattern corresponding to the selected set of reordered coefficients as indicated by the pattern signal and outputing scanned data.

75. The video signal compression system according to claim 74, further comprising:

combining means for combining additional information with the entropy encoded data and the pattern signal to produce a combined signal; and

de-coupling means for receiving the combined signal, extracting the additional information therefrom, and transmitting the entropy encoded data to said entropy decoding means and the pattern signal to said scanning means.

76. The video signal compression system according to claim 75, wherein said combining means is a multiplexer and said de-coupling means is a demultiplexer.

77. The video signal compression system according to claim 75, wherein the additional information is teletext information.

78. The video signal compression system according to claim 74, wherein said multi-scanning means produces the plurality of sets of reordered coefficients according to a runlength coding regime.

79. The video signal compression system according to claim 74, further comprising a discrete cosine transforming means for use in generating the set of video spatial frequency coefficients.

80. The video signal compression system according to claim 74, wherein said entropy encoding means is a variable length coder.

81. The video signal compression system according to claim 74, wherein said scanning means scans the entropy decoded data according to a runlength decoding regime.

82. The video signal compression system according to claim 74, further comprising dequantizing means for dequantizing the scanned data output by said scanning means and outputting dequantized data.

83. The video signal compression system according to claim 81, further comprising inverse discrete cosine transforming means for inverse discrete cosine transforming the dequantized data output by said dequantizing means.

84. A video signal compression method, comprising:

simultaneously scanning a set of video spatial frequency coefficients of an individual sub-block according to a plurality of different scanning patterns to produce a plurality of sets of reordered coefficients;

selecting from the plurality of sets of reordered coefficients a set of reordered coefficients which produces the

most efficient coding according to a predetermined criterion and producing a pattern signal indicating the scanning pattern corresponding to the selected set of reordered coefficients;

entropy encoding the selected set of reordered coefficients and outputting entropy encoded data;

decoding the entropy encoded data and outputting entropy decoded data; and

scanning the entropy decoded data according to the scanning pattern corresponding to the selected set of reordered coefficients as indicated by the pattern signal and outputting scanned data.

85. The video signal compression method according to claim **83**, further comprising steps of:

combining additional information with the entropy encoded data and the pattern signal to produce a combined signal; and

receiving the combined signal and extracting the additional information therefrom, the entropy encoded data therefrom for use in the decoding step, and the pattern signal therefrom for use in the step of scanning the entropy decoded data.

86. The video signal compression method according to claim **85**, wherein said combining step multiplexes the additional information with the entropy encoded data and the pattern signal to produce the combined signal and said extracting step de-multiplexes the additional information, the entropy encoded data, and the pattern signal.

87. The video signal compression method according to claim **85**, wherein the additional information is teletext information.

88. The video signal compression method according to claim **84**, wherein said step of scanning the set of video spatial frequency coefficients produces the plurality of sets of reordered coefficients according to a runlength coding regime.

89. The video signal compression method according to claim **84**, further comprising a step of generating the set of video spatial frequency coefficients by discrete cosine transformation.

90. The video signal compression method according to claim **84**, wherein said entropy encoding is variable length coding.

91. The video signal compression method according to claim **84**, wherein in said step of scanning the entropy decoded data, the entropy decoded data are scanned according to a runlength decoding regime.

92. The video signal compression method according to claim **84**, further comprising dequantizing the scanned data, output in said step of scanning the entropy decoded data, and outputting dequantized data.

93. The video signal compression method according to claim **92**, further comprising inverse discrete cosine transforming the dequantized data.

* * * * *

Exhibit 10

US007020204B2

(12) **United States Patent**
Auvray et al.

(10) **Patent No.: US 7,020,204 B2**
(45) **Date of Patent: Mar. 28, 2006**

(54) **ADAPTIVE METHOD OF ENCODING AND DECODING A SERIES OF PICTURES BY TRANSFORMATION, AND DEVICES FOR IMPLEMENTING THIS METHOD**

(75) Inventors: **Eric Auvray**, Orvault (FR); **Claude Perron**, Rennes (FR); **Alain Ferre**, Cesson Sevigne (FR)

(73) Assignee: **Thomson Licensing**, Boulogne-Billancourt (FR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 396 days.

(21) Appl. No.: **10/071,352**

(22) Filed: **Feb. 8, 2002**

(65) **Prior Publication Data**

US 2002/0110195 A1 Aug. 15, 2002

Related U.S. Application Data

(60) Division of application No. 09/978,376, filed on Oct. 17, 2001, now Pat. No. 6,563,875, which is a continuation of application No. 07/408,515, filed as application No. PCT/FR88/00649 on Dec. 30, 1988, now abandoned.

(30) **Foreign Application Priority Data**

Dec. 30, 1987 (FR) 87 18371

(51) **Int. Cl.**
H04N 7/12 (2006.01)

(52) **U.S. Cl.** **375/240.25**; 375/240.18; 375/240.24

(58) **Field of Classification Search** 375/240.12, 375/240.13, 240.24, 240.25; 348/400.1; 382/236, 238, 248, 250; 386/109, 111
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,761,613 A 9/1973 Limb 178/7.1
4,196,448 A 4/1980 Whitehouse et al. 358/135
4,217,609 A 8/1980 Hatori et al. 358/136

(Continued)

FOREIGN PATENT DOCUMENTS

EP 0 084 270 A3 7/1983

(Continued)

OTHER PUBLICATIONS

Gakkaishi, Terebijon, International Standardization of Colour Still Picture Coding, edited by Hiroshi Yasuda, The Journal of the Institute of the Television Engineers of Japan, vol. 41, No. 9 (Ser. No. 469), Sep. 20, 1987 pp. 815-820, translation attached.

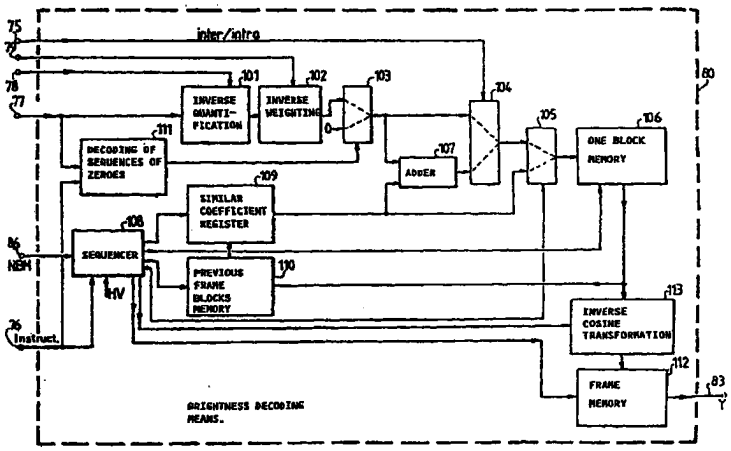
(Continued)

Primary Examiner—Vu Le
(74) *Attorney, Agent, or Firm*—Joseph S. Tripoli; Joseph J. Laks; Frank Y. Liao

(57) **ABSTRACT**

A method and a device for coding and decoding a sequence of images or pictures is disclosed. One exemplary embodiment disclosed codes by dividing each picture into blocks of picture elements. Each element of a block being represented by a digital value. Two types of coding are utilized in order to reduce the amount of data; inter-coding, which takes into account a corresponding block in a previous picture and intra coding, which is independent from a previous picture. Blocks being thus coded so that a further reduction of data is obtained by transmitting high spatial frequencies with less weight than low spatial frequencies. This is accomplished with the use of weighting coefficients. Weighting coefficients are variable as a function of the quantity of information to be transmitted.

1 Claim, 8 Drawing Sheets



U.S. PATENT DOCUMENTS

4,245,248	A		1/1981	Netravali et al. 358/136
4,302,775	A	*	11/1981	Widergren et al. 375/240.06
4,394,774	A		7/1983	Widergren et al. 382/56
4,447,886	A		5/1984	Meeker 364/725
4,541,012	A		9/1985	Tescher 358/133
4,581,638	A		4/1986	Chiariglione et al. 358/135
4,583,114	A		4/1986	Catros 358/13
4,672,427	A		6/1987	Rzeszewski 358/13
4,672,441	A		6/1987	Hoelzlwimmer et al. ... 358/135
4,707,738	A		11/1987	Ferre et al. 358/135
4,734,767	A	*	3/1988	Kaneko et al. 348/400.1
4,901,075	A		2/1990	Vogel 341/63
4,918,523	A	*	4/1990	Simon et al. 375/240.23
4,969,055	A		11/1990	Oberjatzas et al. 360/32

FOREIGN PATENT DOCUMENTS

EP	0 189 703 A1	8/1986
FR	2 589 020	4/1987
JP	60-194875	10/1985
JP	62-272632	11/1987

OTHER PUBLICATIONS

Kaneko, Masahide et al., "Selection of Transformed Coefficients to be Quantized in Hybrid Coding Method", edited by Masahide Kaneko et al., National Convention Record (1987), The Institute of Electronics, Information and Communication Engineers (Part 5), p. 33, translation attached.

H. Bacchi et al., "Real-Time Orthogonal Transformation Of Colour-Television Pictures", Philips Technical Review, vol. 38, No. 4/5. 1978/1979, pp. 119-129.

A. G. Tescher, "Adaptive Transform Coding Of Color Images At Low Rates", National Telecommunications Conference, Houston, Nov. 30-Dec. 4, 1980, vol. 2, pp. 36.3.1-36.3.4, IEEE, New York.

* cited by examiner

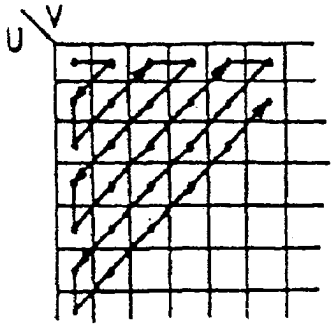


FIG.1

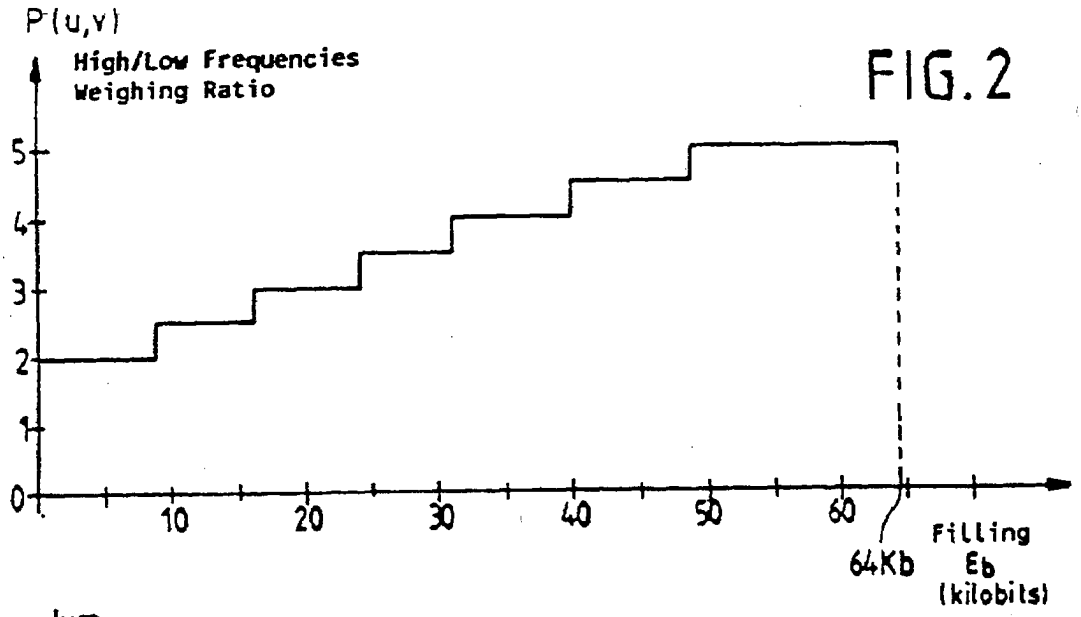


FIG.2

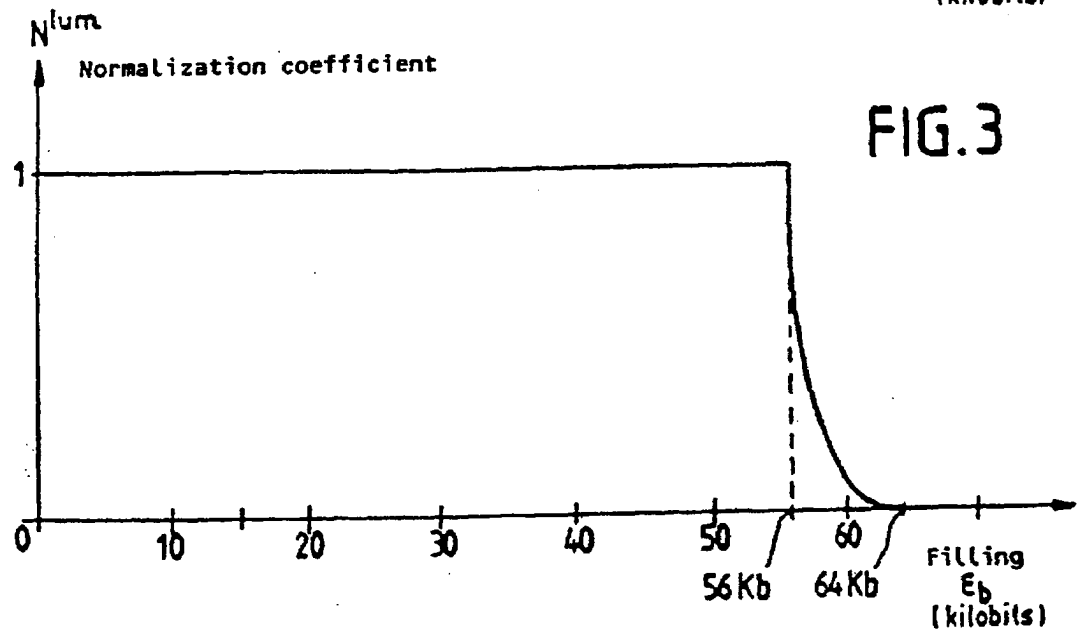


FIG.3

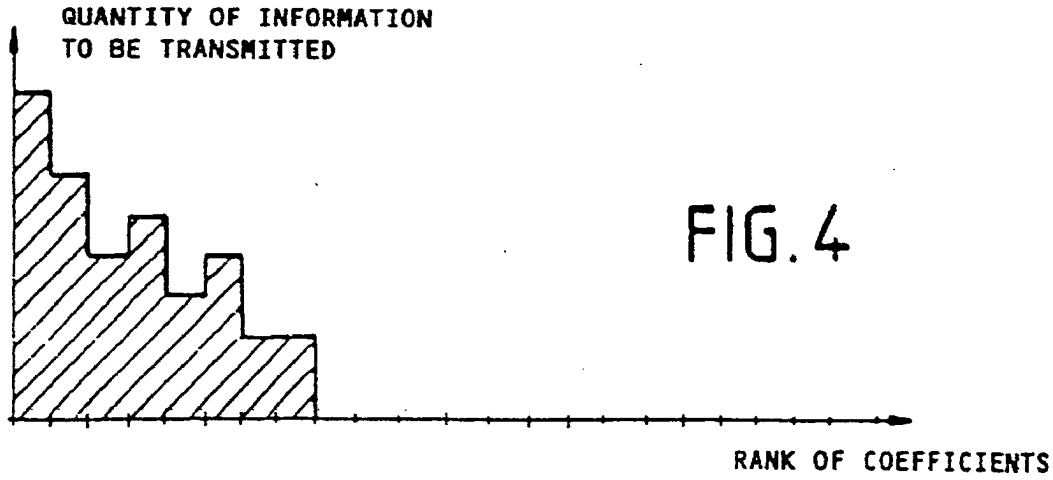


FIG. 4

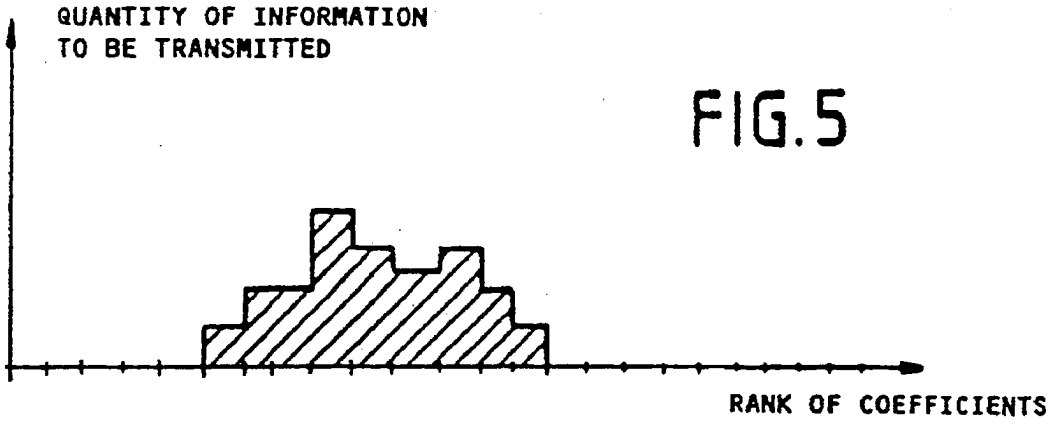


FIG. 5

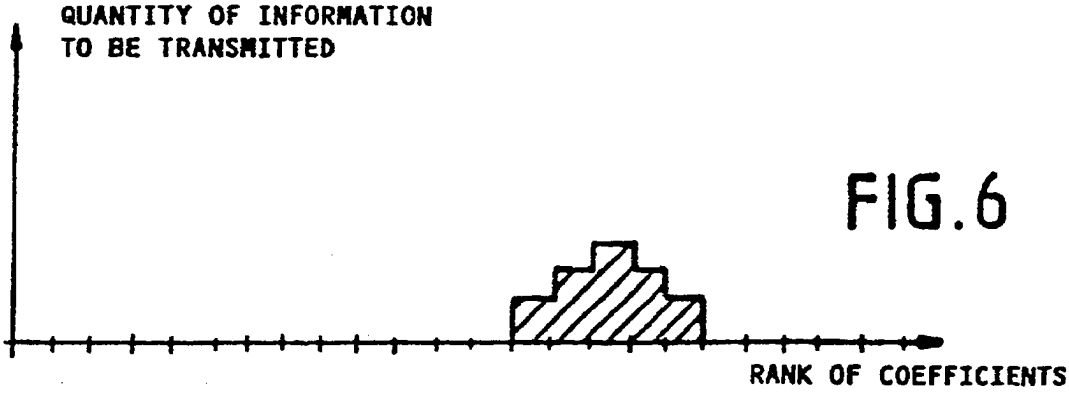


FIG. 6

FIG.7

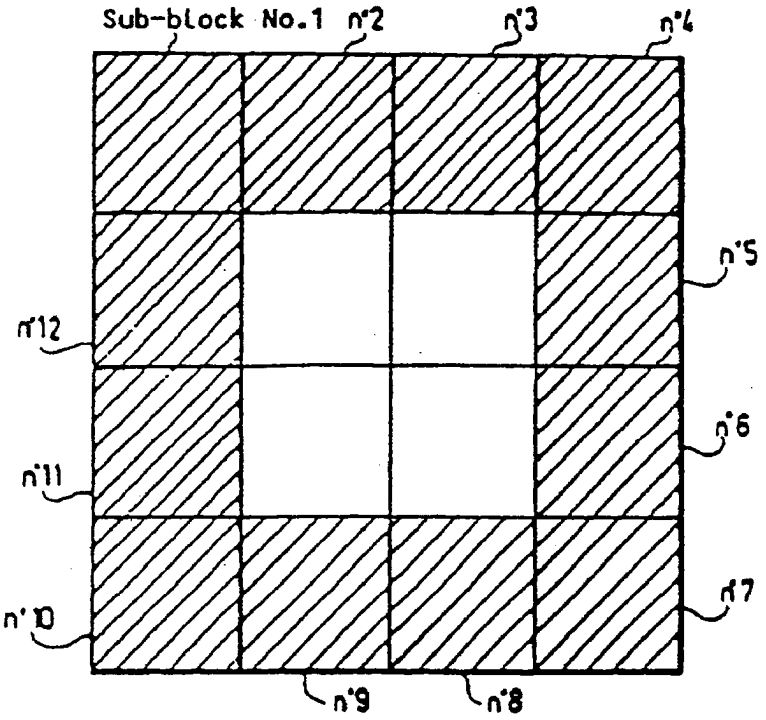
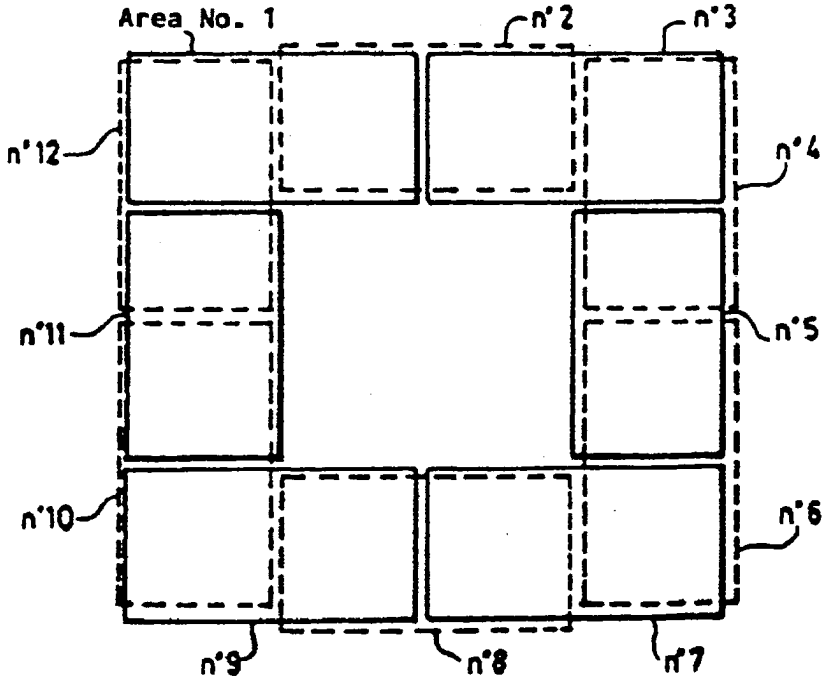

Sub-block No.1
n°2
n°3
n°4
n°5
n°6
n°7
n°8
n°9
n°10
n°11
n°12

FIG.8


Area No. 1
n°2
n°3
n°4
n°5
n°6
n°7
n°8
n°9
n°10
n°11
n°12

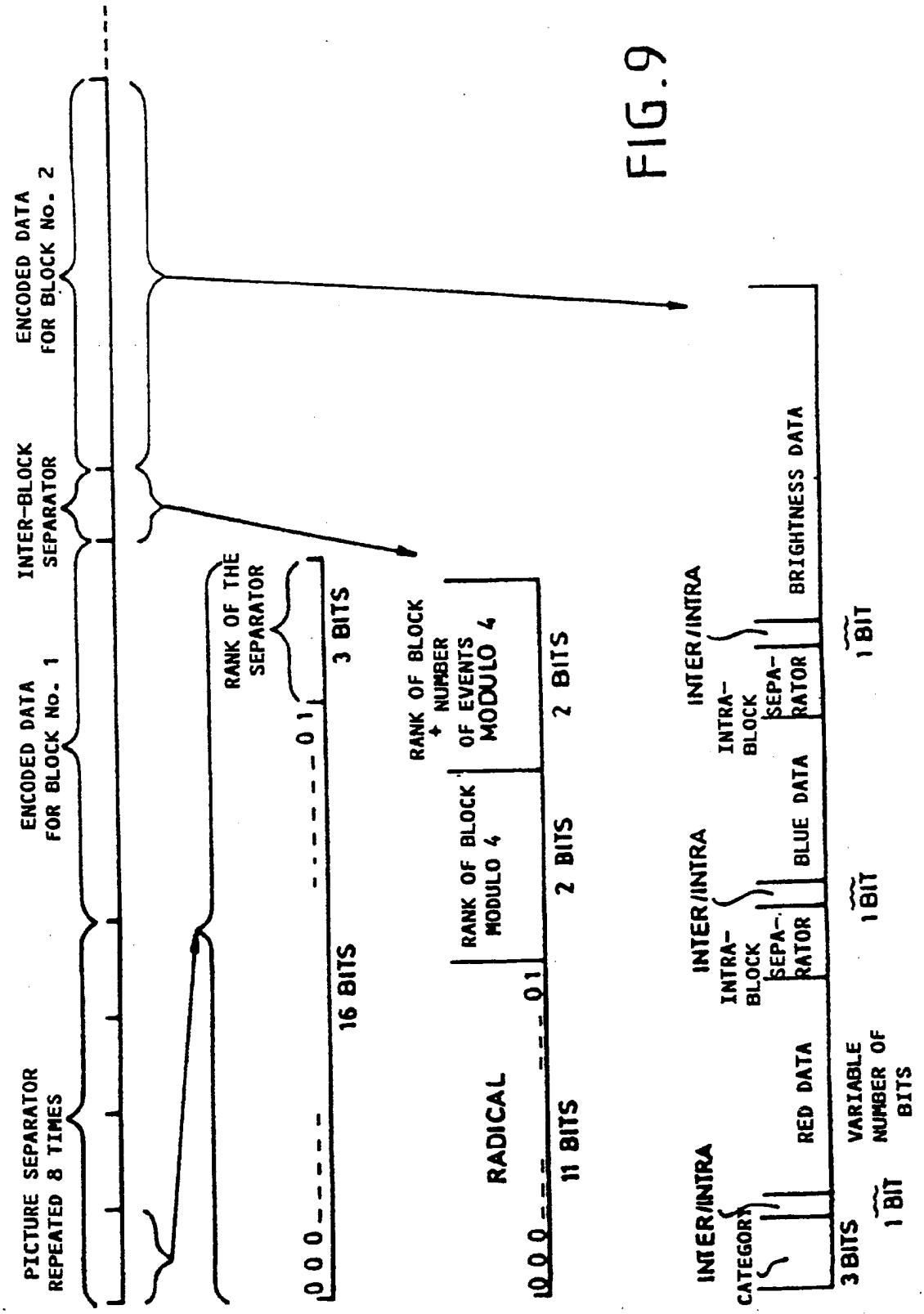

PICTURE SEPARATOR REPEATED 8 TIMES
ENCODED DATA FOR BLOCK No. 1
INTER-BLOCK SEPARATOR
ENCODED DATA FOR BLOCK No. 2
000
16 BITS
RANK OF THE SEPARATOR
01
3 BITS
RADICAL
11 BITS
RANK OF BLOCK MODULO 4
2 BITS
RANK OF BLOCK + NUMBER OF EVENTS MODULO 4
2 BITS
INTER/INTRA CATEGORY
3 BITS
RED DATA
VARIABLE NUMBER OF BITS
INTRA-BLOCK SEPA-RATOR
1 BIT
INTER/INTRA
BLUE DATA
INTRA-BLOCK SEPA-RATOR
1 BIT
INTER/INTRA
BRIGHTNESS DATA
1 BIT

FIG. 9

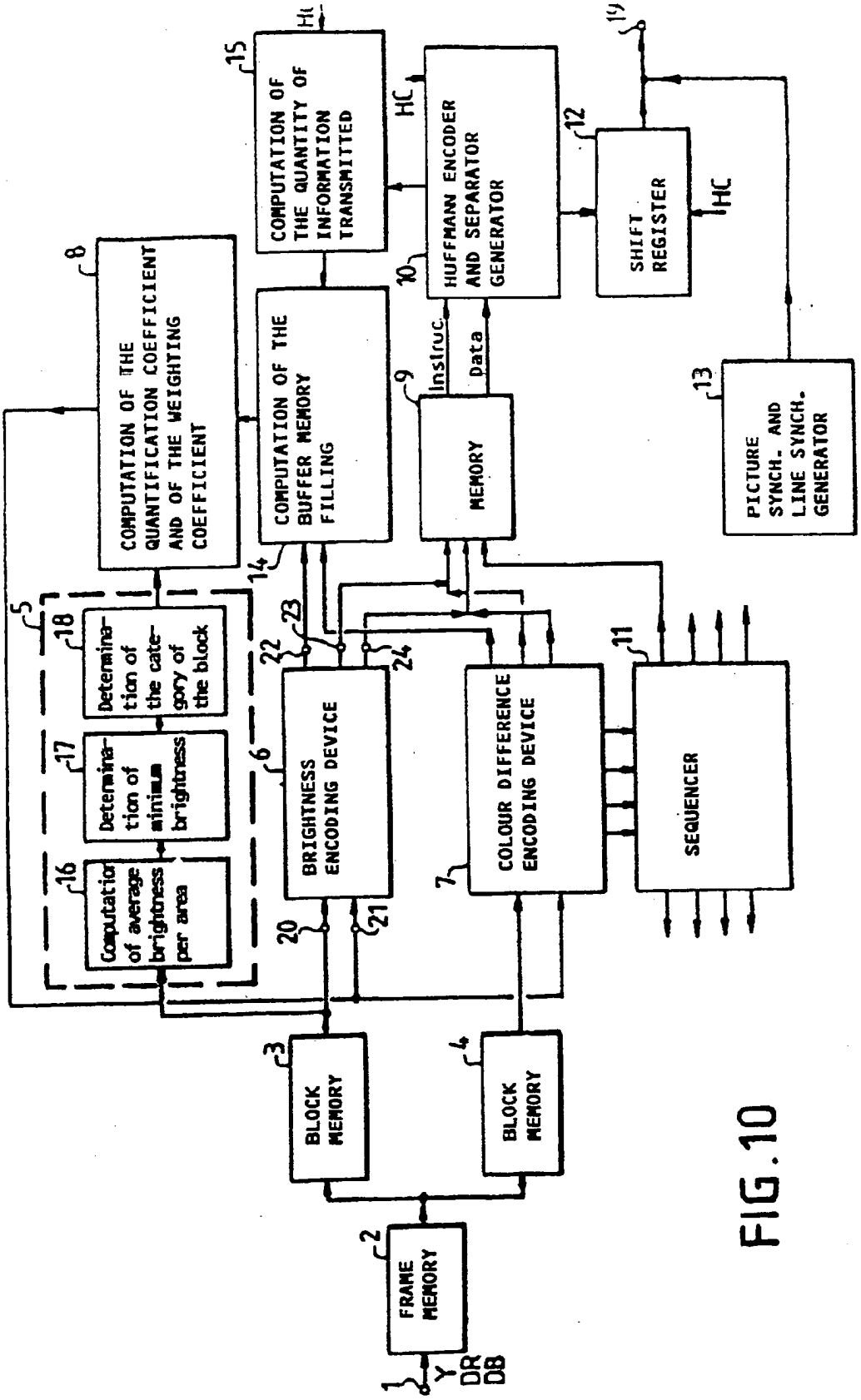

COMPUTATION OF THE QUANTIFICATION COEFFICIENT AND OF THE WEIGHTING COEFFICIENT
COMPUTATION OF THE QUANTITY OF INFORMATION TRANSMITTED
COMPUTATION OF THE BUFFER MEMORY FILLING
HUFFMANN ENCODER AND SEPARATOR GENERATOR
SHIFT REGISTER
MEMORY
PICTURE SYNCH. AND LINE SYNCH. GENERATOR
Determination of the category of the block
Determination of minimum brightness
Computation of average brightness per area
BRIGHTNESS ENCODING DEVICE
COLOUR DIFFERENCE ENCODING DEVICE
SEQUENCER
BLOCK MEMORY
BLOCK MEMORY
FRAME MEMORY
Y
DR
DB
HC
Instruc.
Data

FIG.10

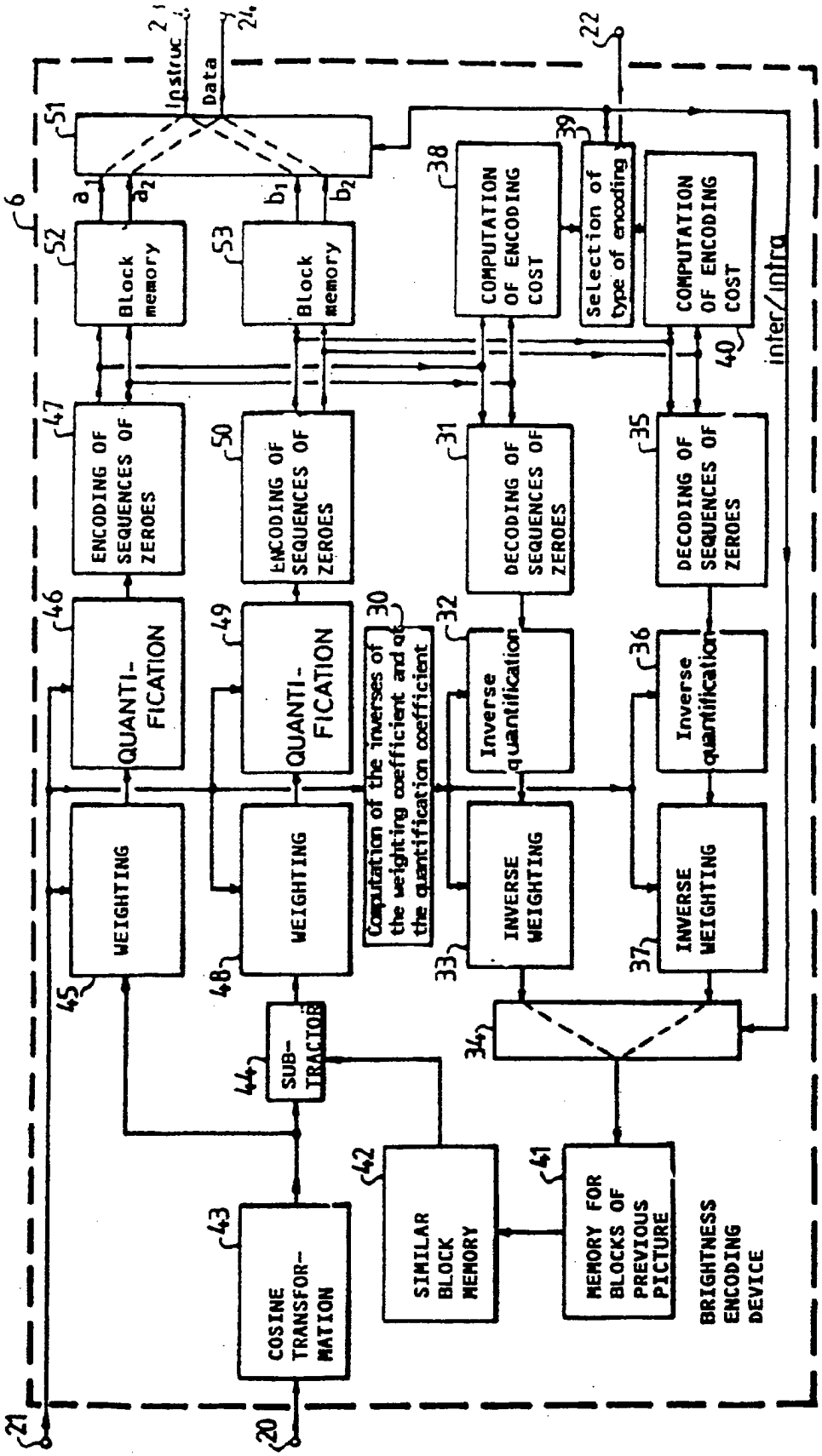

Instruc.
Data
inter/intra
Block memory
Block memory
COMPUTATION OF ENCODING COST
Selection of type of encoding
COMPUTATION OF ENCODING COST
ENCODING OF SEQUENCES OF ZEROES
ENCODING OF SEQUENCES OF ZEROES
DECODING OF SEQUENCES OF ZEROES
DECODING OF SEQUENCES OF ZEROES
QUANTI-FICATION
QUANTI-FICATION
Computation of the inverses of the weighting coefficient and of the quantification coefficient
Inverse quantification
Inverse quantification
WEIGHTING
WEIGHTING
INVERSE WEIGHTING
INVERSE WEIGHTING
SUB-TRACTION
COSINE TRANSFOR-MATION
SIMILAR BLOCK MEMORY
MEMORY FOR BLOCKS OF PREVIOUS PICTURE
BRIGHTNESS ENCODING DEVICE

FIG. 11

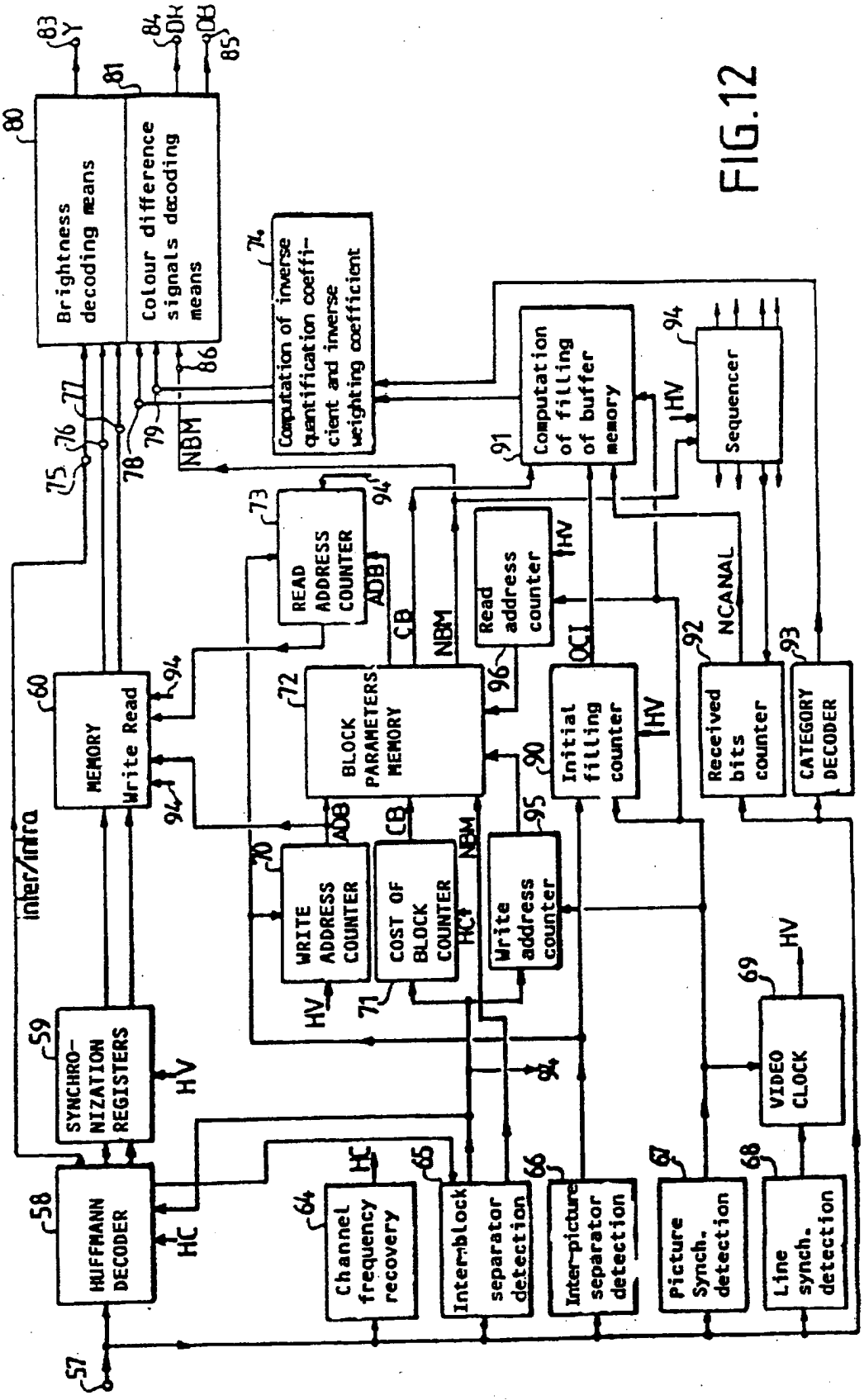

Brightness decoding means
Colour difference signals decoding means
Computation of inverse quantification coefficient and inverse weighting coefficient
Computation of filling of buffer memory
Sequencer
READ ADDRESS COUNTER
Read address counter
MEMORY Write Read
BLOCK PARAMETERS MEMORY
Initial filling counter
Received bits counter
CATEGORY DECODER
WRITE ADDRESS COUNTER
COST OF BLOCK COUNTER
Write address counter
SYNCHRO-NIZATION REGISTERS
VIDEO CLOCK
HUFFMANN DECODER
Channel frequency recovery
Interblock separator detection
Inter-picture separator detection
Picture Synch. detection
Line synch. detection
inter/intra
NBM
CB
ADB
HV
HC
NCANAL
OCI

FIG.12

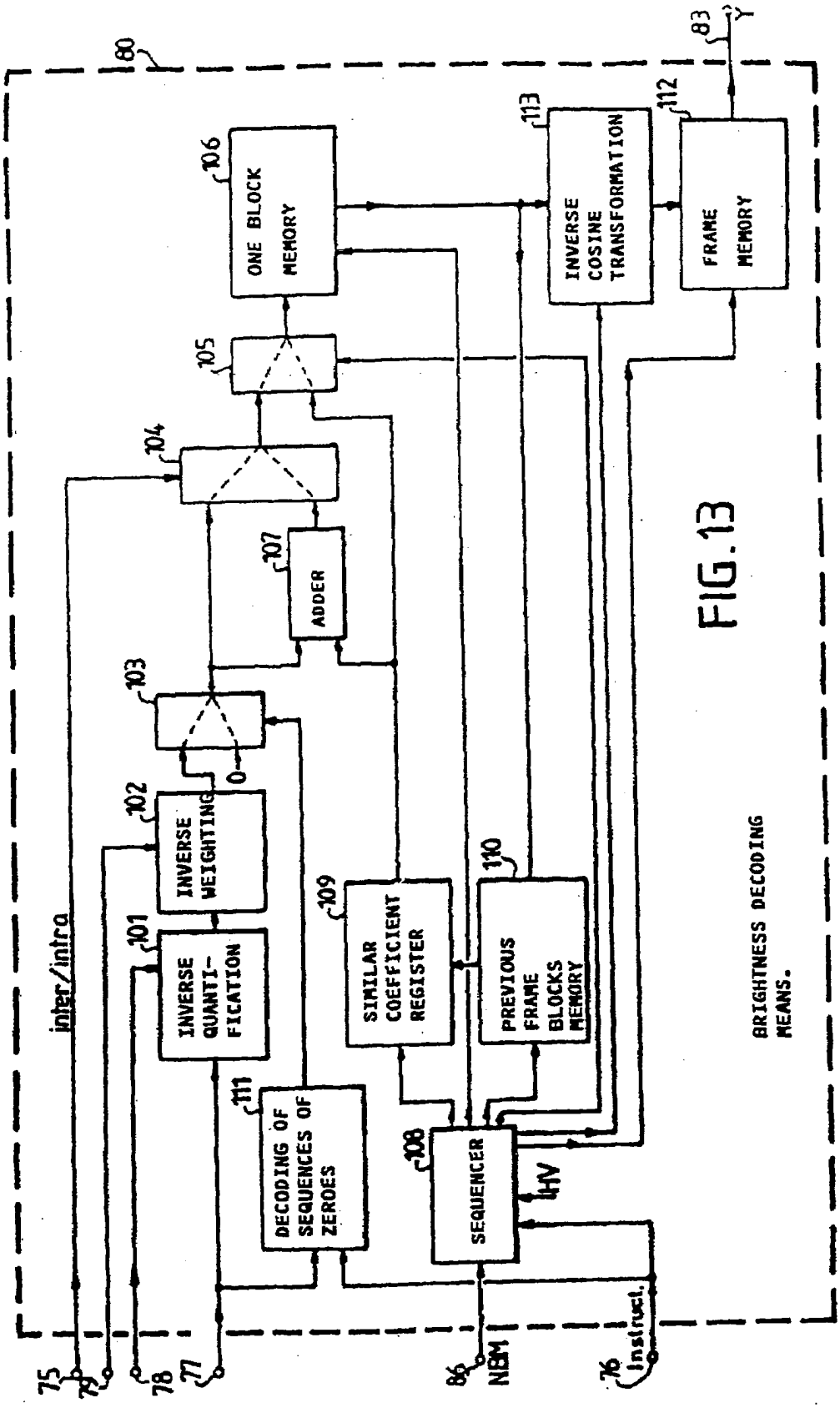

80
83
Y
112
113
106
ONE BLOCK MEMORY
INVERSE COSINE TRANSFORMATION
FRAME MEMORY
105
104
107
ADDER
103
0
102
INVERSE WEIGHTING
101
INVERSE QUANTI-FICATION
inter/intra
109
SIMILAR COEFFICIENT REGISTER
110
PREVIOUS FRAME BLOCKS MEMORY
111
DECODING OF SEQUENCES OF ZEROES
108
SEQUENCER
HV
BRIGHTNESS DECODING MEANS.
75
79
78
77
86
NBM
76
Instruct.

FIG. 13

ADAPTIVE METHOD OF ENCODING AND DECODING A SERIES OF PICTURES BY TRANSFORMATION, AND DEVICES FOR IMPLEMENTING THIS METHOD

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a divisional of application Ser. No. 09/978,376, filed Oct. 17, 2001, now U.S. Pat. No. 6,563,875, which is a continuation of application Ser. No. 07/408,515, filed Nov. 30, 1995 now abandoned claiming the benefit and priority of PCT International Application No. PCT/FR88/00649, filed Dec. 30, 1988, and French Application No. 87 18371, filed Dec. 30, 1987.

The invention relates to an adaptive method of encoding and decoding a series of pictures by transformation, and devices for implementing this method. The object of such a method is to reduce the quantity of information to be transmitted, or to be stored, when pictures have been digitized. It is applicable, for example, to digital video transmission systems or to digital video recorders.

It is known to encode a digitized picture by using a two-dimensional transformation of the cosine or Fourier, or Hadamard, or Haar, or Karhunen-Loeve type. Such an encoding consists in: dividing each picture into blocks of picture elements, each picture element being represented by a digital value which is the value of its brightness or of a colour difference: applying the transformation to each block in order to obtain a matrix of values called the transformation coefficients of the block; and in transmitting these transformation coefficients in an encoded form, for example using a Huffmann code. The decoding then consists in: decoding the Huffmann code words in order to obtain the transformation coefficients; then in restoring the digital values representing each picture element by applying, to the transformation coefficients corresponding to a block of picture elements, the two-dimensional transformation which is the inverse of that used for the encoding. The transformations used in practice are transformations for which there exists fast algorithms, for example the cosine transformation.

The French Patent Application 2,575,351 describes an adaptive method of encoding and decoding consisting in:

dividing each picture into blocks of picture elements;

applying the cosine transformation to each block, the latter being represented by a block of brightness values in order to obtain a block of transformation coefficient;

determining, for each block, if it represents a scene with much movement or little movement;

transmitting the value of the transformation coefficients of the block if the latter represents a scene with much movement, or transmitting the differences in the value of these coefficients with respect to the coefficients of the similar block in the previous picture, if the block represents a scene with little movement;

transmitting an information indicating the type of encoding used for each block, these two types of encoding being called respectively intra-picture encoding and inter-picture encoding. The coefficients or differences of coefficients are transmitted in the form of Huffmann code words.

According to this known method, the decoding consists, before applying the inverse transformation, in determining a value of the transformation coefficients of each block representing a scene with little movement, by adding the difference in value of each of its coefficients respectively to the value of the coefficients of the similar block in the previous picture.

According to this known method, the encoding furthermore consists in applying a weighting to the values of the coefficients or to the values of the differences of coefficients, with a greater weight for the coefficients or the differences of coefficients corresponding to the low spatial frequencies of the picture, with respect to the coefficients or to the differences of the coefficients corresponding to the high spatial frequencies of the picture; and in quantifying according to a linear scale the weighted coefficients and differences of coefficients. The quantification step is variable according to the quantity of information to be transmitted. This is equivalent to multiplying all of the coefficients or all the differences of transformation coefficients of a block by a same coefficient called the quantification coefficient which is variable according to the quantity of information to be transmitted for the blocks of picture elements encoded before the block concerned; and in retaining only the whole part of the result of the multiplication.

The information to be transmitted is stored in a buffer memory enabling a transmission at a constant rate. A regulating device supplies a value of the quantification coefficient which continuously diminishes while the buffer memory is filling and which continuously increases while the buffer memory is emptying.

Naturally, the decoding furthermore consists in multiplying each transmitted coefficient value or each transmitted difference of coefficients value, by a coefficient equal to the inverse of the weighting coefficient used for the encoding; and then in multiplying it by a coefficient equal to the inverse of the quantification coefficient used for the encoding.

When a series of pictures represents a scene containing much movement, the quantity of information to be transmitted is high, and consequently the quantification coefficient is small in order to reduce the amplitude of the values of the transformation coefficients or differences of transformation coefficients to be transmitted. Furthermore, the weighting coefficients give greater weight to the transformation coefficients corresponding to the low spatial frequencies of the picture in order to transmit the essential information of the picture while sacrificing less essential information which corresponds to the high spatial frequencies of the picture.

When the series of pictures represents a scene with little movement or a static scene, the encoding of each block is of the inter-picture type in order to exploit the correlation existing between these successive pictures. From one picture to the next, the values of the differences of transformation coefficients of similar blocks have a decreasing amplitude and the quantity of information to be transmitted tends to reduce. The regulation then reacts by increasing the quantification coefficient. On the other hand, the information remaining to be transmitted no longer relates to the low spatial frequencies of the picture as it has been favoured by the weighting and has therefore been transmitted. The information remaining to be transmitted relates only to the high spatial frequencies of the picture and the latter are then transmitted with a large amount of information. After a time interval corresponding to several pictures, the totality of the information representing a static scene is then transmitted and enables the reconstruction of the scene with very good fidelity.

For the encoding and decoding of colour television pictures, the previously mentioned document suggests process-

ing in parallel three series of digital values corresponding to a brightness signal and to two colour difference signals respectively.

This known method has two disadvantages: the fact of the parallel processing of these three series of digital values leads to the use of three buffer memories which must restore the encoded information with data rates having constant ratios because the transmission channel has a constant data rate. Now, the information data rates corresponding to a brightness signal and to two colour difference signals have extremely variable ratios because the saturation of the colours is very variable and can even be zero in the case of pictures containing only whites, greys and blacks. The fact of imposing a constant ratio between these three information data rates leads in practice to uselessly increasing the quantity of information transmitted, or in sacrificing a portion of the information corresponding to colour differences, which is harmful to the fidelity of the reproduction.

Another disadvantage results from the regulation used in this method. When, in a same picture, there is a succession of blocks encoded by an inter-picture encoding, the quantity of information to be transmitted being small, the regulation reacts by increasing the quantification coefficient and tends to maintain a filling of the buffer memory. If an isolated block, or several blocks are to then be encoded by an intra-picture encoding, because they correspond to a limited area which is in motion, it is suddenly necessary to transmit large amounts of information. The buffer memory being maintained practically full, the regulation can only react by sacrificing a large portion of the information to be transmitted, i.e. by suddenly reducing the quantification coefficient when the buffer memory approaches saturation. In such a case, the blocks of picture elements encoded by the inter-picture encoding are restored with excellent fidelity while the adjacent blocks, encoded by an intra-picture encoding are restored with mediocre fidelity. The difference in quality is then very noticeable because these two types of blocks are adjacent in the same picture.

The purpose of the invention is to overcome these two disadvantages of the known method. The object of the invention is an adaptive method of encoding consisting in particular in storing in a same buffer memory the information to be transmitted corresponding to the values of brightness and to the values of the two colour difference signals, and consisting in using weighting coefficients and identical quantification coefficients, except for the application of a constant, for the transformation coefficients or the differences of transformation coefficients corresponding to these three types of signals.

According to another feature, the method according to the invention consists in using weighting coefficients which, in addition to giving a greater weight to information corresponding to the low spatial frequencies of the picture, are also variable according to the quantity of information to be transmitted, in order to further reduce the weight given to the information corresponding to the high spatial frequencies of the picture when the filling of the buffer memory increases and approaches the maximum.

According to another feature of the method according to the invention, the quantification coefficient is variable as a function of the filling rate of the buffer memory, but with a discontinuity corresponding to a fixed filling threshold, in order to be constant below this filling threshold and in order to increase when the filling rises above this threshold.

According to the invention, an adaptive method of encoding and decoding of a series of pictures by transformation, the encoding consisting in:

dividing each picture into blocks of picture elements, each block being represented by a block of brightness values, a block of blue colour difference values and a block of red colour difference values;

applying a two-dimensional transformation to each block of values in order to obtain a block of transformation coefficients of the block of values concerned;

transmitting, for each block of values, either the value of transformation coefficients of the block, or the difference in value of these transformation coefficients, with respect to the value of the transformation coefficients of a similar block in the picture preceding the picture being encoded, in order to minimize the quantity of information to be transmitted for the block in question, the encoding being called intra-picture or inter-picture respectively;

furthermore consisting in multiplying the transformation coefficients and the differences of transformation coefficients, before they are transmitted, by a coefficient called the weighting coefficient, favouring the low spatial frequencies of the pictures; and also in multiplying them by a coefficient called the quantification coefficient which is variable as a function of the quantity of information to be transmitted;

the decoding consisting for each block in:

multiplying each transmitted value of transformation coefficient or each transmitted value of transformation coefficient difference, by a coefficient equal to the inverse of the weighting coefficient used for the encoding and by a coefficient equal to the inverse of the quantification coefficient used for the encoding;

adding, to the value of each difference of transformation coefficients, the value of a transformation coefficient, similar to the coefficient in question in a similar block to the block in question and belonging to the picture preceding the picture being decoded;

applying to each transformation coefficient a transformation which is the inverse of the transformation applied for the encoding, in order to obtain a block of values representing a portion of the decoded picture;

is characterized in that it furthermore consists in regulating the data rate of the transmitted information, in storing in a same buffer memory, the information to be transmitted corresponding to the 3 types of blocks of values, and in multiplying the transformation coefficients and the differences of transformation coefficients of the 3 types of blocks by a same variable weighting coefficient and by a same variable quantification coefficient, except for the application of a constant multiplication factor.

The invention will be better understood and other characteristics will appear with the help of the following description and of the accompanying figures in which:

FIG. **1** shows the order of scanning the transformation coefficients or the differences of transformation coefficients of a block of Picture elements, in one example of implementation of the method according to the invention;

FIG. **2** shows a graph illustrating a weighting performed in this example of implementation;

FIG. **3** shows a graph illustrating a quantification performed in this example of implementation;

FIGS. **4** to **6** illustrate the regulation of the data rate of the transmitted information in this example of implementation;

FIGS. **7** and **8** illustrate the implementation of a variant of the method according to the invention;

FIG. **9** shows the synchronization signals of an encoder and a decoder, in an example of implementation of the method according to the invention;

FIGS. **10** and **11** show the block diagram of an embodiment of an encoding device for the implementation of the method according to the invention;

FIGS. **12** and **13** show the block diagram of an embodiment of a decoding device for the implementation of the method according to the invention.

In one example of implementation, the series of pictures is constituted by a series of colour television frames, sampled and digitized. Each picture element is represented by a brightness value, a red colour difference value and a blue colour difference value, each of these values having eight bits. The brightness is sampled at a frequency of 10.125 MHz while each of the colour difference signals is sampled at a frequency of 5.0625 MHz. The data rate of the encoded information is constant and in the order to 10 Mbits per second.

Each television picture to be encoded is constituted by two interlaced frames analysed in a conventional way by a television camera. Each frame is encoded separately.

In this example of implementation the transformation used is the cosine transformation. It is applied to blocks of 16×16 brightness values, blocks of 16×8 red colour difference values, and blocks of 16×8 blue colour difference values. Any other known two-dimensional transformation can be used for the implementation of the method according to the invention. The transformation is applied in parallel to each of these three types of block. For each block of values it supplies a matrix of values called transformation coefficients of the block of values concerned. The block of transformation coefficients has dimensions identical to those of the block to be transformed. The transformation coefficients have real values.

The transformation coefficients of the brightness values f(i,j) are computed according to the formula:

$$F(u,v)=\sum_{i=0}^{15}\sum_{j=0}^{15} f(i,j)\cdot c(u)\cdot c(v)\cdot \cos\frac{(2i+1)\cdot u\cdot \pi}{32}\cdot \cos\frac{2(j+1)\cdot v\cdot \pi}{32} \quad (1)$$

where $c(u)=1/\sqrt{2}$ if $u=0$

$c(u)=1$ if $u\neq 0$

The transformation coefficients of the colour difference values f'(i,j) are computed according to the formula:

$$F'(u,v)= \quad (2)$$

$$\sum_{i=0}^{15}\sum_{j=0}^{15} f'(i,j)\cdot c(u)\cdot c(v)\cdot \cos\frac{(2i+1)\cdot u\cdot \pi}{32}\cdot \cos\frac{2(j+1)\cdot v\cdot \pi}{16}$$

i and j are respectively the line index and the column index in the block of values to be encoded; u and v are respectively the line and column indices of the transformation coefficients in the block of these coefficient. The transformation coefficient situated in the first column and on the first line is equal to twice the average value of the coefficients of a block of transformation coefficients. It has a value which is always positive. This value must be encoded with the greatest possible accuracy since the slightest error in this transformation coefficient results in a very visible difference between a block of picture elements and the adjacent blocks.

The other coefficients of a transformation block correspond to spatial frequencies of the picture which are increasing as u and v increase. For the highest values of u and v, the transformation coefficients are generally zero. In the series, the coefficients of a block of transformation coefficients are considered according to a scanning order which is graphically represented in FIG. **1** and which corresponds to increasing values of the sum u^2+v^2. The scanning path of the transformation coefficients is chosen in such a way as to optimize the compression ratio for the type of picture which is to be encoded, according to their statistical characteristics.

The implementation of the method according to the invention then consists in performing, in parallel, an encoding called the inter-picture encoding and an encoding called the intra-picture encoding for each type of value to be encoded: brightness value, blue colour difference value and red colour difference value. The inter-picture encoding consists in computing the difference in value between the transformation coefficients of a block of picture elements in question, respectively with regard to the transformation coefficients of a similar block to the block in question in the picture preceding the picture being encoded. The intra-picture encoding consists in directly using the value of the transformation coefficients of the block. In both cases, the method of encoding then consists in applying a weighting, a quantification and then a Huffmann encoding.

In general, the intra-picture encoding of a block representing a portion of a picture in motion requires a larger amount of information than the inter-picture encoding. Conversely, the inter-picture encoding of a block representing a static portion of picture generally requires less information than the intra-picture encoding. The choice of the type of encoding is common for all three types of signal to be encoded. In this example of implementation, the choice of the type of encoding consists in precisely determining the quantities of information respectively necessary in both cases for a same block of digital values to be encoded. Each quantity of information is computed by counting the number of encoded data bits supplied by the following series of operations: weighting, quantification, Huffmann encoding. The method then consists in transmitting the data supplied by the encoding requiring the smallest amount of information.

The weighting enables the exploitation of the fact that a suppression of information encoding certain transformation coefficients of a block of picture elements does not give rise to much degradation in the decoded picture. The coefficients corresponding to the low spatial frequencies of the picture are more sensitive to suppressions of information than the coefficients corresponding to the high spatial frequencies of the picture. The weighting is such that the coefficients corresponding to the low spatial frequencies are favoured. It consists in multiplying the value of the transformation coefficients or of the differences of the transformation coefficients of a block by a weighting coefficient which is given, for the brightness, by the following formula:

$$p^{lum}(u,v)=\exp\left[-\frac{R\cdot u^2+v^2}{Pon^2\cdot Nor}\right] \quad (3)$$

where u and v are respectively the index of the column and of the line of the coefficient or of the difference of coefficients to which the weighting applies; where R is a constant which depends on the size of the block and on the sampling frequency of the picture, its value being 1.4 for a sampling frequency of 10.125 MHz and for a block of size 16×16; where Nor is a constant parameter but depending on R which is given by the following formula:

$$Nor = \frac{2\times 16^2}{R\times 16^2 + 16^2} \quad (4)$$

Nor=0.42 for a sampling frequency of 10.125 MHz;

and where Pon is a variable parameter which defines the severity of the weighting. Its value depends on the filling of the buffer memory storing the encoded information to be transmitted, corresponding to the three types of signal representing the picture elements. This information is the information relating to the blocks preceding the block of picture elements being encoded. The number of bits in question is that obtained after the Huffmann encoding of the non-zero values, the encoding by sequences of zero values, and after insertion of data separating words. The severity of the weighting is an increasing function of the filling of the buffer memory, in order to act against this filling.

In this example of implementation, the capacity of the buffer memory is 64 kilobits. The value of the parameter Pon, and the weighting ratio obtained, between the high and the low spatial frequencies of the picture are given in the following table:

Filling of buffer memory	Value of the Pon parameter	Value obtained for the weighting ratio high/low frequencies
64 to 48 Kb	18	5
48 to 40 Kb	18.5	4.5
40 to 32 Kb	19	4
32 to 24 Kb	20	3.5
24 to 16 Kb	22	3
16 to 8 Kb	24	2.5
8 to 0 Kb	27	2

The value of the transformation coefficients or of the differences of the transformation coefficients for the colour difference signals, is weighted by a coefficient given by the formula:

$$p^{ch}(u, v) = \exp -\left[\frac{R'\cdot\left(\frac{u}{2}+1\right)^2 + v^2}{Pon^2\cdot Nor'}\right] \quad (5)$$

where R' is a constant which depends on the size of the block and on the sampling frequency for the colour difference signal and which is equal to 0.7 for blocks of 16×8 and for a sampling frequency of 5.0625 MHz; and where Nor' is a constant which is given by the following formula:

$$Nor' = \frac{2\times 16^2}{R'\times 16^2 + 16^2} \quad (6)$$

Nor'=0.59 for a sampling frequency of 5.0625 MHz.

The weighting coefficient $P^{ch}(u, v)$ is also a function of the filling of the buffer memory, by means of the variable Pon, in order to participate in the process of regulation of the data rate of the transmitted encoded information. The weighting coefficient is the same for the data encoded by the inter-picture encoding and for that encoded by the intra-picture encoding.

The method of regulation furthermore consists in multiplying the value of the transformation coefficient or of the differences of transformation coefficients of a block by a quantification coefficient which is a function of the filling of the buffer memory, the latter containing the encoded data corresponding to the blocks preceding the block being encoded.

The quantification operation is performed in parallel on the transformation coefficients obtained by the intra-picture encoding and on the differences of transformation coefficients obtained by the inter-picture encoding, after the weighting operation. For a given block of picture elements, all of the transformation coefficients and all of the differences of transformation coefficients corresponding to the brightness are multiplied by the same quantification coefficient value. All of the transformation coefficients and all of the differences of transformation coefficients corresponding to the two colour difference signals are multiplied by a weighting coefficient which has the same value as that corresponding to the brightness, except for the application of a constant multiplication factor. This constant is equal to 1.41 in order to compensate for a constant multiplication factor introduced during the computation of the cosine transforms and which is slightly different for blocks of different sizes, as is the case for the brightness on the one hand and for the colour differences on the other hand.

The quantification coefficient is constant for a filling E_b of the buffer memory, less than a threshold value; it is exponentially decreasing when the filling E_b is above this threshold value. In this example, in which the capacity of the buffer memory is equal to 64000 bits, the filling threshold value is taken as equal to 56000 bits. For the brightness, the quantification coefficient is given by the following formula:

$$N^{lum} = \exp\left(-\frac{E_b - 56000}{Nor}\right) \text{ if } E_b \geq 56000 \text{ bits} \quad (7)$$

$$N^{lum} = 1 \text{ if } E_b < 56000 \text{ bits}$$

For the colour difference signals, the quantification coefficient is given by the following formula:

$$N^{chr} = 1,41\cdot\exp\left(-\frac{E_b - 56000}{Nor'}\right) \text{ if } E_b \geq 56000 \text{ bits} \quad (8)$$

$$N^{chr} = 1,41 \text{ if } E_b < 56000 \text{ bits}$$

where the constants Nor and Nor' have the previously defined values.

The values of the transformation coefficients or of the differences of transformation coefficients are truncated after the weighting and the quantification in order to round them to the closest whole value.

FIG. 2 shows the graph of the ratio between the weighting coefficient applied to the high spatial frequencies and the weighting coefficient applied to the low spatial frequencies of the picture, for the brightness, as a function of the fitting E_b of the buffer memory. It increases in steps as the filling varies from 0 to 64 Kbits.

FIG. 3 shows the graph of the quantification coefficient N^{lum}, corresponding to the brightness, as a function of the fitting E_b. It can clearly be seen on this graph that the quantification coefficient is constant for most of the filling values and that it decreases very rapidly when the filling is close to its maximum. The relationship between the quan-

tification coefficient and the filling, in the method according to the invention, is therefore clearly different from those used conventionally and which vary continuously. A conventional quantification coefficient does not include such a horizontal level but decreases regularly as a function of the filling.

FIGS. **4**, **5** and **6** illustrate the regulation process, in the case in which three successive pictures represent a static scene. Each of these figures shows a graph in which the quantity of information actually transmitted is plotted vertically and in which the rank of the transformation coefficients or of the differences of transformation coefficients of each of these pictures is plotted horizontally, this rank being determined on the scanning path shown in FIG. **1**. The quantities of information concerned are those obtained after the weighting, the quantification and the Huffmann encoding.

However, the quantity of information corresponding to the first transformation coefficient, i.e. having 0 as a line index and as a column index, is not shown in FIGS. **4** to **6** as it is not subject to the data rate regulation. The first coefficient is not weighted and is not standardized in order to avoid showing visible discontinuities between the blocks on the restored picture. FIGS. **4** to **6** therefore show the quantity of information corresponding only to the other transformation coefficients or differences of transformation coefficients.

The first picture of these three successive pictures is assumed to be different from the pictures having possibly preceded it. The transformation coefficients of this first picture are therefore all encoded by an intra-picture encoding necessitating a large amount of information, which is particularly distributed over the transformation coefficients having a low rank. In addition, the weighting has the effect of also favouring the coefficients of low rank. And, finally, certain coefficients of high rank are rounded to zero during the operation consisting in rounding to the closest whole value. Everything happens as if there were a threshold at +0.5 and −0.5. For all of these reasons, in FIG. **4**, the coefficients of high rank are not transmitted by any quantity of information. In particular, many coefficients of high rank are rounded to the zero value because they are less than 0.5 in absolute value. The number of coefficients or differences of coefficients rounded to zero increases when there is a reduction in the quantification coefficient resulting from a large amount of filling of the buffer memory. The threshold effect combined with the quantification therefore tends also to suppress information corresponding to high spatial frequencies.

FIG. **5** corresponds to a second picture which immediately follows the first one and which is identical to it. The transformation coefficients of the second picture are therefore theoretically strictly identical to those of the first picture. They will be encoded by an inter-picture encoding in order to exploit the correlation between the first and second pictures. The inter-picture encoding is performed by computing the difference between the transformation coefficients of the second picture and the transformation coefficients of the first picture after having submitted the latter to an encoding and then to a decoding in order to subtract a same value during the encoding step and during the decoding step.

The weighting and quantification operations suppress information and therefore cause encoding errors which result in a non-zero difference between the transformation coefficients before encoding and the transformation coefficients after encoding followed by decoding. There are therefore non-zero differences between the coefficients encoded and then decoded for the first picture and the coefficients which will be encoded for the second picture. These differences are in particular due to the fact that the weighting coefficient and the quantification coefficient vary from one picture to another.

FIG. **5** shows the quantity of information corresponding to these differences of coefficients, these differences having undergone a weighting, a quantification and a Huffmann encoding. The quantity of information constituted by these differences is lower than the quantity of information corresponding to the values of the transformation coefficients of the first picture for several reasons. Firstly, because the differences of coefficients have low values, since the first picture and the second picture are identical. This quantity of information corresponds above all to the average frequencies and to the high frequencies, i.e. to the average ranks and to the high ranks, because the weighting and quantification performed during the encoding of the first picture have sacrificed the information corresponding to the average ranks and to the high ranks. This information will enable the addition of details in the second restored picture. The encoding of all of the blocks of the second picture being an inter-picture encoding, using the correlation with the first picture, the quantity of information to be transmitted diminishes the buffer memory empties in consequence and the regulation process causes an increase in the quantification coefficient and then its maintenance at the constant value: 1.

The increase in the quantification coefficient increases the amplitude of the differences of transformation coefficients and therefore tends to increase the quantity of information to be transmitted for the coefficients of average and high ranks, and therefore tends to fill the buffer memory. However, the levelling of the quantification coefficients slows down this tendency. Furthermore, the information to be transmitted corresponds in particular to the average and high spatial frequencies since the information corresponding to the low spatial frequencies has been transmitted to a large degree during the encoding of the first picture. The weighting acts progressively against the high frequencies as the buffer memory becomes filled. Therefore the weighting itself also tends to reduce the quantity of information transmitted for the second picture. Finally, this quantity if distinctly less than that transmitted for the first picture.

The encoding of a third picture identical to the two previous ones is also an inter-picture encoding and only has to transmit information corresponding to high spatial frequencies which have not been able to be transmitted during the encoding of the first and second pictures. This information will enable the addition of fine details to the restored third picture. Thus when there is a series of static pictures, the restored pictures rapidly achieve a very good fidelity.

FIG. **6** shows the quantity of information to be transmitted for the third picture, as a function of the rank of the coefficients. It should be noted that this quantity of information corresponds in particular to the very high spatial frequencies and that it is generally smaller with respect to the quantity of information to be transmitted for the encoding of the second picture and for the encoding of the first picture, because the weighting very much acts against the very high frequencies, even though the buffer memory is beginning to empty. The severity of the quantification and the weighting is chosen such that the regulation does not tend to maintain the filling at a constant level, but tends to reduce the filling during each inter-picture encoding.

In the most general case, each picture comprises static areas and areas in motion. The blocks located in the areas in

motion require an intra-picture encoding which tends to saturate the buffer memory. The severity of the weighting and the quantification is chosen such that the memory is not saturated by the information corresponding to these blocks. The weighting is a function of the filling of the buffer memory in such a way that it acts to a lesser degree against the coefficients or the differences of coefficients corresponding to the high spatial frequencies, as the filling diminishes. But the severity of the weighting remains such that the buffer memory empties when there is a series of blocks encoded by the inter-picture encoding, in order to have a capacity available for the encoding of blocks encoded by an intra-picture encoding which produces a large amount of information to be transmitted.

Thus when one or more successive blocks have to be encoded by an intra-picture encoding, the buffer memory is not close to saturation and consequently the quantification coefficient does not have to be suddenly increased in order to avoid an overshooting of the capacity of the buffer memory when a block to be encoded by the intra-picture encoding arrives. By avoiding sudden variations in the quantification coefficient, this regulation process avoids suddenly degrading the quality of restoration of the picture from one block to another in the same picture. This makes it possible to avoid a visible contrast in the quality of restoration, between blocks encoded by inter-picture encoding and blocks encoded by intra-picture encoding, close to each other in the same picture.

Since the method according to the invention consists in multiplying the transformation coefficients or differences of transformation coefficients corresponding to the brightness and to the colour difference signals, by the same weighting coefficient and by the same quantification coefficient, apart from the application of a constant multiplication factor, these three types of signals are therefore encoded with the same quality within a same block, and the information to be transmitted can be stored in a common buffer memory. This storage in a common buffer memory enables the transmission of the encoded information with any ratio between the quantities of information corresponding to the three types of signals. The absence of an imposed ratio between the quantities of information transmitted for the three types of signals enables, with equal fidelity, an important gain in the compression rate of the pictures.

In fact, the quantity of information to be transmitted for the two colour difference signals is extremely variable depending on the scenes represented by the pictures. When the pictures have colours which are not very saturated, the quantity of information to be transmitted for the colour difference signals is low. In this case, the common regulation enables the transmission of a reduced quantity of information for the colour difference signals, unlike the conventional method of independent regulation for the three types of signals, which leads to the use of three independent buffer memories and imposes a constant ratio between the quantities of information transmitted for the three types of signals.

The filling E_b of the buffer memory must be known before starting the encoding of a block in question. It must take into account the encoded information corresponding to all of the blocks which precede the block in question. It is computed by adding the quantities of information to be transmitted for all of the blocks preceding the block in question, and by subtracting from this sum the quantity of information transmitted, computed by taking the product of the data rate of the transmission channel and the duration which has elapsed between the start of the transmission and the end of the transmission of the information encoding the block preceding the block in question.

After the quantification, each value of a transformation coefficient or difference of transformation coefficients, with the exception of the first coefficient in each block, and with the exception of the zero values, is encoded by a Huffmann code. The transformation coefficients or differences of transformation coefficients of one block are considered successively in the order of scanning corresponding to increasing u^2+v^2, according to FIG. 1. The coefficients or differences of coefficients which are zero are encoded by sequences, the lengths of the sequences being encoded by a Huffmann code. The order of scanning chosen is such that the series of coefficients or of differences of coefficients of a block always ends with a long sequence of zero values. The first coefficient or the first difference of coefficients of each block, having 0 as a line index and as a column index, is transmitted without Huffmann encoding.

In order to optimize the reduction of the data rate, the Huffmann encoding is performed according to 8 different trees;

A1, for encoding the transformation coefficients corresponding to the brightness signal, which are preceded by a sequence of zeroes;

A2, for encoding the transformation coefficients corresponding to the brightness signal, which are not preceded by a sequence of zeroes;

A3, for encoding the differences of transformation coefficients corresponding to the brightness signal, which are preceded by a sequence of zeroes;

A4, for encoding the differences of transformation coefficients corresponding to the brightness signal, which are not preceded by a sequence of zeroes;

A5, for encoding the transformation coefficients corresponding to any of the colour difference signals, which are preceded by a sequence of zeroes;

A6, for encoding the transformation coefficients corresponding to any of the colour difference signals, which are not preceded by a sequence of zeroes;

A7, for the encoding of the differences of transformation coefficients corresponding to any of the colour difference signals, which are preceded by a sequence of zeroes;

A8, for the encoding of differences of transformation coefficients corresponding to any of the colour difference signals, which are not preceded by a sequence of zeroes.

However, it is possible to use identical encoding trees A5 and A7; and identical encoding trees A4, A6 and A8, at the cost of a certain degradation in the compression rate. It should also be noted that the encoding trees also encode particular events: packing bits and data separator words.

The fact of using two different trees for encoding the values of coefficients or of differences of coefficients which are not zero and which are not preceded by a sequence of zeroes and for encoding the coefficients or differences of coefficients which are not zero and which are preceded by a sequence of zeroes, results in a reduction in the quantity of information to be transmitted in the order of 10% with respect to the known methods in which a single encoding tree is used for these two separate cases. The reason for this reduction is as follows: a priori, it would be necessary to have two separate trees, with a prefix to distinguish them from each other, in order to encode on the one hand a sequence of zeroes and, on the other hand, to encode a coefficient or a non-zero coefficient difference. But there are never two consecutive sequences of zeroes, as in this case they would be encoded as a single sequence. Consequently,

it is certain that after a sequence of zeroes there is a coefficient or a difference of coefficients which is not zero. It is known information which does not therefore have to be transmitted. The use of the two trees mentioned above enables this redundancy of information to be exploited in order to reduce the quantity of information to be transmitted.

In this example of implementation, the Huffmann codes used for encoding the coefficients have a dynamic range limited to −63, +63. Those used for encoding the differences of coefficients have a dynamic range limited to −31, +31. In the case of overshoot, at least one overshoot prefix is added. In order to distinguish the 0 modulo +64 and the 0 modulo −64 values, two distinct code words are added. The multiple values of +64 and −64 are respectively denoted 0+ and 0− in the following description and they encoded using several overshoot prefixes. The last sequence of zeroes in each block is not encoded, the encoded data corresponding to each block being separated by an inter-block synchronization word. The value of the first coefficient or of the first difference of coefficients in each block is represented in clear by nine bits.

The eight Huffmann trees satisfy the following conditions:

the code words all have a length less than 16 bits;

no licit concatenation of code words must make a series of 10 zeroes appear, consequently:

the code words cannot terminate, unless by exception, in more than 5 zeroes;

the word "00000" is reserved for precise uses;

the code words cannot begin with more than 4 zeroes;

only the encoding trees corresponding to the colour difference signals include synchronization words.

The encoding tree A1 encodes 195 events. The non-zero coefficients give rise to 129 possible events which are: the values −63, . . . , −1, 1, . . . , +63; an overshoot prefix relating to the coefficients; a value which is a multiple of +64, which is referenced 0+; a value which is a multiple of −64, which is referenced 0−.

The sequences of zeroes give rise to 65 possible events: the values of length: 1,. . . , 63: an overshoot prefix relating to the sequences of zeroes; and a zero value 0_p associated with the sequences of zeroes.

A particular event is constituted by a packing.

The conditions which this tree A1 must satisfy are as follows: the event 0+ must be encoded by "00000"; the code words must end in at least 3 zeroes; and the overshoot prefix for the coefficients must end in 1.

The tree A2 encodes 129 events: the values −63, . . . , −1, 1, . . . , 63; an overshoot prefix relating to the coefficients; a value which is a multiple of +64, referenced 0+; a value which is a multiple of −64, referenced 0−. This tree must satisfy the following condition: the shortest code word must have a length of two bits and be constituted by "00". There is no prohibited event.

The tree A3 encodes 195 events and has the following characteristics:

the non-zero coefficients give rise to 129 events: the values −63, . . . , −1, 1, . . . , 63; an overshoot prefix relating to the coefficients; a value which is a multiple of +64; and a value of which is a multiple of −64;

the sequences of zeroes give rise to 65 events: the values 1, . . . , 63; an overshoot prefix relating to the sequences of zeroes; a value 0_p relating to the sequences of zeroes;

a particular event is constituted by a packing.

This tree A3 must satisfy the following conditions: the value which is a multiple of +64 is encoded by "00000"; the code words must not end in more than 4 zeroes; the length of the code words, for the lengths of sequences of zeroes, is greater than three bits; and the overshoot prefix relating to the coefficients must end in a 1.

The tree A4 must encode 65 events which are: the values of non-zero coefficients: −31, . . . , −1, +1, . . . , 31; an overshoot prefix relating to coefficients; a value which is a multiple of +31; a value which is a multiple of −31. This tree must satisfy the following condition: the shortest code word must have a length of one bit and be equal to 0. There is no prohibited event.

The tree A5 encodes 131 events and must have the following characteristics: 65 events for the coefficients, constituted by the values −31, . . . , −1, +1, . . . , 31; an overshoot prefix relating to coefficients, 0+, 0−; 65 events for the sequences of zeroes; the values 1, . . . , 63, an overshoot prefix associated with the sequences of zeroes, and the zero length; a particular event which is constituted by an intra-block synchronization word. This tree must satisfy the following conditions: the value 0+ must be encoded by 00000; the sequences of zeroes cannot end in more than 4 zeroes; the length of the sequences of zeroes must be greater than 3; and the code of the overshoot prefix relating to the coefficients must end in 1.

A particular event is constituted by an intra-block synchronization word.

The tree A6 encodes 65 events and it is identical to the tree A4.

The tree A7 encodes 131 events and it is identical to the tree A5.

The tree A8 encodes 65 events and it is identical to the tree A5.

An optional refinement of the method according to the invention consists in making the weighting coefficient and the quantification coefficient functions of a parameter called the category of the block of elements being encoded. This parameter represents the difficulty of restoration of this block of picture elements. In fact, experience shows that the worst restored blocks are characterized by the fact that they contain at least one relatively uniform dark area extending over at least one block of picture elements adjacent to the block in question, the boundary between the two blocks passing through the dark area over a relatively long length. In such a case the dark area is encoded differently on either side of the boundary, which makes the division of the picture into blocks visible, particularly because the granular noise is not restored in the same way and is visible particularly in a dark area.

In one example of implementation, the method consists in classifying the blocks of picture elements into eight categories numbered from 1 to 8 according to the increasing difficulty in restoring them without making the boundaries between the blocks appear. It consists in sub-dividing each block of 16×16 elements into blocks of 4×4 elements, then in computing the average value of the brightness in each of the sub-blocks of 4×4 elements. In practice, only the sub-blocks located at the periphery of a block are considered.

FIG. 7 shows an example of a block, with the twelve sub-blocks for which an average value of the brightness is computed. The latter are cross-hatched. The method then consists in computing an average value of brightness in areas of elongated shape located at the periphery of the blocks of picture elements and covering two adjacent sub-blocks. These areas partially overlap. In FIG. 7 the sub-blocks are numbered in the clockwise direction starting from the one located in the upper left-hand corner. In FIG. 8 the areas are numbered in the clock-wise direction starting from the one located in the top left corner. For example the area

N°1 covers the sub-block N°1 and sub-block N°2. The area N°2 covers the sub-block N°2 and the sub-block N°3. The average brightness value in an area is equal to the half-sum of the average brightness values of the two sub-blocks enclosed by this area. This average brightness value is computed according to the following formula:

$$L(\text{area } N°i)=\tfrac{1}{2}(L(\text{block } N°i)+L(\text{block } N°(i+1))) \quad (9)$$

For i=1 to 12; and where L(block N°i) and L(block N°i(+1)) respectively represent the average brightness value in block N°i and the average brightness value in block N°i+1.

The method then consists in determining the area having the smallest average brightness value. This minimum brightness value is referenced L min and determines the difficulty of encoding the block in question. The method then consists in classifying the block in question into a category of difficulty from among eight categories, by comparing the minimum brightness value with seven threshold values and consists in determining a weighting coefficient and a quantification coefficient depending on the category of difficulty determined for the block in question.

The severity of the weighting and of the quantification coefficient is reduced as the difficulty of encoding a block becomes greater, i.e. as the determined minimum brightness becomes lower. The distribution of the blocks into eight categories of difficulty enables a progressiveness in the reduction of severity in the weighting and quantification when the encoding difficulty increases.

Another optional characteristic of the method according to the invention consists in the protection against the propagation of errors, a propagation associated with the differential inter-picture encoding method. If similar blocks in a series of pictures, i.e. having the same position in each of the pictures in the series, are encoded using inter-picture encoding, an error in the first block is repeated in all of the following similar blocks. When such an error can be detected, it is possible to replace all of the incorrect block by the similar block of picture elements in the picture preceding the one containing the incorrect block. As the pictures are, in this example, constituted of two separately encoded frames, the similar block is a block of elements of the frame preceding the frame in question and having the same parity. However, this correction method does not restore a perfect picture and, consequently, it is therefore necessary to limit the propagation of errors by imposing an intra-picture encoding for each block having a given position, with a fixed maximum interval corresponding, for example, to 30 pictures. If the intra-picture encoding is imposed at random or periodic times, the cost in data rate is significantly increased.

The method according to the invention enables the limitation of the propagation of errors with a slight increase in the information data rate. It comprises a first criterion consisting in imposing the intra-picture encoding when, for a given block, the relative difference of the cost of inter-picture encoding and the cost of intra-picture encoding is less than a first threshold value, or when the given block has not been encoded by an intra-picture encoding for a number of pictures N(i,j) greater than a second fixed threshold value; (i,j) being coordinates marking the position of the block in a picture. The first threshold value can be a function f(N(i,j)) of the number of pictures since the given block was encoded by an intra-picture encoding. It is an increasing function in such a way that it causes an intra-picture encoding at the end of a certain time, even if the relative cost difference remains constant.

The relative difference between encoding costs is computed by taking the difference between the number of bits necessary for the encoding of the block using an intra-picture encoding and the number of bits necessary for encoding the block using an inter-picture encoding, and in dividing this difference by the number of bits necessary for encoding the block using an inter-picture encoding. The function f(N(i,j)) can be a function of the form $A.N^2(i,j)$ or $A.N^3(i,j)$, in which A is a constant chosen such that the forcing takes place at the latest after 50 frames encoded by inter-picture encoding. In practice, it is necessary to provide a second criterion enabling the number of pictures during which a given block is encoded by inter-picture encoding to be limited in a definite way. This second criterion consists in comparing the number of pictures during which the given block has been encoded by inter-picture encoding with a second threshold value No fixed for example at 50, which corresponds to 50 frames and therefore to a duration of 1 second in a European television standard.

In certain cases, these criteria can lead to a large number of intra-picture encoding forcings in a same picture. In order to avoid a sudden increase in the quantity of information to be transmitted, it is necessary to stagger in time the intra-picture encoding forcing operations. For this purpose, the method furthermore consists in imposing an intra-picture encoding only for successive blocks separated by an interval greater than a third fixed threshold value. For example, it can consists in only allowing the forcing for blocks whose number, in the frame in question, is equal to N_1 modulo 4, N_1, being a whole value varying from 0 to 3 and changing at each frame. In this example, any block is encoded by an intra-picture encoding with an interval at most equal to N_0+4 frames.

The encoding method according to the invention furthermore consists in transmitting with the encoded data synchronization information enabling the sampling frequency of the pictures to be recovered after transmission over an asynchronous channel; and furthermore consists in transmitting separators enabling the nature of the various encoded data which are transmitted in series over the transmission channel to be recovered.

In order to recover the frequency called the video frequency of the picture sampling, two types of synchronization patterns are transmitted independently from the encoded data and their separators, while freezing the transmission of these encoded data. A picture synchronization pattern is transmitted at a frequency of 25 Hz, before the encoded data of each even frame; and a line synchronization pattern is transmitted at the frequency of 15625 Hz, in order to slave a clock to the picture elements sampling frequency. These two types of synchronization pattern do not have a fixed position with respect to the encoded data and are not shown in FIG. 9.

These two types of synchronization pattern do not have to be such that they cannot be imitated by concatenations of data, because these patterns are separated by a given number of bits, determined to the nearest 1 bit. A learning process, consisting in checking the presence of successive patterns at times provided for this, enables them to be distinguished from data.

The encoded data separators are shown in FIG. 9. The encoded data corresponding to two frames are preceded by a picture separator which is repeated 8 times in this example. Each picture separator comprises a 16-bit prefix comprising 15 zeroes and 1 one; and includes a 3-bit binary word giving the rank of the separator in the repetition. In practice, the number of repetitions is chosen as a function of the error rate

in the transmission channel. The prefix is a binary word which cannot be imitated by a licit concatenation of Huffmann code words and of inter-block separator words. The repetition of the picture separators enables them to be protected from isolated errors and small packets of errors. The detection of a picture separator is only validated if it is made several times and the exact position of the picture separators is known by means of the 3 bits encoding the rank of each picture separator.

The encoded data corresponding to block N°1 are transmitted after the picture separator repeated 8 times. Then an inter-block separator is transmitted and precedes the encoded data for block N°2. The inter-block separator comprises an 11-bit radical constituted of 10 zeroes and 1 one; a two-bit binary word representing the rank of the block, modulo 4; and a two-bit binary word representing the sum modulo 4 of the rank of the block and the number of events encoded in the block following the inter-block separator. The radical thus constituted can be imitated by a licit concatenation of code words belonging to the eight Huffmann encoding trees. For this purpose the encoding trees comprise code words beginning with at most four 0 and ending in at most five 0. A code word including only 0 is prohibited since, if it were repeated, there would be imitation of the inter-block separator.

The lower section of FIG. **9** shows the format of the encoded data for a block. It comprises: a three-bit binary word representing the category of the block; a bit indicating the type of encoding, inter-picture or intra-picture, encoded data of the red colour difference signal; then these data, with a number of variable bits; then an intra-block separator constituted by a Huffmann code word; then one bit called the inter-intra bit, indicating the type of encoding of the encoded data for the blue colour difference signal; then an intra-block separator, constituted by a Huffmann code word; then a bit indicating the type of encoding for the brightness signal encoded data; then the encoded data of the brightness signal.

It should be noted that the picture separators introduce a negligible redundancy considering their rarity. The intra-block separators are essential since the last sequence of zeroes of each block is not encoded. They are not protected and do not therefore introduce redundancy. On the other hand, there is a redundancy in the inter-block separators. According to the prior art, the inter-block separators belonged to the inter-picture and intra-picture encoding trees of the brightness signal and had a length of 5 bits. The one used in this example of implementation has a length of 15 bits, giving a redundancy of 10 bits. Furthermore, the Huffmann encoding Furthermore, the Huffmann encoding trees of the colour difference signals include a reserved word formed of five consecutive 0 for encoding the value 0+, which increases the average length of the Huffmann codes with respect to those used in the prior art. Redundancy of information in the inter-block separators is estimated as equal to at least 1% of the total transmitted information. This redundancy is low but enables the protection against errors of inter-block separators to be considerably improved.

A good detection of inter-block separators is essential as the loss of a single bit of the encoded data causes a total loss of synchronization of the decoding with respect to the encoding and therefore causes the loss of a complete picture.

In the case in which an inter-block separator is incorrect, it is possible to resynchronize the decoding with the encoding by means of the binary word representing the rank of the block, modulo 4.

There are at least four possibilities of detecting an error in a block, at inter-block separator level:

by detecting an inter-block separator before having detected the two intra-block separators contained in any normal block;

by detecting an inter-block separator whose beginning does not correspond with the end of the data of the preceding block, the end of these data being provided by means of the two-bit binary word representing the rank of the block plus the number of events modulo 4;

by detecting a block rank, modulo 4, not equal to the rank of the previous block incremented by 1;

by detecting a sum of a block rank and of a number of events, modulo 4, which is not equal to the sum of the rank of the block and of the number of events received.

The reception of a block is only validated if none of these conditions occurs. Experience shows that the use of the rank of the block, modulo 4, and of the sum of the rank of the block and of the number of events, modulo 4, which are transmitted in the inter-block separators, enables a large majority of errors affecting the blocks to be detected.

When a block is detected as being incorrect, the method then consists in masking it by replacing it with the similar block in the frame which immediately precedes the frame being decoded. It should be noted that an isolated error in an inter-block separator gives rise to the masking of the block which precedes it and the block which follows it, since the end of the first and the start of the second are not correctly identifiable.

The most annoying type of error is constituted by packets of errors affecting at least four consecutive blocks, because in this case is it not possible to resynchronize the decoding with the encoding since the rank of the block is transmitted modulo 4. All of the following blocks, in the same picture, are shifted. The synchronization is only regained at the start of the next picture. Furthermore, the error propagates over the following images in the blocks encoded by inter-image encoding. It is possible to increase resistance to errors of the inter-block separators by increasing the modulo of the word representing the rank of the block and of the word representing the sum of the rank of the block and the number of events.

FIG. **10** shows the block diagram of an embodiment of an encoding device for the implementation of the method according to the invention. This example comprises: an input terminal **1**; a frame memory **2**; a first and a second block memory **3** and **4**; a device **5** for the classification of the blocks; a brightness encoding device **6**; a colour difference encoding device **7**; a device **8** for computing the quantification coefficient and the weighting coefficient; a memory **9**; a Huffmann encoder and separator generator device **10**; a sequencer **11**; a shift register **12**; a picture synchronization and line synchronization generator **13**; a device **14** for computing the filling of the buffer memory, constituted by the memory **9**, the device **10** and the register **12**; a device **15** for computing the quantity of transmitted information; and an output terminal **19** connected to an asynchronous transmission channel having a constant data rate of 10 Mb per second.

The input terminal **1** receives in parallel a brightness value Y, a red colour difference value DR, and a blue colour difference value DS in the form of a triplet of binary words. Each triplet represents an element of a picture. The series of pictures concerned is a conventional series of television pictures in which each picture is constituted from two interlaced frames but these two frames are independently encoded. The brightness signal is sampled at the frequency

of 10.125 MHz and each of the colour difference signals is sampled at a frequency of 5.06 MHz. The encoding devices **6** and **7** operate in parallel. While the device **6** encodes two brightness values, the device **7** encodes a red colour difference value and a blue colour difference value.

A data input of the frame memory **2** is connected to the input terminal **1**. Read and write control inputs of this memory **2** are connected to the outputs of the sequencer **11** by links which are not shown. The sequencer **11** controls the storage of the values Y, DR, DS, as they become available. A data output of the memory **2** is connected to data inputs of the block memories **3** and **4**. Control inputs of the memories **3** and **4** are connected to outputs of the sequencer **11** by links which are not shown. The sequencer **11** controls the reading from the memory **2** and the writing into the memory **3** of 16×16 brightness values representative of a block of 16×16 picture elements. It simultaneously controls the reading from the memory **2** and the writing into the memory **4** of 8×16 red colour difference values and of 8×16 blue colour difference values representative of the same block of picture elements.

A data output of the block memory **3** is connected to an input terminal **20** of the device **6** and to an input of the classification device **5**. A data output of the block memory **4** is connected to an input of the device **7**. Another input of the device **7** and an input terminal **21** of the device **6** are connected to an output of the device **8**. The device **8** supplies the value of a quantification coefficient and of a weighting coefficient, calculated in order to regulate the data rate of the encoded information transmitted on the transmission channel. The device **8** has a first input connected to an output of the classification device **5**, and a second input connected to an output of the computing device **14**. The device **14** has a first input connected to an output of the device **15**, a second input connected to an output terminal **22** of the device **6** and a third input to a first output of the device **7**.

The memory **9** has: a first data input connected to an output terminal **23** of the device **6** and to a second output of the device **7**; a second data input connected to an output terminal **24** of the device **6** and to a third output of the device **7**; and a third data input connected to an output of the sequencer **11**.

The function of the memory **9** is to store the values of cosine transformation coefficients or of cosine transformation coefficient differences, or the lengths of sequences of zeroes, representing the brightness values or the colour difference values in order to enable a regulation of the data rate of the encoded information sent in the channel. The data received by the first data input of the memory **9** are transformation coefficient values or transformation coefficient difference values or lengths of sequences of zeroes. The data received by the second data input of the memory **9** are indicators corresponding to the data applied to the first data input, in order to indicate the type of encoding, inter- or intra-picture, and the type of data: data corresponding to brightness values or to a red colour difference or to a blue colour difference, and indicating their coefficients or differences of coefficients which are not zero on the one hand, and the lengths of sequences of zeroes on the other hand.

The data received by the third data input of the memory **9** also corresponds to the data received by the first input and indicate the start of a block or, within a block, the start of the brightness data, or the start of the red colour difference data or the start of the blue colour difference data. These two indicators are stored in the memory **9** at the same time as a datum representing the brightness or a colour difference and constitute an instruction for controlling the device **10**, a Huffmann encoder and separator generator, in order to encode the data according to eight distinct Huffmann trees, and in order to supply the inter-block separators, the intra-block separators and the inter-picture separators. The memory **9** has two outputs respectively connected to two inputs of the device **10** in order to supply it in parallel with a datum and a corresponding instruction.

The memory **9** also has read and write control inputs respectively connected to outputs of the sequencer **11** by links which are not shown. The sequencer **11** controls the reading of data and of the corresponding instructions progressively as the device **10** encodes and transmits these data on the channel. The device **10** indicates to the sequencer **11** its availability by a link which is not shown.

The device **10** has an output connected to a parallel input of the shift register **12**. The register **12** has an output connected to the output terminal **16** of the encoding device and has a control input receiving a clock signal HC which defines the transmission frequency an the channel. The picture synchronization and line synchronization generator **13**, has an output also connected to the output terminal **14** in order to supply synchronization patterns at picture frequency and at line frequency. The generator **13** is controlled by the sequencer **11** by means of a link which is not shown. The transmission of the synchronization patterns is performed completely independently from the transmission of the encoded data and their separators while periodically freezing the transmission of these encoded data in order to transmit the synchronization patterns. These patterns will enable, after the decoding, the recovery of the picture and line frequencies which are asynchronous with respect to the channel frequency.

The device **10** is essentially constituted by a sequencer and by read only memories. The read only memories enable the performance of a transcoding from data supplied by the memory **9**; this transcoding is a function of the type of data and the type of data is indicated by the instruction accompanying them. The sequencer is controlled by these instructions to select a read only memory corresponding to a Huffmann code appropriate to the data to be transcoded. The sequencer also supplies the binary words constituting the inter-block separators, the intra-block separators and the picture separators. This sequencer comprises counters for determining the rank of each picture separator, the rank of each block, modulo 4, and the sum of the rank of each block and of the number of events encoded in this block, modulo 4, in order to include these values in the separators, according to the previously described method.

The sequencer **11** supplies clock signals to all of the components of this encoding device and it supplies in particular control signals to the devices **6** and **7** with a period corresponding to the processing of a block of 16×16 picture elements. It should be noted that the values representative of the picture elements are stored in the frame memory **2** with stop time intervals corresponding to the line suppression and to the frame suppression. But these representative values are re-read from the memory **2** at a slightly slower rate, such that the reading is performed at a regular frequency without taking account of the line suppression and frame suppression time intervals.

An output of the device **10** is connected to a parallel input of the shift register **12** to supply it with a binary word corresponding to an encoded datum or to a separator. The shift register **12** transmits the bits of this binary word successively to the output terminal **19** under the effect of the clock HC which corresponds to the transmission frequency on the channel in question.

The device **8** supplies a weighting coefficient which is the same for the brightness encoding device **6** and for the colour difference encoding device **7**, and it supplies a quantification coefficient which is the same, except for the application of a multiplication coefficient, for the devices **6** and **7**. These two coefficients therefore provide a common regulation for the data rate of the information to be transmitted corresponding to the brightness and for the information to be transmitted corresponding to the colour differences. The memory **9** stores both of these types of information to be transmitted together with indicators enabling these different types of information to be identified and constituting instructions for controlling the device **10**.

As the memory **9** is placed upstream of the Huffmann encoder **10**, the regulation of the flow of bits on the channel consists in fact in acting on the amplitude of the coefficients or coefficient differences, by the variable weighting and quantification, before encoding them by means of the Huffmann encoder. A reduction in the amplitude is represented by a reduction in the number of bits at the output of the Huffmann encoder. Everything happens as if there were, instead of the memory **9**, the device **10** and the register **12**, only a buffer memory storing the binary data in series and restoring them in series to the channel. The device **14** in fact computes, not the filling of the memory **9**, but the filling of this buffer memory. The filling of the buffer memory is equal to the quantity of binary information, in the form of Huffmann codes, remaining to be transmitted at the time in question. There is no mathematical relationship between the filling of the memory **9** and the filling of the buffer memory. Consequently, the capacity of the memory **9** is chosen by considering the average length of the Huffmann codes. In this example, the average length is equal to 2 bits. The memory **9** has a capacity of 32K words, each word being constituted by a datum and an instruction, and corresponds to a capacity of 64K bits for the buffer memory as defined before.

The device **15** supplies to the device **14** the value of the quantity of information transmitted on the channel. The devices **6** and **7** supply to the device **14** the cost of encoding each coefficient or difference of coefficients. The device **14** computes the value of the filling of the buffer memory by accumulating the costs of encoding and by subtracting the transmitted quantity. Then it supplies the value of the filling to the computing device **8** which determines a quantification coefficient and a weighting coefficient according to the formulae (3) to (8), by modulating the severity of the quantification and of the weighting as a function of the category of the block determined by the device **5**.

The counting device **15** determines the number of transmitted bits, from the clock signal HC which indicates to it the frequency of transmission on the channel, which is known and constant but which is asynchronous with respect to the sampling frequency of the pictures. The value of the ratio of weighting of the high frequencies with respect to the low frequencies corresponds to the values shown in FIG. **2**. The brightness quantification coefficient has a constant value for a buffer memory filling varying from 0 to 56 Kb and then decreases exponentially for a filling varying from 56 Kb to 64 Kb.

The device comprises, in series, between its input and its output: a device **16** for computing the average brightness in the peripheral areas of each block of picture elements; a device **17** for determining the minimum brightness in each block; and a device **18** for determining the category of a block.

The device **5** computes the average brightness in 12 sub-blocks of 4×8 picture elements, at the periphery of each block, then computes the average brightness in 12 areas of 4×8 elements, according to the method previously described and illustrated in FIGS. **7** and **8**. The device **17** determines the minimum value from among the average values computed by the device **16**. The device **18** compares this average value with the **7** fixed threshold values and derives from this a binary word whose value can vary between 0 and 7 and which constitutes the category number of the block, representing the difficulty of encoding and of restoration of this block. The device **5** is controlled by the sequencer **11** by means of links which are not shown. The device **5** can be produced in the form of a hard-wired logic circuit or in the form of microprocessor and a program memory. In both cases, its embodiment is within the scope of a person skilled in the art.

FIG. **11** shows the block diagram of the brightness encoding device **6**. The device **7** has an entirely similar block diagram. In this embodiment the device **6** comprises: a device **43** for computing a two-dimensional cosine transformation over blocks of size 16×16. The device **43** has an input connected to the input terminal **20** in order to successively receive the brightness values corresponding to a picture block. The two-dimensional transformation is computed in two stages corresponding to two one-dimensional transformations, implementing the known Beyong Gi Lee algorithm. The device **43** can be embodied for example according to the description given in the French Patent Application N°2,581,463.

The encoding device **6** furthermore comprises means enabling the computation in parallel of the transformation coefficients of a block of brightness values and the differences between these values and the transformation coefficients of the similar block in the previous frame. It performs the operations of weighting, quantification and encoding of the sequences of zeroes, in parallel on the coefficients and on the differences of transformation coefficients.

The transformation coefficients computed by the device **43** are successively processed by a weighting device **45**, a quantification device **46**; and a device for encoding the sequences of zeroes **47**. The latter has a first output and a second output respectively supplying encoded data and an indicator indicating the type of data supplied, i.e.: the value of a transformation coefficient or length of a sequence of zeroes. These two outputs are respectively connected to two inputs of a memory **52** intended for storing data and the corresponding indicators, for a block of picture elements encoded according to the intra-image encoding. The memory **52** has two data outputs respectively connected to two inputs a_1 and a_2 of a multiplexer **51**, in order to respectively supply it with a data word and an indicator word.

The device **6** also comprises a subtracter **44** having a first input connected to the output of the device **43** in order to receive the value of a transformation coefficient and having a second input connected to an output of a memory **42** storing the values of the transformation coefficients of the similar block to the one being processed, in the frame encoded immediately previously. The subtracter **44** therefore computes the difference between a transformation coefficient and the similar transformation coefficient in the preceding frame. This difference is then successively processed by a weighting device **48**, a quantification device **49**, and a device **50** for encoding sequences of zeroes. The device **50** has two outputs respectively supplying an encoded datum constituted by a difference of transformation

coefficients or by a length of a sequence of zeroes, and supplying an indicator corresponding to this type of data.

These two outputs are respectively connected to two data inputs of the block memory **53**, intended for storing data and corresponding indicators for a block of picture elements encoded according to the inter-picture encoding. The memory **53** has two data outputs respectively connected to two imputs b_1 and b_2 of the multiplexer **51** in order to supply it with a data word and an indicator word respectively, the latter constituting an instruction for controlling the device **10**.

The multiplexer **51** has a control input connected to an output of a device **39** for selecting the type of encoding. It also has two outputs respectively connected to the output terminals **23** and **24** of the device **6** in order to respectively supply an instruction and a data word constituted by a transformation coefficient value or a transformation coefficient difference value, or a length of a sequence of zeroes value. Depending on the value of a control signal supplied by the device **39**, the multiplexer **51** connects the inputs a_1 and a_2 respectively to its two outputs or connects the inputs b_1 and b_2 respectively to its two outputs, depending on whether the encoding to be performed is of the intra-picture type or of the inter-picture type respectively.

The weighting devices **45** and **48**, and the quantification devices **46** and **49** have control inputs connected to the input terminal **21** of the device **6** in order for each of them to receive a binary word respectively defining the weighting coefficient and the quantification coefficient applied to the transformation coefficients and to the differences of transformation coefficients of the brightness values. The input terminal **21** is also connected to an input of a device **34** computing the computing the inverse of the weighting coefficient and the inverse of the quantification coefficient.

The device **6** furthermore comprises a device **31** for decoding sequences of zeroes corresponding to the transformation coefficients, this device **31** having two inputs respectively connected to the two outputs of the device **47**, and having an output supplying either a non-zero transformation coefficient supplied by the first output of the device **47**, or a sequence of zero values, depending on the value of the indicator supplied by the second output of the device **47**. The zero or non-zero transformation coefficient values supplied by the device **31** are then successively processed by an inverse quantification device **32** and by an inverse weighting device **33** and are then supplied to a first input of a multiplexer **34**.

The device **6** furthermore comprises a device **35** for decoding the sequences of zeroes corresponding to differences of transformation coefficients, having two inputs respectively connected to the first output and to the second output of the device **50** for respectively receiving data, constituted by differences of transformation coefficient or lengths of sequences of zeroes, and indicators indicating the type of these data. The device transmits the non-zero transformation coefficient differences without modifying them, and it supplies a sequence of zero values in order to restore the sequences of zero transformation coefficient differences. These transformation coefficient difference values are supplied by an output of the device **35** and are successively processed by an inverse quantification device **36** and by an inverse weighting device **37** and are then applied to the second input of the multiplexer **34**.

The inverse weighting devices **33** and **37**, and the inverse quantification devices **32** and **36** have control inputs connected to an output of the device **30** in order to respectively receive the inverse weighting coefficient and the inverse quantification coefficient corresponding to the brightness values of the block being processed, which are computed by the device **30**. The multiplexer **34** has an output which is connected either to its first input or to its second input, depending on the value of a binary signal applied to a control input which is connected to the output of the encoding type selection device **39**. The output of the multiplexer **34** is connected to a data input of a memory **41** storing the values of the transformation coefficients of all of the blocks of picture elements of the frame having been processed immediately previously.

A data output of the memory **41** is connected to a data input of a memory **42** storing only the transformation coefficients of the block in the previous frame which is similar to the block of picture elements being processed. The memories **41** and **42** have write and read control inputs connected to outputs of the sequencer **11** by links which are not shown. A data output of the memory **42** is connected to the second input of the subtracter **44** in order to supply it with the value of the transformation coefficients of the similar block, in an order corresponding to the order of transformation coefficients computed by the device **43**, this order for example being the zigzag order shown in FIG. **1**. The memory **42** and the memory **41** act as a digital delay line providing a one-frame delay.

The device **6** furthermore comprises a device **38** for computing the cost of intra-picture encoding and a device **40** for computing the cost of inter-picture encoding, for a same block of picture elements. The device **38** has two inputs respectively connected to the two outputs of the device **47** and has an output connected to an input of the device **39** for selecting the type of encoding. The device **40** has two inputs respectively connected to the two outputs of the encoding device **50** and has an output connected to another input of the device **39**. The devices **38** and **40** compute a cost of encoding taking account of the inter-block, intra-block and inter-picture separators; and taking account of the Huffmann code words used for encoding each transformation coefficient, each difference of transformation coefficient, and each sequence of zeroes. The selection device **39** therefore simultaneously receives two binary words indicating the cost of encoding by intra-picture encoding and by inter-picture encoding.

The device **39** determines which is the lowest cost and in principle selects the type of encoding corresponding to this cost. But it can also impose an intra-picture encoding. The device **39** has a first output connected to the control inputs of the multiplexers **34** and **51** in order to control the inter-picture encoding or the intra-picture encoding; and it has a second output connected to the output terminal **22** in order to supply the cost of encoding of the block. This cost is used for computing the filling of the virtual buffer memory.

In order to compare the encoding costs and for imposing the intra-picture encoding in certain cases, the device **39** can be constituted from a microprocessor and a read only memory containing a program corresponding to the implementation of this method.

The method of forcing comprises three criteria. A first criterion consists: in computing the difference between the cost of the intra-picture encoding and the cost of inter-picture encoding; then in dividing this difference by the cost of the inter-picture encoding; then in comparing the result with a first variable threshold value. This first threshold value is computed by counting the number N(i,j) of blocks having the coordinates (i,j) and having been encoded by an inter-picture encoding since the last time that a block of

coordinates (i,j) was encoded by an intra-image encoding; then in computing a function of N(i,j), divided by a constant. This function can be $N^2(i,j)$, for example.

A second forcing criterion consists in comparing the number N(i,j) with a second threshold value, N_0, which is fixed at 30 for example. The encoding is forced to be an intra-picture encoding when N(i,j) exceeds 30.

A third criterion, intended to stagger the forcing operations in time, consists in only allowing the forcing for blocks whose number, in the frame in question, is equal to a value N_1 modulo 4. The value N_1 is a whole value varying from 0 to 3 and changing at each frame.

The production of this computing program for a microprocessor is within the capabilities of a person skilled in the art.

FIG. **12** is the block diagram of an embodiment of a picture decoder for the implementation of the method according to the invention. This example comprises: an input terminal **57** connected to a transmission channel; a Huffmann decoder **58**; a set **59** of synchronization registers; a memory **60**; means of decoding the brightness **80**; means of decoding the colour difference signals **81**; a device **64** for recovery of the channel frequency; a device **65** for detecting the inter-block separators; a device **66** for detecting the inter-picture separators; a device **67** for detecting the picture synchronization patterns; a device **68** for detecting the line synchronization patterns; a clock **69** at the video signals frequency; a counter **70** of write addresses of the buffer memory; a counter **71** of the cost of a block; a memory **72** for storing the parameters of a block; a counter **73** of read addresses of the buffer memory; a device **74** for computing the inverse quantification coefficient and the inverse weighting coefficient; a counter **90** of the initial filling; a device **91** for computing the filling of the buffer memory constituted by the memory **60**, the decoder **58**, and the registers **59**; a counter **92** of the number of bits received; a category decoder **93**; a sequencer **94**; a counter **95** of write addresses of the parameters memory; a counter **96** of the read addresses of the parameters memory; and three output terminals, **83** to **85**, respectively supplying a brightness value Y, a red colour difference value DR, and a blue colour difference value DB.

The device **67** for detecting the Picture synchronization patterns and the device **68** for detecting the line synchronization patterns have inputs connected to the input terminal **57** and have outputs respectively connected to the two inputs of the clock **69**. The clock **69** supplies a clock signal HV which will determine the frequency of the brightness values, and of the colour difference values restored by the decoder.

The sequencer **94** supplies control signals to all of the components of the decoding device in synchronism with the video clock signal. For purposes of simplification, this block diagram shows only one type of video clock signal, referenced HV, but there are in fact several video clock signals having frequencies which are sub-multiples of the sampling frequency of the brightness signal. The production of these clock signals is within the capabilities of a person skilled in the art.

The device **64** for recovering the channel frequency has an input connected to the input terminal **57** and has an output supplying a clock signal HC corresponding to the frequency of the bits transmitted on the channel. This clock signal is applied in particular to a clock input of the counter **71** counting the cost of a block in order to count the number of bits corresponding to each block received.

The Huffmann decoder **58** has an input, connected to a transmission channel by the input terminal **57**, for receiving a series of binary values at a constant frequency of 10 Mb per second, this series being transmitted by an encoding device such as described previously. It also has a clock input receiving the clock signal HC, and a synchronization input connected to a first output of the inter-block separator detection device **65**. The latter supplies a signal which reinitializes the decoder **58** at the start of the transmission of the encoded data of each block. The decoder **58** can only decode a code word corresponding to an event if it has correctly decoded the code word corresponding to the preceding event. In the case of a transmission error, the Huffmann decoder remains unsynchronized until the detection of the next inter-block separator.

The device **65** has an input connected to the input terminal **57** in order to receive the transmitted bits and to (sic) an input connected to an output of the decoder **68** (sic) in order to receive a logic signal each time that the decoder **58** has decoded an event.

The function of the device **65** is to recognize each inter-block separator by means of the pattern constituting the radical, and to check the absence of transmission error by means of the two binary words which follow the radical. For this purpose, it compares the rank of the block, modulo 4, transmitted in the inter-block separator, and the rank of the block counted according to the number of previously received separators. Furthermore the device **65** checks the number of code words received, i.e, the number of events in the previous block, by comparing the transmitted value of the sum of the rank of the block and the number of events, modulo 4, with the sum computed from the number of previously detected blocks and from the number of previously detected events, modulo 4. An inter-block separator is recognized as valid by the device **65** when it is followed by two other inter-block separators checking these two conditions.

When one of these three checks gives a negative result, a second output of the detection device **65** supplies a masking command constituted by a binary word NBM indicating the number of blocks to be masked, to a first input of the memory **72**. The association of this error detection and the process of masking incorrect blocks enables incorrect transmissions to be corrected in most cases.

In general, error correcting devices, adapted to the type of channel, are respectively interposed between the output terminal **19** of the encoding device and the input terminal **57** of the decoding device. These devices are conventional and are not shown in the figures. They enable the correction of small packets of errors, by means of a small redundancy of the transmitted bits. The checks Performed by the inter-block separator detection device **65** enable the detection of the errors which remain. The latter can be serious for the restored picture because they can falsify not only the brightness or the colours of a block but can affect the position of the whole of the block if an inter-block separator is not recognized. The checking of the rank of each inter-block separator and the checking of the number of decoded events enables a precise computation of the number NBM of blocks to be masked and therefore enables them to be masked and the restoration of an image having a much better quality than if the blocks were restored in inaccurate positions.

The first output of the device **65** is also connected to a zero reset input of the counter **71** for counting the cost of a block; to a clock input of the counter **95** of write addresses of the memory **72**; and to an input of the sequencer **94** by means of a link which is not shown.

When an inter-block separator is valid, the binary signal supplied by the first output of the device **65** reinitializes the

Huffmann decoder **58**, resets to zero the counter **71** counting the cost of a block, increments the counter **95** of write addresses by one unit, and initiates the sequencer **94** such that it commands a writing, in the memory **72**, of the parameters of the block which is recognized as valid. The parameters written into the memory **72** are: the address, ADB, of writing the first word of the encoded data of the block, into the memory **60**; the cost of this block, CB, i.e. the number of bits between the two inter-block separators enclosing these data; and the value of MBN which is equal to the number of blocks to be possibly masked, this number being zero when there is no block to be masked. These three parameters are respectively supplied by the output of the counter **70** write addresses of the buffer memory; the output of the counter **71** counting the cost of a block; and by the third output of the inter-block separator detection device **65**. These three outputs are respectively connected to three data inputs of the memory **72**. The latter has a first, second and third data output for respectively restoring the values of these three parameters. It also has read and write control inputs connected to outputs of the sequencer **94** by links which are not shown.

When an inter-block separator is recognized as valid, the sequencer **94** controls a writing into the memory **72** for storing the parameters of the block which follows this separator. The counter **95** of write addresses has an output connected to a write address input of the memory **72** in order to supply it with a write address for the parameters each time that an inter-block separator is validated. When one or more inter-block separators are not recognized as valid, a single set of parameters is written into the memory **72** for the data of several blocks, as everything happens as though the data corresponded to a single block. These data are stored in the buffer memory **60** even if they are incorrect, and they are read from the memory **60**, but they are not used for restoring a picture. The counter **95** also has a zero reset input connected to the output of the picture synchronization detection device **67** in order to be reset to zero at the start of each picture.

The output of the counter **70** of write addresses is also connected to a write address input of the buffer memory **60**. An input for loading the counter of read addresses, **73**, is connected to the first data output of the memory **72** in order to receive a start of block address, ADB; and has an output connected to a read address input of the buffer memory **60**. The counter **70** has a clock input receiving the video clock signal HV, and has a zero reset input connected to the output of the device **67**. The output of the device **67** is also connected to a zero reset input of the counter **73** of read addresses of the buffer memory. The counter **73** has a clock input connected to an output of the sequencer **94** by a link which is not shown.

The second output of the memory **72** is connected to an input of the device **91** for computing the filling of the buffer memory in order to supply it with the cost of a block, CB. The third output of the memory **72** is connected to an input of the sequencer **94** and to an input terminal **86** of the means **80** and **81** for supplying them with the value of the number of blocks to be masked, NBM.

The Huffmann decoder has a first output and a second output respectively connected to two inputs of registers **59** which are called synchronization registers as they enable the synchronization of the encoded data with the video clock HV, while the Huffmann decoder **58** operates at the channel clock frequency HC. The decoder **58** has a third output supplying an encoding selection binary signal: inter-picture encoding or intra-picture encoding, to an input terminal **75** of the means **80** and **81**. Two outputs of the synchronization registers **59** are respectively connected to two data inputs of the buffer memory **60**, respectively corresponding to encoded data and to a binary instruction word indicating the type of encoded data. The buffer memory **60** has a first output and a second output respectively connected to input terminals **77** and **76** of the means **80** and **81** in order to supply them respectively with encoded data and a binary instruction word.

The memory **60** also has a write clock input and a read clock input respectively connected to two outputs of the sequencer **94** by links which are not shown. When an inter-block separator has been recognized as valid, the sequencer **94** commands the writing into the memory **60**, of the encoded data corresponding to at least one block, at a series of addresses supplied by the counter **70**, following the start address of the block ADB, which is the only one stored in the memory **72**.

For reading the encoded data stored in the memory **60**, the sequencer **94** commands, for each block or group of blocks (if an error has been detected):

a reading, from the memory **72**, of the address ADB corresponding to the start of the block;

a loading of this address into the counter of read addresses **73**;

a reading at the address ADS, from the buffer memory **60**, the address ADS having been supplied to the read address input by the counter **73**;

a series of incrementations of the content of the counter **73**;

a series of readings, from the buffer memory **60**, at addresses supplied by the counter **73**.

As the memory **60** is placed downstream of the Huffmann decoder **58**, everything occurs as if, instead of the decoder **58** and the memory **60**, there were a buffer memory storing in series the binary data transmitted by the channel and restoring them in series. The computing device **91** in fact computes the filling of this buffer memory, which is not related mathematically to the filling of the memory **60** as the latter contains binary words supplied by the Huffmann decoder. The filling of the buffer memory is equal to the quantity of binary information, in the form of Huffmann codes, which remains to be decoded at the instant in question. The capacity of the memory **60** is identical to the capacity of the memory **9** of the encoding device and is sufficient in all cases. In this example it is 32K words, each word being constituted by a datum and an instruction.

The device **74** for computing the quantification coefficient and the weighting coefficient has two outputs respectively connected to input terminals **78** and **79** of the means **80** and **81**, and has two inputs respectively connected to an output of the computing device **91** and to an output of the category decoder **93**. The computing device **91** has a first input connected to the second data output of the memory **72**, supplying a binary word CB which is the cost of encoding a block; a second input connected to an output of the initial filling counter **90**, supplying a value OCI; a third input connected to an output of the counter **72**, supplying the number of bits received NCANAL; and a fourth input, a zero reset input, connected to an output of the picture synchronization detection device **67**.

The initial filling counter, **90**, has a clock input receiving the video clock signal HV; a stop input connected to the output the inter-picture separator detection device **66**; and a zero reset input connected to the output of the picture synchronization pattern detection device **67**. The counter **90** counts the number of bits supplied by the channel to the

buffer memory, between the instant at which a picture synchronization pattern is detected and the instant at which an inter-picture separator is detected. The result of this count constitutes the value of the initial filling OCI of the buffer memory, at the start of the each picture.

The counter **92** of the number of received bits has an input connected to the input terminal **57** and an input connected to an output of the sequencer **94**. The counter **92** measures the exact number of bits received by the buffer memory since the start of a block, this number not being known in advance in an accurate way as the channel is asynchronous. The counter **92** is reset to zero by a signal supplied by the sequencer **94**, in principle at the start of the reception of each block, but the sequencer **94** skips one or more zero resets when the binary word NBM is not zero, i.e. when there is at least one block to be masked. For example, if there are two blocks to be masked, the sequencer **94** only commands a zero reset of the counter **92** at the end of the second masked block.

The category decoder **93** has an input connected to the input terminal **57** for decoding a binary word indicating a category and located just after each inter-block separator. It supplies this binary word to the computing device **74** which takes it into account for computing the quantification coefficient and the inverse weighting coefficient in the same way as the device for computing the quantification and weighting coefficients in the previously described encoding device.

The device **74** for computing the inverse quantification coefficient and the inverse weighting coefficient operate in a similar way to the device **30** computing the quantification coefficient and the weighting coefficient, but in addition it performs the computation of the inverse of the quantification coefficient and the inverse of the weighting coefficient obtained by the formulae (3) to (8).

In these formulae the filling of the buffer memory of the encoding device is replaced by a value which is equal to a constant less the filling of the buffer memory of the decoding device. In fact, the sum of the filling of these two buffer memories is equal to a constant when the regulation is correctly operating in the encoding device and the decoding device, the consequence of this regulation being that each encoded datum undergoes a constant delay between the time at which it enters into the buffer memory of the encoding device and the time at which it leaves the buffer memory of the decoding device, since the data rate of the channel is constant. This delay corresponds to the constant value of the sum of the two fillings.

This constant is determined by measuring the initial filling OCI of the buffer memory of the decoding device, by means of the initial filling counter **90**, which measures the number of bits entering into the device **58** between the time at which the device detects the picture synchronization pattern, which is transmitted independently from the flow of encoded data, and the time at which the device **66** detects the presence of an inter-picture separator in the encoded data arriving at the input of the device. The maintenance of the complementary nature of the filling of the two buffer memories enables the inverse quantification coefficient and the inverse weighting coefficient to be computed exactly in the decoder. No information representing the filling of the buffer memory is sent in clear on the transmission channel and consequently this information is not disturbed by the errors.

FIG. **13** shows the more detailed block diagram of the brigtness decoding means **80**. The means **81** have a similar block diagram and are used alternately for decoding the red colour difference signals and blue colour difference signals. The means **80** comprise: an inverse quantification device **101**; an inverse weighting device **102**; three multiplexers **103** to **105**, each having two inputs and one output; a memory **106** storing a block of transformation coefficients; an adder **107**; a sequencer **108**; a register **109** for storing a similar coefficient; a memory **110** for storing the blocks of similar coefficients in the frame preceding the current frame; a device **111** for decoding the sequences of zeroes; a frame memory **112**; and a device **113** for computing the two-dimensional inverse cosine transforms.

The device **101** has a data input connected to the input terminal **77** which receives encoded data supplied by the buffer memory **60**, and has a control input connected to the input terminal **78** which receives the value of an inverse quantification coefficient computed by the device **74**. An output of the device **101** is connected to an input of the device **102**. The latter also has an input connected to the input terminal **79** in order to receive the value of an inverse weighting coefficient computed by the device **74**, and has an output connected to a first input of the multiplexer **103**. The multiplexer **103** has a second input continuously receiving a zero value, and has an output which is connected either to the first input or to the second input depending on the value of a binary signal applied to a control input, connected to an output of the device **111**.

The device **111** decodes the sequences of zeroes from the data and from an instruction, applied respectively to a first input and to a second input which are respectively connected to the input terminal **77** and to the input terminal **76** of the means **80**. The output of the multiplexer **103** therefore supplies the value of a coefficient or a difference of transformation coefficient. It is connected to a first input of the multiplexer **104** and to a first input of the adder **107**. A second input of the adder **107** is connected to an output of the register **109** which supplies it with the value of the transformation coefficient similar to the coefficient being decoded and occurring in the picture preceding the picture being decoded.

The output of the adder **107** therefore supplies the value of a transformation coefficient when its first input receives the value of a difference of transformation coefficient. This output is connected to the second input of the multiplexer **104**. The multiplexer **104** has a control input connected to the input terminal **75** in order to receive the value of a control bit selecting an inter-picture decoding or an intra-picture decoding, and it has an output connected to a first input of the multiplexer **105**. A second input of the multiplexer **105** is connected to the output of the register **109** in order to receive the value of the coefficient similar to the coefficient being decoded. A control input of the multiplexer **105** is connected to an output of the sequencer **108** in order to possibly receive a masking control signal. When this masking signal is applied to the multiplexer **105**, the latter transmits the value of the similar coefficient supplied by the register **109** instead of transmitting the value of the transformation coefficient supplied by the multiplexer **104**.

The output of the multiplexer **105** is connected to a data input of the memory **106**. The memory **106** has write and read control inputs respectively connected to the outputs of the sequencer **108**, the latter commanding the memory **106** to store all the transformation coefficients of a block before commanding the inverse cosine transformation of these coefficients. The sequencer **108** has an input receiving the video clock signal HV, an input connected to the input terminal **76** in order to receive an instruction depending on

the type of data to be decoded and an input connected to the input terminal **86** in order to receive the value NBM of the number of blocks to be masked. If NBM=0 the sequencer **108** does not command the masking. If NBM is other than 0, the sequencer **108** commands the masking of the number of indicated blocks.

The memory **110** has a data input connected to a data output of the memory **106** in order to store all of the blocks of transformation coefficients resulting from the decoding of a frame in order to be able to supply the coefficients similar to the transformation coefficients of the following frame. The memory **110** has a data output connected to a data input of the register **109**, and has read and write control inputs connected to the outputs of the sequencer **108**.

The data output of the memory **106** is also connected to an input of the computing device **113**. The latter has a zero reset input connected to an output of the sequencer **108**, and has an output connected to a data input of the picture memory **112**. The frame memory **112** has a read and write control input connected to outputs of the sequencer **108** and has a data output connected to the output terminal **83** of the decoder, in order to supply a series of brightness values Y. The frame memory **112** has the function of restoring the series of brightness values in the conventional scanning order of a frame while the computing device **113** supplies the decoded brightness values in the order of division of the blocks in the frame. The embodiment of the computing device **113** for performing inverse cosine transformations is conventional. It can be embodied according to the description in the French Patent Application No. 2,581,463.

The scope of the invention is not limited to the examples of embodiment described above and numerous variant embodiments are within the capabilities of a person skilled in the art.

The invention claimed is:

1. A method for decoding a sequence of pictures coded in such a way that a picture is divided into blocks of picture elements, each block being represented by corresponding luminance and chrominance blocks and that an inter coding takes into account a previous picture and an intra coding is independent from a previous picture, and coding using weighting coefficients, high spatial frequencies being less weighted than low spatial frequencies, and using the same weighting coefficients for coding of the corresponding luminance and the chrominance blocks; wherein same coding type (inter or intra) is specified at a block level and the same coding type is applied to the corresponding luminance and chrominance blocks; and a picture separator word is inserted between encoded data corresponding to two consecutive pictures, each picture separator word comprises a pattern which cannot be imitated by licit concatenations of encoded data.

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Exhibit 11

US005422676A

United States Patent [19]

Herpel et al.

[11] Patent Number: 5,422,676

[45] Date of Patent: Jun. 6, 1995

[54] **SYSTEM FOR CODING AN IMAGE REPRESENTATIVE SIGNAL**

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[52] **U.S. Cl.** **348/420;** 348/407

[58] **Field of Search** 348/400, 407, 420; H04N 7/133, 7/137

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,849,812	7/1989	Borgers et al.	348/400
5,091,782	2/1992	Krause et al.	348/400

FOREIGN PATENT DOCUMENTS

262555	9/1987	European Pat. Off. .
290085	4/1988	European Pat. Off. .
1381730	3/1988	U.S.S.R. .

OTHER PUBLICATIONS

W. Jass et al., "A Hybrid DCT-Coder with Local Adaptivity for the Interlaced HDTV-Transmission with 140 Mbit/s", Proceedings of the SPIE Image Processing Algorithms and Techniques, Feb. 12–14, 1990, pp. 378–388.

R. Kutra, Block Adaptive Frame/Field DCT Coding Decided by the Vertical Difference Test, Proceedings of the Third International Workshop on HDTV, Aug. 30–Sep. 1, 1989, pp. 739–748.

P. Vogel, Videobild auf der Datenleitung, Funkschau, vol. 60, No. 26, Dec. 16, 1988, pp. 60–63.

DeWith, P. H. N., Motion-Adaptive Intraframe Transform Coding of Video Signals, Philips Journal of Research, vol. 44, No. 2/3, pp. 345–364, FIG. 3.

Ericsson, S., Fixed and Adaptive Predictors for Hybrid Predictive/Transform Coding, IEEE Transactions on Communications, vol. COM-33, No. 12, Dec. 1985.

Kamangar, F. A. et al., Interfield Hybrid Coding of Component Color Television Signals, IEEE Transactions on Communications, vol. COM-29, No. 12, Dec. 1981, pp. 1740–1753.

Progressive Picture Transmission Using Interleaved Blocks, Electronics Letters, 5 Dec. 1985, vol. 21, No.25/26, pp. 1181–1182, FIG. 1.

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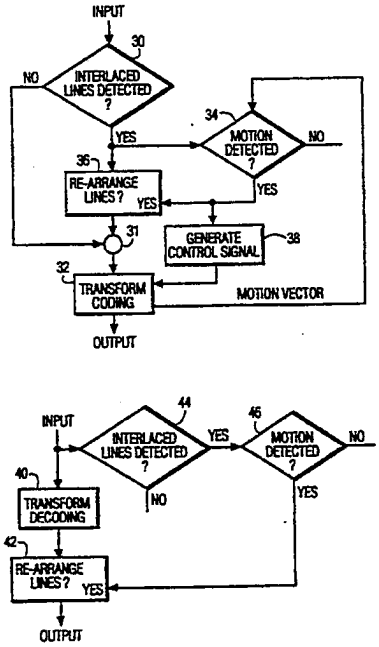
[57] **ABSTRACT**

A hybrid Discrete Cosine Transform (DCT) coder processes blocks of (e.g., 8×8) pixels from interlaced or progressive scanned image signals. Processing of image lines by the coder is modified in the presence of image motion to avoid switching between 8×8 and 2×(4×8) transformations. For motion, the lines of two vertically superimposed image blocks are rearranged to produce first and second modified blocks. The modified first block contains pixels from lines in a first field, and the modified second block contains pixels from lines in an associated adjacent second field.

10 Claims, 3 Drawing Sheets



11	11	11	11
12	12	12	12
13	13	13	13
14	14	14	14

FIG.1a

11	11	11	11
13	13	13	13
21	21	21	21
23	23	23	23

21	21	21	21
22	22	22	22
23	23	23	23
24	24	24	24

FIG.1b

12	12	12	12
14	14	14	14
22	22	22	22
24	24	24	24

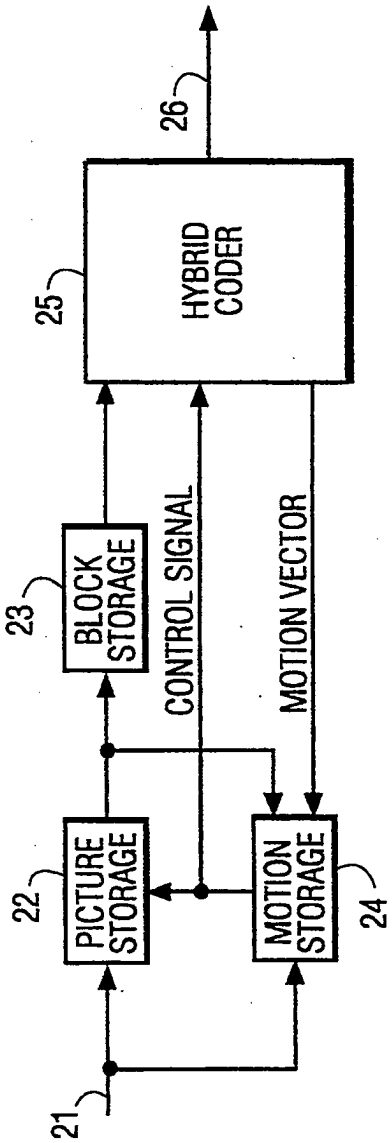

26
HYBRID CODER
25
BLOCK STORAGE
23
CONTROL SIGNAL
MOTION VECTOR
PICTURE STORAGE
22
MOTION STORAGE
24
21

FIG. 2

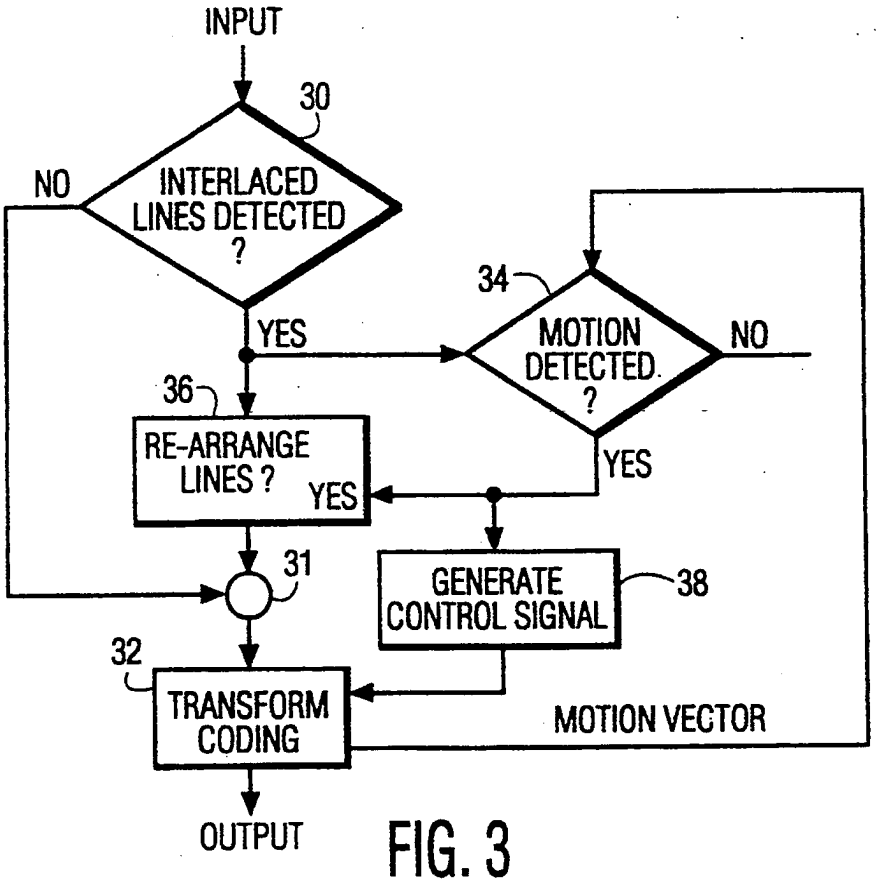

INPUT
30
INTERLACED LINES DETECTED ?
NO
YES
34
MOTION DETECTED ?
NO
YES
36
RE-ARRANGE LINES ?
YES
31
GENERATE CONTROL SIGNAL
38
32
TRANSFORM CODING
MOTION VECTOR
OUTPUT

FIG. 3

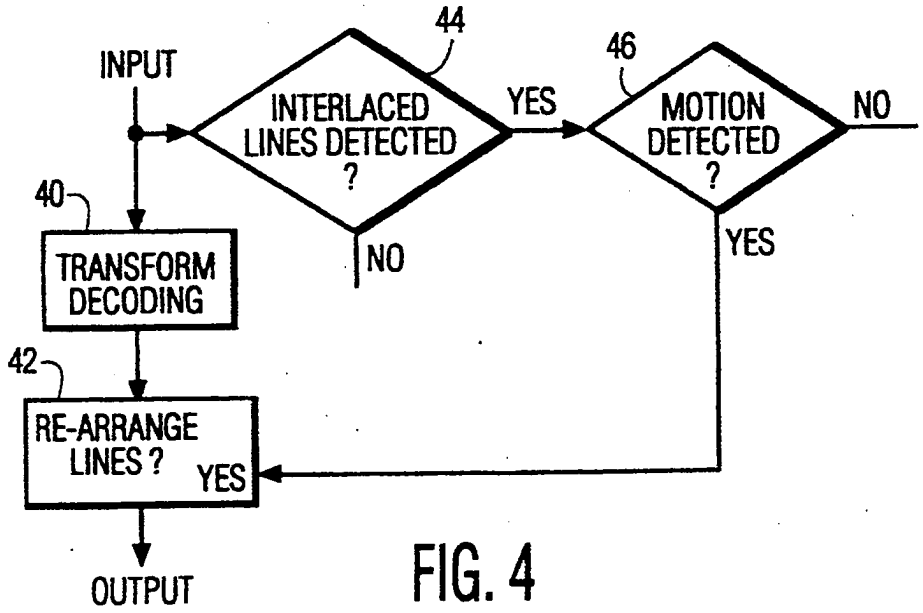

INPUT
44
INTERLACED LINES DETECTED ?
YES
46
MOTION DETECTED ?
NO
NO
YES
40
TRANSFORM DECODING
42
RE-ARRANGE LINES ?
YES
OUTPUT

FIG. 4

SYSTEM FOR CODING AN IMAGE REPRESENTATIVE SIGNAL

This is a continuation of PCT application PCT/EP 92/00843 filed Apr. 14, 1992 by Carsten Herpel and Heinz-Werner Keesen titled "Process for Coding Picture Signals".

BACKGROUND OF THE INVENTION

This invention relates to a system for coding image signals such as by means of a DCT (Discrete Cosine Transform), for example.

A transformation circuit for facilitating an 8*8 or a 2*(4*8) DCT transformation is described in DE 36 42 664. Switching between an 8*8 and a 2*(4*8) DCT may be accomplished in response to the state of a logic level on a control line.

SUMMARY OF THE INVENTION

An object of the invention is to provide a system for coding image signals by means of a codec suitable for processing both progressively scanned and interlace scanned image signals.

In a system according to the present invention, before coding with a hybrid coder which can process blocks of progressively scanned picture elements (pixels), line sections from respective blocks of interlace scanned picture elements within two vertically superimposed blocks are arranged such that only line sections from one field of an image signal are contained within each of these blocks. Image motion is detected and the line sections are re-sorted within the superimposed blocks in the presence of dynamic image content.

According to a method for hybrid coding of image signals proposed by ISO-MPEG (International Organisation for Standardization, Motion Picture Expert Group) under Standard Proposal number ISO 11172, progressively scanned input signals are DCT processed in blocks, whereby respective blocks of 8*8 picture elements are coded or decoded and a sequence of interframe coded images is replaced as regular intervals by intra-frame coded images. The effectiveness of the coding is also a function of the relatively high spatial corelation of picture elements within such blocks. If interlaced source signals are to be processed by such a hybrid decoder, coding effectiveness decreases if dynamic image content or the data rate required for coding increases. This results because every second line derives from a block having different phases of motion, and correlation of picture elements within such a block decrease. In contrast, coding effectiveness is maintained in the presence of a static image. With a dynamic image, image lines associated with a first field from two superimposed 8*8 picture element blocks are now combined into a first 8*8 block, and lines associated with a corresponding second field from these two superimposed 8*8 picture element blocks are combined into a second 8*8 block, and are applied in this form to the hybrid coder.

Due to such reorganisation of the input signals, it is not necessary to switch between 8*8 and a 2*(4*8) DCT transformation in the hybrid coder as in DE 36 42 664. Instead, an 8*8 DCT can also be advantageously performed for a dynamic image.

A motion detector indicates whether a static or dynamic image is present, and re-sorting or addressing of the lines is done accordingly. Such motion information may be added to the coded data for the respective block

by means of a bit per block or double block. During decoding, the corresponding lines are arranged in the original sequence whereby the motion information is evaluated. According to the MPEG standard, four luminance picture element blocks arranged in the shape of a square are combined into a macroblock. Advantageously, two of the superimposed blocks of such a macroblock form a pair in the above-mentioned sense. Accordingly, one bit per macroblock can indicate the resorting.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates the location of image lines within blocks for static (a) and dynamic (b) images.

FIG. **2** is a block diagram codec apparatus in accordance with the invention.

FIGS. **3** and **4** are flow diagrams respectively depicting encoder and decoder processing methods in accordance with the principles of the invention.

DETAILED DESCRIPTION

FIG. **1***a* and **1***b* respectively show two superimposed blocks of luminance or chrominance picture elements in the x-y plane. For simplicity of illustration, each block includes 4*4 picture elements instead of 8*8 picture elements. In general, the blocks could also have a size of (2*n)*(2*m) where n=1, 2, 3, . . . , m=1, 2, 3, . . . , instead of 8*8. The two digit numbers respectively designate the spatial position of a picture element. The first digit of each number represents the block number, and the second digit represents the line number within a block.

The picture elements which are to be coded or decoded in progressively scanned form by a known hybrid coder are arranged as shown in FIG. **1***a*. This arrangement also applies for picture elements associated with static interlace scanned images. Before coding a dynamic image, the lines of two superimposed blocks are interchanged in accordance with FIG. **1***b*, and after decoding they are re-arranged in accordance with FIG. **1***a*.

FIG. **2** shows a known type of hybrid coder **25** for processing a signal according to the MPEG standard. An interlaced image signal from a picture n is supplied via an input **21** to inputs of a picture storage unit **22** and a motion detector **24**. Items of data (two superimposed blocks) of a picture n-1, needed by motion detector **24**, and the line sections of the respective two blocks involved, are read out from picture store **22** into a block storage unit **23**. From unit **23** coder **25** selects 8*8 blocks on each occasion. Picture elements for static images corresponding to FIG. **1***a*, and those for dynamic images corresponding to FIG. **1***b*, are stored in a buffer in block storage unit **23**.

Motion detector **24** can be implemented in accordance with various known methods. For example, the absolute value differences of picture elements from blocks having the same spatial position of picture n and picture n-1 may be formed for each block or double block that has to be coded. Alternatively, motion vectors (e.g., for two superimposed blocks on each occasion) formed by coder **25** can be used instead of the motion detector. Thus transform coder **25** may provide a Motion Vector to indicate a motion condition for rearranging the line structure of an interlaced signal. If the instantaneous sum of the absolute value differences, and/or the amount of the corresponding motion vectors for this block or these blocks, exceeds a predetermined

threshold (i.e., dynamic picture content is present), the picture elements shown in FIG. 1*b*, otherwise those corresponding to FIG. 1*a*, are stored in unit 23. Otherwise, the picture elements shown in FIG. 1*a* are stored in unit 23. A Control Signal from motion detector 24 in FIG. 2 indicating the occurrence of a rearranged line structure may be provided to transform coder 25 for adding the control signal to be coded signal.

The described re-sorting operation may be performed in accordance with the following program:

```
DO y = 1,N/2
  DO x = 1,N
    Bout1(x,y) = Bin1(x,2*y-1)
    Bout1(x,y) = Bin1(x,2*y)
  ENDDO
ENDDO
  DO y = 1,N/2
  DO x = 1,N
    Bout1(x,y + N/2) = Bin2(x,2*y-1)
    Bout1(x,y + N/2) = Bin2(x,2*y)
  ENDDO
ENDDO,
```

where B_{in1} is the block located in the higher (upper) position and N is an even number.

Coder 25 may be a standard coder such as described in CCITT H.261, and in the MPEG standard ISO/IEC 11172-2. Integrated circuit coders of this type are commercially available (eg., GEC Plessey VP 2611 and SGS-Thomson STI3230). Unit 22 may include a standard frame storage device such as may be used for image processing, and unit 23 may include a standard Random Access Memory (RAM). As noted above, unit 24 may be a standard motion detector which operates by obtaining the absolute values of pixel block differences and comparing a sum of these values to a threshold to determine the presence or absence of motion.

FIG. 3 is a flow chart illustrating a method as described above in accordance with the principles of the invention. In method step 30 an input signal is evaluated to determine if it exhibits interlaced or progressive scan form. A progressive scan signal is transformed and coded without further processing at step 32 via node 31. If an interlaced signal is detected at step 30, the interlaced signal is evaluated at step 34 to determine if it contains motion. If it does not, the interlaced signal is coupled via step 36 without rearranging its original line structure to step 32 where the interlaced signal is transformed and coded. If step 34 senses that the interlaced signal contains motion, the processing of step 36 is controlled so as to rearrange the line structure of the interlaced signal (as previously discussed). The interlaced signal with rearranged line structure is transformed and subsequently coded by step 32. In step 38 a control signal indicating a rearranged line structure when an interlaced signal with motion is detected is provided to the coding function in step 32. The coding function in step 32 may provide a motion vector to motion detection step 34 to indicate a motion condition for rearranging the line structure of an interlaced signal. Picture and block storage steps as may be required to facilitate the process illustrated by FIG. 3 have been discussed previously in connection with FIG. 2 and have not been shown to simplify FIG. 3.

FIG. 4 is a flowchart illustrating decoder processing steps associated with the coding process discussed in connection with FIG. 3. An input signal transform coded as discussed previously is decoded and inverse transformed by step 40. Before being applied to an output, the decoded signal is processed by a step 42, which rearranges the line structure back to an original structure if the signal exhibits an interlaced line format with motion. For this purpose step 44 determines if the input signal exhibits an interlaced line structure. If it does, step 46 determines if the interlaced signal contains motion. If motion is detected, a control signal is provided to step 42 to effect rearranging of the lines of the interlaced signal back to an original structure.

We claim:

1. A method for coding a signal representing an image comprising picture element (pixel) blocks of predetermined size using a hybrid coder suitable for transforming blocks of scanned pixels, comprising the steps of:

transforming progressively scanned pixel blocks independent of dynamic image content;

for static images, transforming interlaced scanned pixel blocks with an original line structure; and

for images with dynamic content, (a) rearranging the original line structure of an interlace scanned image signal so as to produce first and second vertically superimposed pixel blocks of similar predetermined size, said first block containing pixels associated with image lines of a first field, said second block containing pixels associated with image lines of an associated adjacent second field; and (b) transforming said first and second blocks.

2. A method according to claim 1, further comprising the step of:

generating a control signal indicating the occurrence of said rearranging of said line structure; and

adding said control signal to a coded signal produced by transforming said first and second blocks, for each pair of transformed first and second blocks.

3. A method according to claim 1, comprising the further step of:

rearranging said line structure in response to an output signal from a motion detector.

4. A method according to claim 1, comprising the further step of:

rearranging said line structure in response to a motion vector generated by said hybrid coder.

5. A method according to claim 1, wherein said blocks are 8×8 pixel blocks.

6. A method according to claim 5, wherein

said vertically superimposed blocks are arranged within a group of four blocks arranged in a square pattern, each block of said group comprising 8×8 luminance pixels.

7. A method according to claim 6, further comprising the step of:

generating, for each said group of four blocks, a control signal indicating the occurrence of said rearranging of said line structure; and

adding said control signal to a coded signal produced by transforming said first and second blocks, for each pair of transformed first and second blocks.

8. A method for decoding a signal representing an image comprising picture element (pixel) blocks of predetermined size, said signal having been coded using a hybrid coder suitable for transforming blocks of scanned pixels, said coding comprising the steps of: (a) transforming progressively scanned pixel blocks independent of motion, (b) transforming interlaced scanned pixel blocks with an original line structure in the pres-

ence of a static image; (c) rearranging the original line structure of an interlace scanned image signal in the presence of motion so as to produce first and second vertically superimposed pixel blocks of similar predetermined size, said first block containing pixels associated with image lines of a first field, said second block containing pixels associated with image lines of an associated adjacent second field; and (d) transforming said first and second blocks in the presence of motion; said decoding method comprising the steps of:

inverse transforming progressively scanned pixel blocks independent of image motion;

inverse transforming said interlace scanned pixel blocks with an original line structure in the presence of a static image;

inverse transforming said first and second blocks in the presence of image motion; and

rearranging said line structure of said interlace scanned image signal back to said original line structure after said inverse transforming in the presence of motion.

9. A decoding method according to claim **8** and further including the step of

evaluating a control signal indicative of said rearranging of said line structure.

10. A method for decoding a signal representing an image comprising picture element (pixel) blocks of predetermined size, said decoding method comprising the steps of:

inverse transforming progressively scanned pixel blocks independent of dynamic image content;

for static images, inverse transforming interlace scanned pixel blocks with an original line structure; and

for images with dynamic content, (a) inverse transforming first and second blocks of pixels of an interlaced scanned image, said first and second blocks being vertically superimposed pixel blocks of similar predetermined size, said first block containing pixels associated with image lines of a first field, said second block containing pixels associated with image lines of an associated adjacent second field; and (b) rearranging said line structure of said interlace scanned image signal back to said original line structure after said inverse transforming for images with dynamic content.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,422,676

DATED : June 6, 1995

INVENTOR(S) : Carsten Herpel; Heinz-Werner Keesen

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

TITLE PAGE: item [30],

Add under "Foreign Application Priority Data"

---Apr. 14, 1992 PCT/EP 92/00843---

Signed and Sealed this

Twenty-first Day of January, 1997

Attest:

BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks

Exhibit 12

US00RE35093E

United States Patent [19]

Wang et al.

[11] E Patent Number: Re. 35,093

[45] Reissued Date of Patent: Nov. 21, 1995

[54] **SYSTEMS AND METHODS FOR CODING EVEN FIELDS OF INTERLACED VIDEO SEQUENCES**

[75] Inventors: **Feng M. Wang**, Milpitas, Calif.; **Dimitris Anastassiou**, Tenafly, N.J.

[73] Assignee: **The Trustees of Columbia University In the City of New York**, New York, N.Y.

[21] Appl. No.: **353,968**

[22] Filed: **Dec. 9, 1994**

Related U.S. Patent Documents

Reissue of:

[64] Patent No.: **5,193,004**
Issued: **Mar. 9, 1993**
Appl. No.: **621,343**
Filed: **Dec. 3, 1990**

U.S. Applications:

[63] Continuation of Ser. No. 218,970, Mar. 25, 1994, abandoned.

[51] **Int. Cl.**[6] **H04N 7/36**

[52] **U.S. Cl.** **348/413**; 348/420

[58] **Field of Search** 348/402, 413, 348/420; H04N 7/133, 7/36

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,821,119	4/1989	Gharui	348/402
4,873,573	10/1989	Thomas et al.	348/416
4,897,720	1/1990	Wu et al.	348/412
4,999,705	3/1991	Puri	348/412
5,001,559	3/1991	Gonzales	348/400
5,008,746	4/1991	Bernard et al.	348/429
5,049,991	9/1991	Niihara	348/416
5,134,480	7/1992	Wang	348/620

FOREIGN PATENT DOCUMENTS

0374548 6/1990 European Pat. Off. .

Primary Examiner—Howard W. Britton
Attorney, Agent, or Firm—Brumbaugh, Graves, Donohue & Raymond

[57] **ABSTRACT**

In accordance with the invention, a method, for coding multi-mode predictive interpolative coded fields of video, includes the steps of:

(a) providing a current field of interlaced pixel data, and past and future fields of such data;

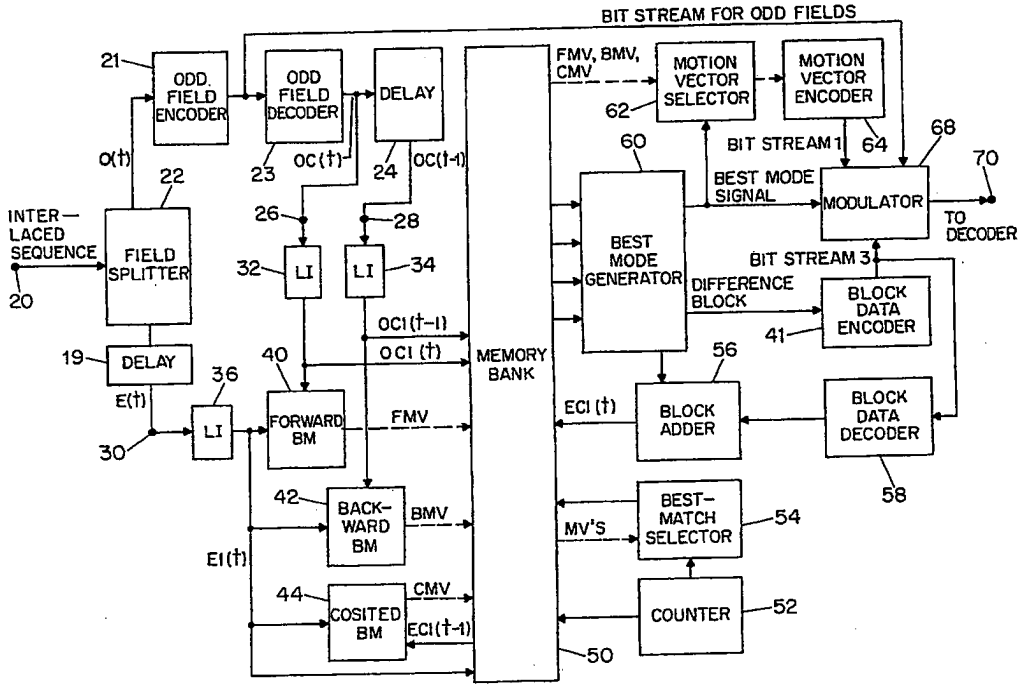
(b) providing estimated pixel data at omitted line positions in the past and future fields of data to form enhanced fields of pixel data;

(c) comparing a block of pixel data from the current field with corresponding blocks of data from such past and future fields to derive motion vector signals indicative of best matched blocks of data;

(d) developing pixel error signals representing pixel by pixel errors based on utilization of best matched blocks in different modes for comparison with the block of pixel data from the current field and developing best mode signals indicative of which of such modes represents the least overall error; and

(e) providing the best mode signals, motion vector signals, pixel error signals, and the future odd field of data for transmission for use by a decoder.

56 Claims, 9 Drawing Sheets



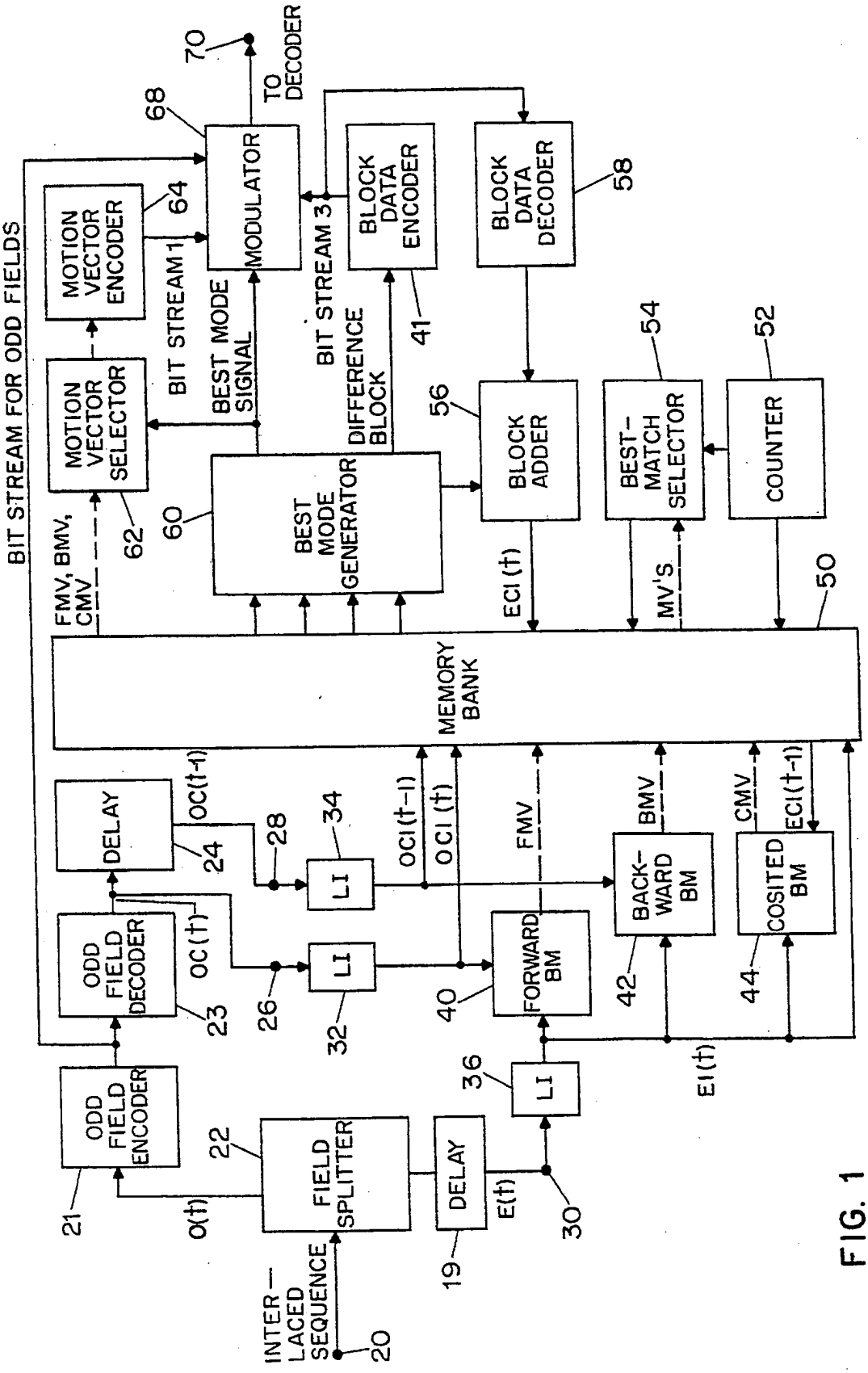

BIT STREAM FOR ODD FIELDS
70
TO DECODER
68
MODULATOR
64
MOTION VECTOR ENCODER
BIT STREAM 1
BEST MODE SIGNAL
BIT STREAM 3
BLOCK DATA ENCODER
41
BLOCK DATA DECODER
58
MOTION VECTOR SELECTOR
62
FMV, BMV, CMV
60
BEST MODE GENERATOR
DIFFERENCE BLOCK
56
BLOCK ADDER
54
BEST-MATCH SELECTOR
52
COUNTER
ECI (t)
MV'S
50
MEMORY BANK
DELAY
24
OC(t-1)
28
34
LI
OCI(t-1)
OCI (t)
FMV
BMV
CMV
ECI(t-1)
ODD FIELD DECODER
23
OC(t)
26
LI
32
FORWARD BM
40
BACK-WARD BM
42
COSITED BM
44
EI(t)
ODD FIELD ENCODER
21
O(t)
22
FIELD SPLITTER
DELAY
19
E(t)
36
LI
30
INTER-LACED SEQUENCE
20

FIG. 1

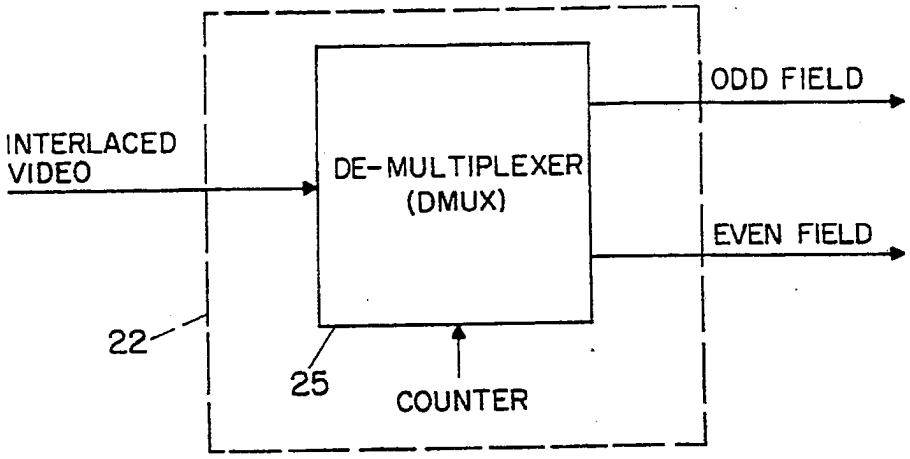


FIG. 2

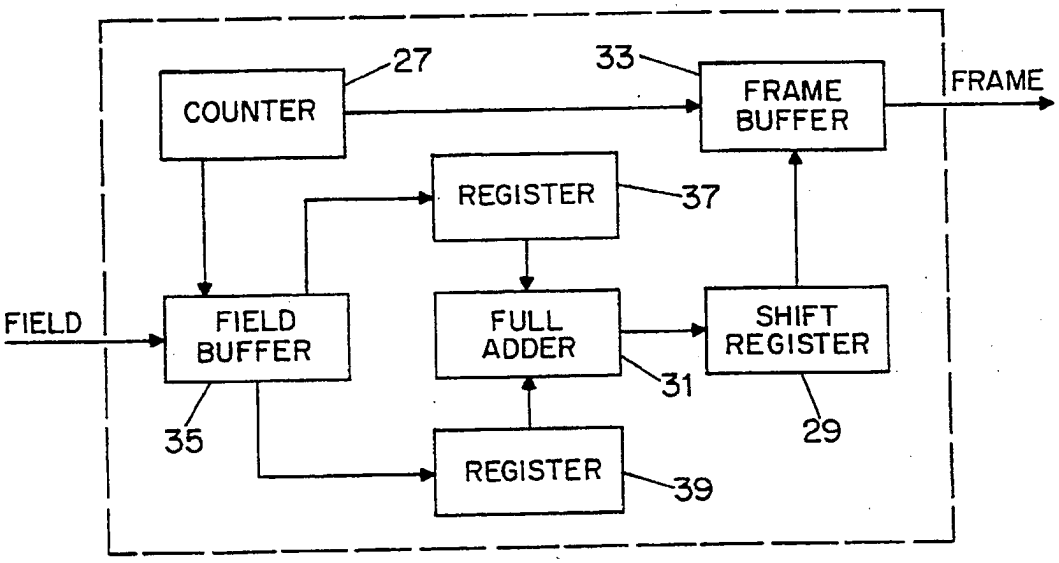


FIG. 3

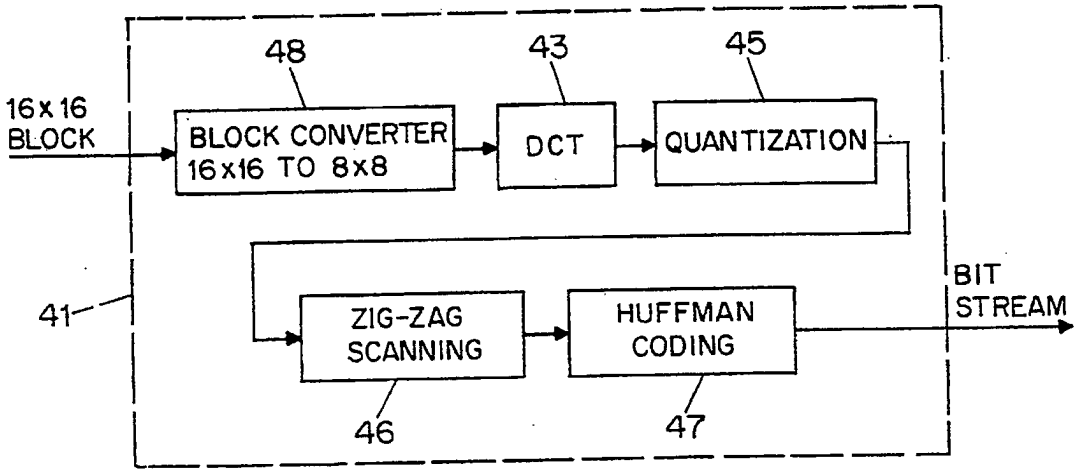


FIG. 4

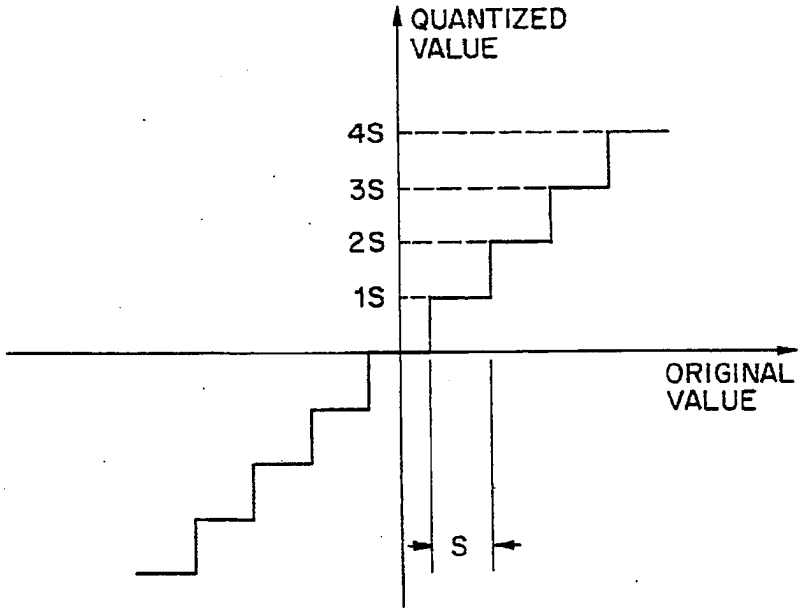

QUANTIZED VALUE
4S
3S
2S
1S
ORIGINAL VALUE
S

FIG. 5

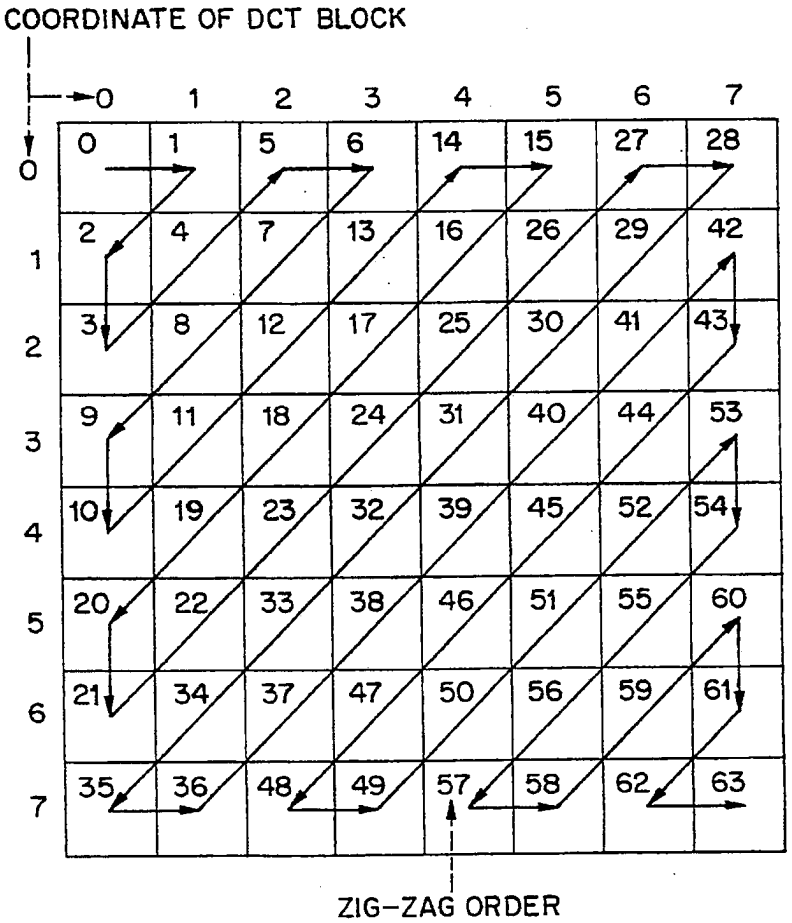

COORDINATE OF DCT BLOCK
0 1 2 3 4 5 6 7
0 1 5 6 14 15 27 28
2 4 7 13 16 26 29 42
3 8 12 17 25 30 41 43
9 11 18 24 31 40 44 53
10 19 23 32 39 45 52 54
20 22 33 38 46 51 55 60
21 34 37 47 50 56 59 61
35 36 48 49 57 58 62 63
ZIG-ZAG ORDER

FIG. 6

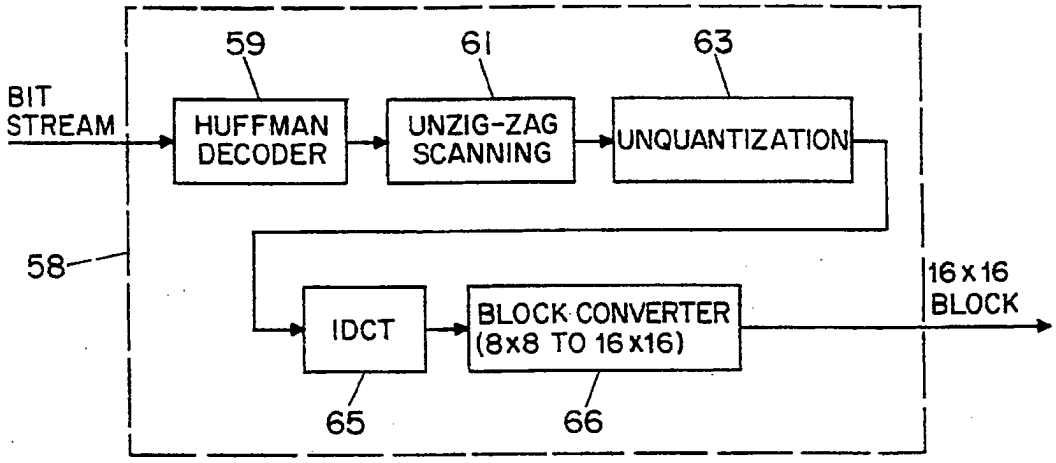

59
61
63
BIT STREAM
HUFFMAN DECODER
UNZIG-ZAG SCANNING
UNQUANTIZATION
58
16 x 16 BLOCK
IDCT
BLOCK CONVERTER (8x8 TO 16x16)
65
66

FIG. 7

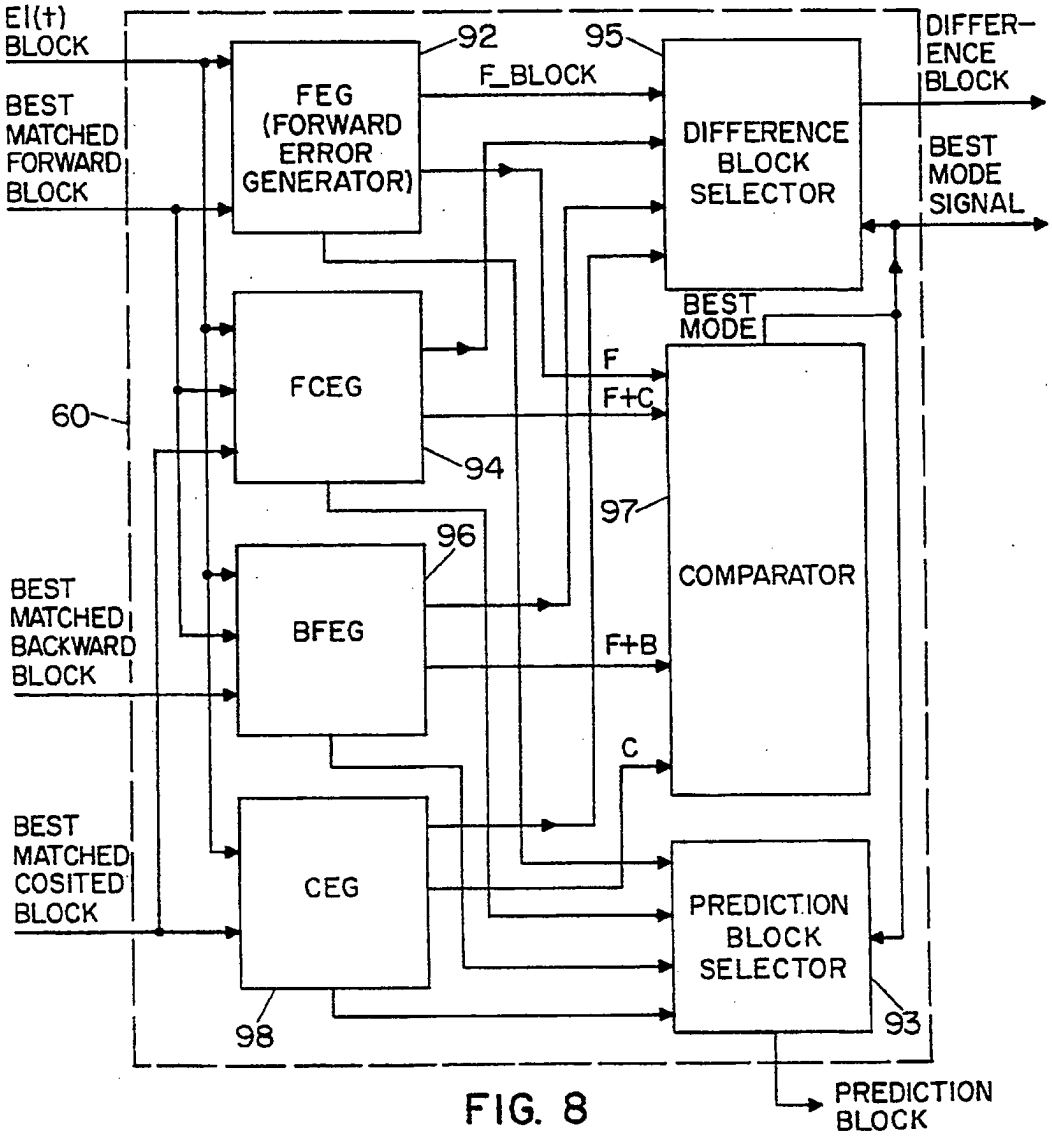

E(t) BLOCK
BEST MATCHED FORWARD BLOCK
BEST MATCHED BACKWARD BLOCK
BEST MATCHED COSITED BLOCK
92
95
F_BLOCK
FEG (FORWARD ERROR GENERATOR)
DIFFERENCE BLOCK SELECTOR
DIFFER-ENCE BLOCK
BEST MODE SIGNAL
BEST MODE
F
F+C
FCEG
60
94
97
96
BFEG
F+B
C
COMPARATOR
CEG
PREDICTION BLOCK SELECTOR
98
93
PREDICTION BLOCK

FIG. 8

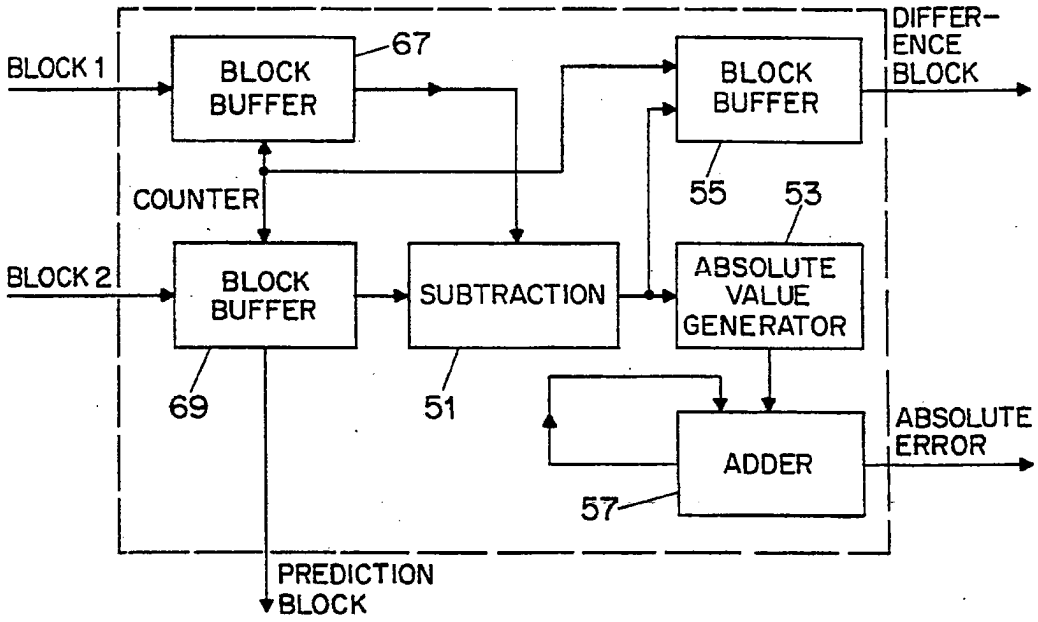

BLOCK 1
BLOCK BUFFER
67
BLOCK BUFFER
DIFFER-ENCE BLOCK
COUNTER
55
53
BLOCK 2
BLOCK BUFFER
SUBTRACTION
ABSOLUTE VALUE GENERATOR
69
51
ABSOLUTE ERROR
ADDER
57
PREDICTION BLOCK

FIG. 9

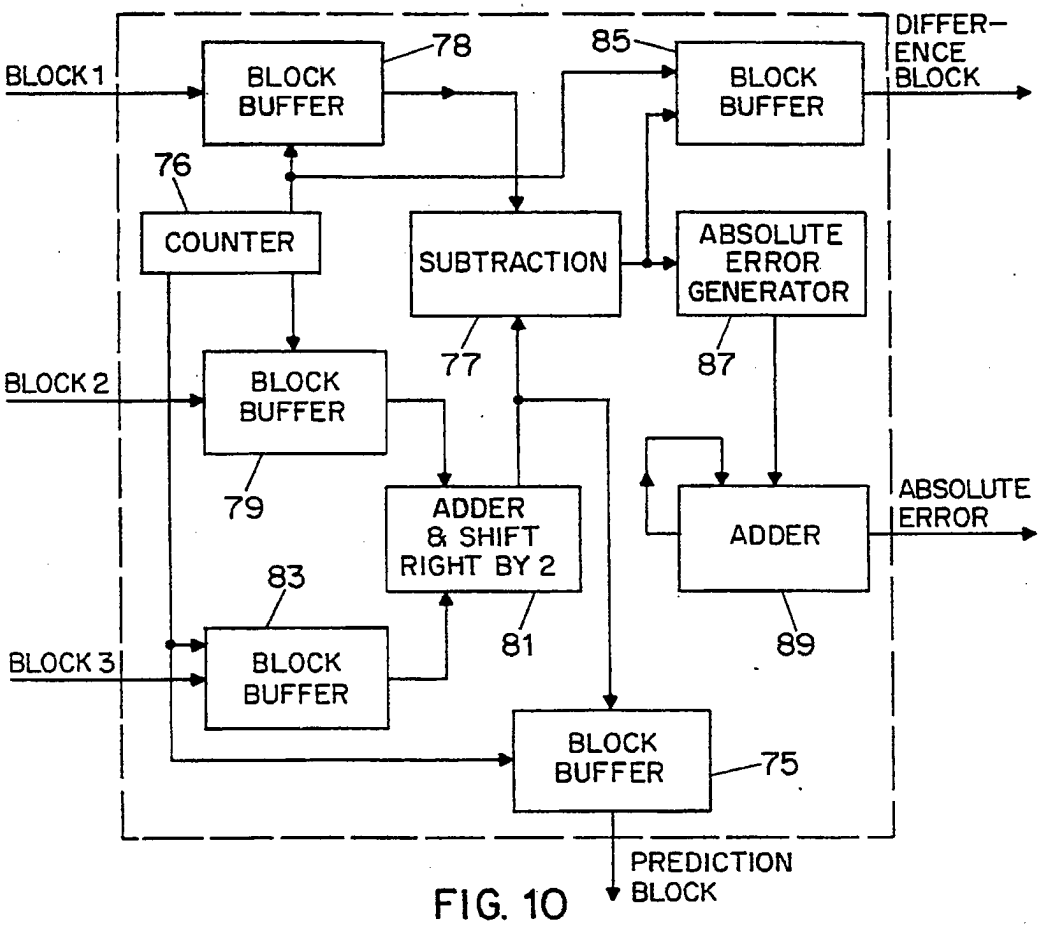

BLOCK 1
BLOCK BUFFER
78
85
BLOCK BUFFER
DIFFER-ENCE BLOCK
76
COUNTER
SUBTRACTION
ABSOLUTE ERROR GENERATOR
77
87
BLOCK 2
BLOCK BUFFER
79
ADDER & SHIFT RIGHT BY 2
ADDER
ABSOLUTE ERROR
83
81
89
BLOCK 3
BLOCK BUFFER
BLOCK BUFFER
75
PREDICTION BLOCK

FIG. 10

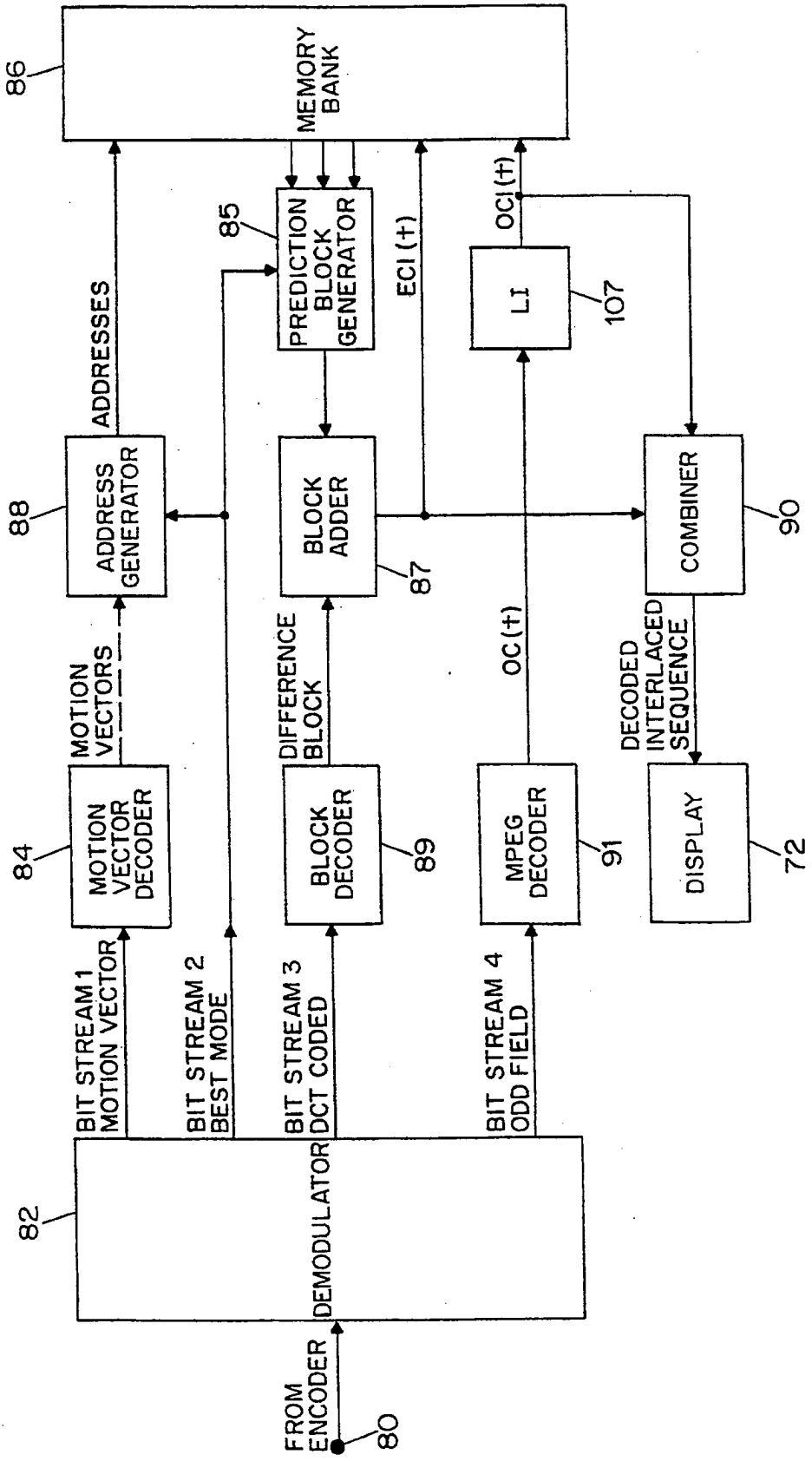

86
MEMORY BANK
85
PREDICTION BLOCK GENERATOR
ECI (+)
OCI (+)
LI
107
ADDRESSES
88
ADDRESS GENERATOR
BLOCK ADDER
87
COMBINER
90
MOTION VECTORS
DIFFERENCE BLOCK
OC (+)
DECODED INTERLACED SEQUENCE
84
MOTION VECTOR DECODER
BLOCK DECODER
89
MPEG DECODER
91
DISPLAY
72
BIT STREAM 1 MOTION VECTOR
BIT STREAM 2 BEST MODE
BIT STREAM 3 DCT CODED
BIT STREAM 4 ODD FIELD
82
DEMODULATOR
FROM ENCODER
80

FIG. 13

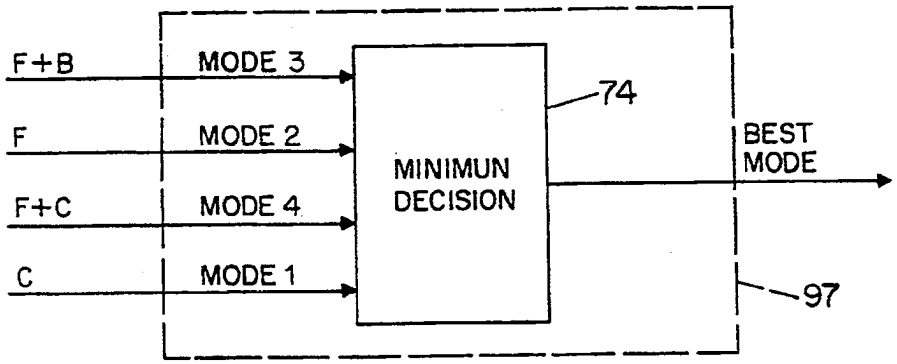


FIG. 11

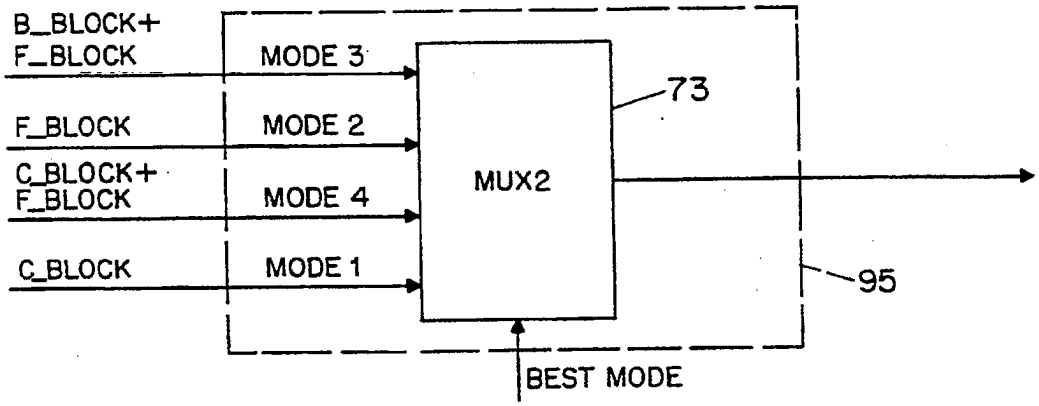


FIG. 12

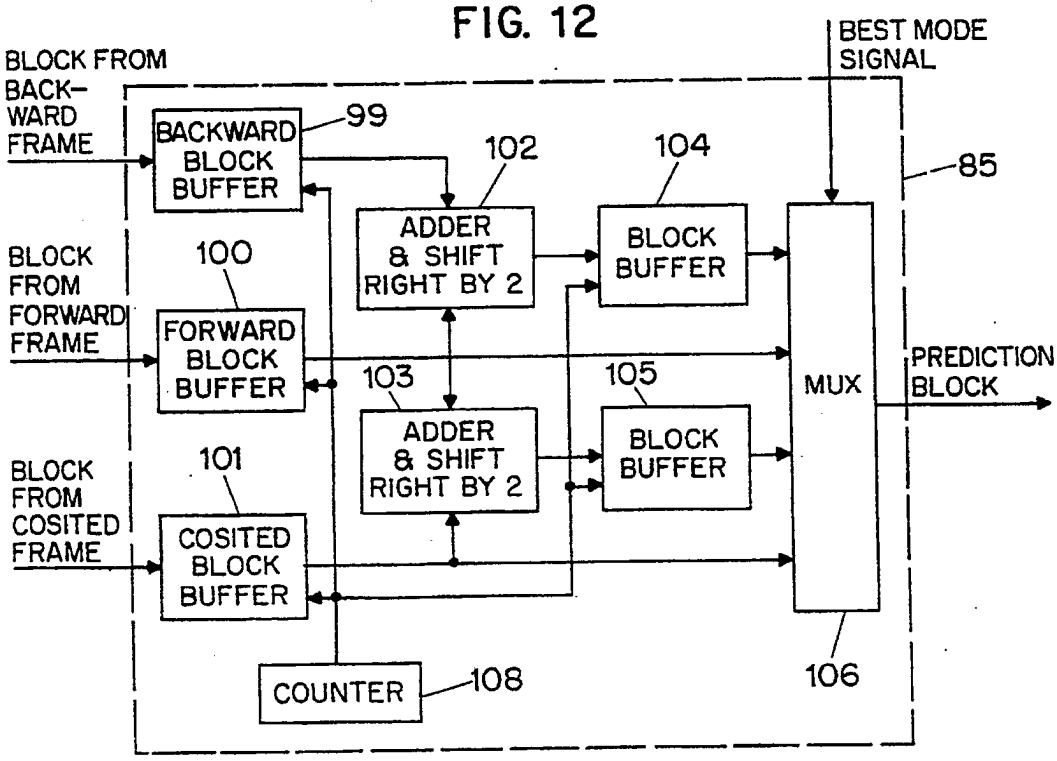


FIG. 14

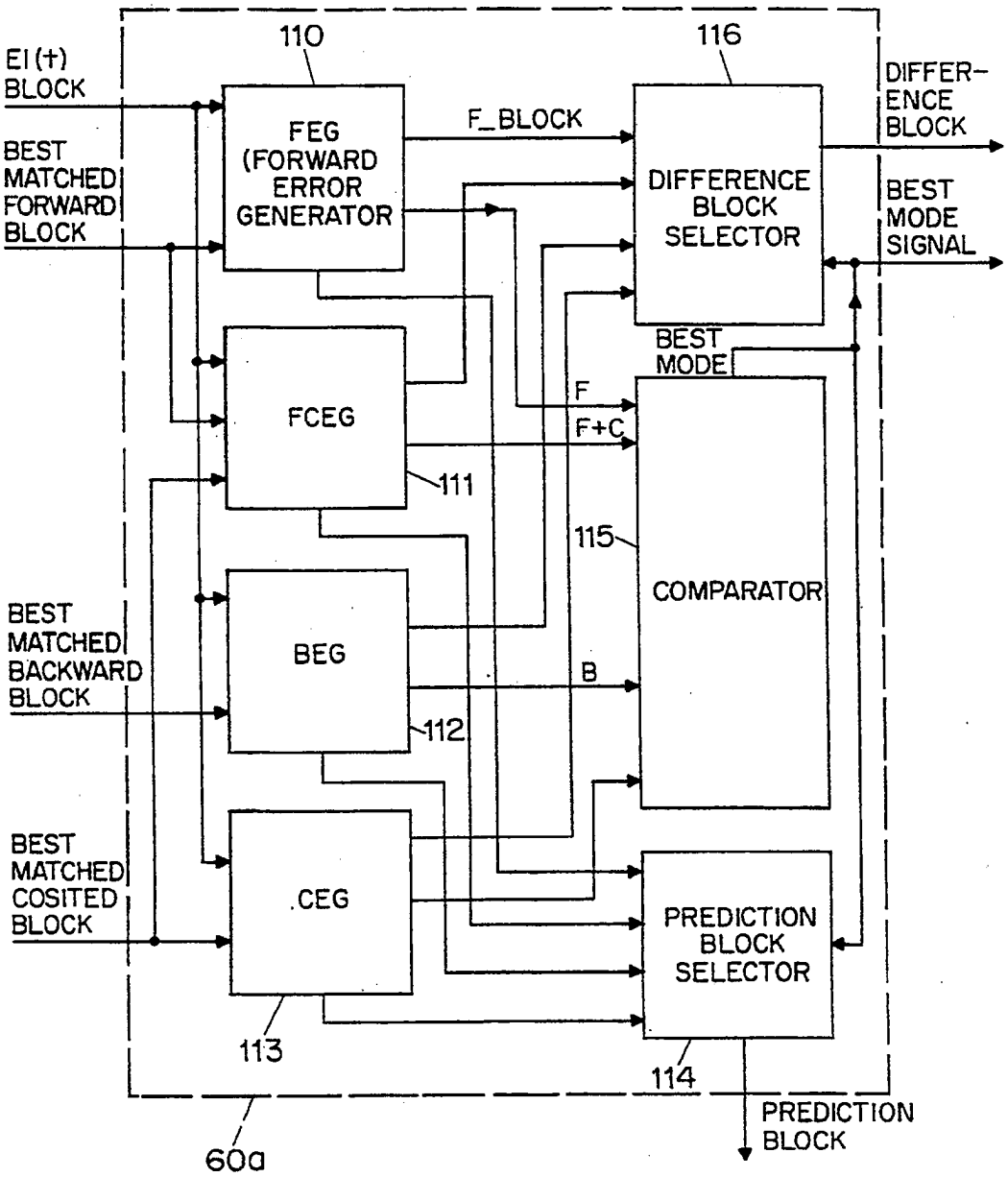

110
116
EI(t) BLOCK
BEST MATCHED FORWARD BLOCK
FEG (FORWARD ERROR GENERATOR
F_BLOCK
DIFFERENCE BLOCK SELECTOR
DIFFER-ENCE BLOCK
BEST MODE SIGNAL
BEST MODE
FCEG
F
F+C
111
115
COMPARATOR
BEST MATCHED BACKWARD BLOCK
BEG
B
112
BEST MATCHED COSITED BLOCK
CEG
PREDICTION BLOCK SELECTOR
113
114
PREDICTION BLOCK
60a

FIG. 15 (a)

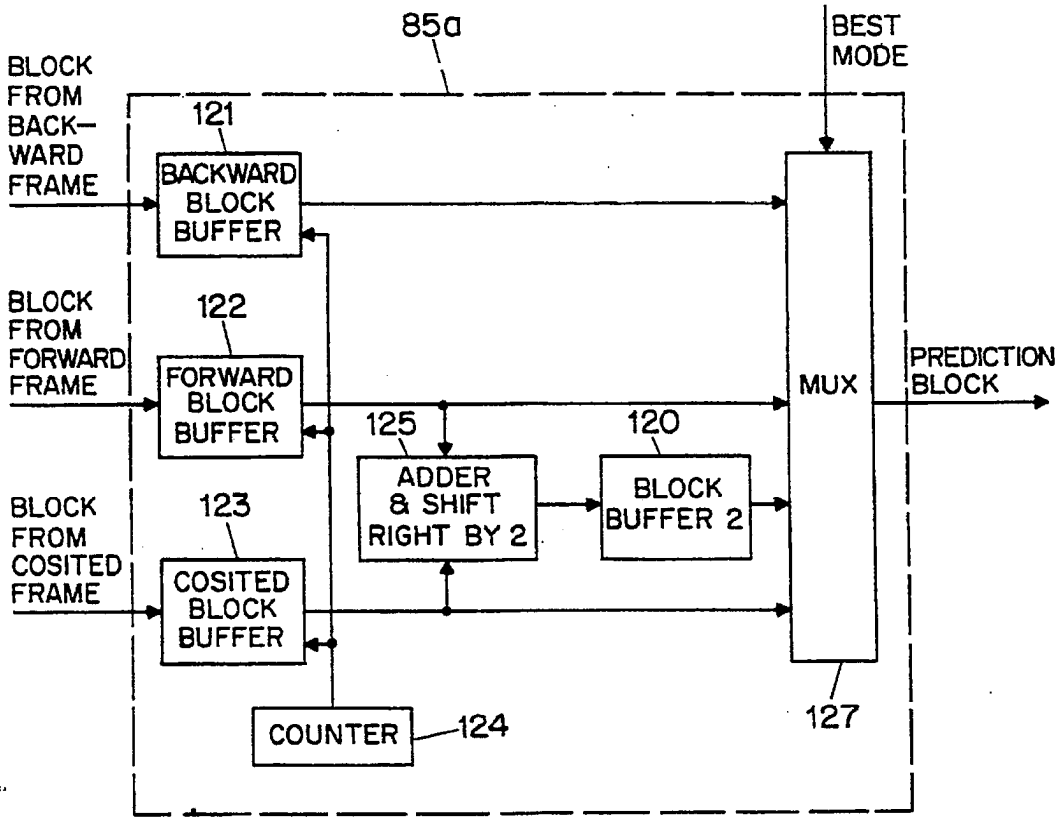

85a
BEST MODE
BLOCK FROM BACK-WARD FRAME
121
BACKWARD BLOCK BUFFER
BLOCK FROM FORWARD FRAME
122
FORWARD BLOCK BUFFER
125
ADDER & SHIFT RIGHT BY 2
120
BLOCK BUFFER 2
BLOCK FROM COSITED FRAME
123
COSITED BLOCK BUFFER
MUX
PREDICTION BLOCK
COUNTER
124
127

FIG. 15 (b)

SYSTEMS AND METHODS FOR CODING EVEN FIELDS OF INTERLACED VIDEO SEQUENCES

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

The U.S. Government has a paid-up license in this invention and the right in limited circumstances to require the patent owner to license others on reasonable terms as provided for by the terms of contract No. CDR-88-1111 awarded by the National Science Foundation.

This application is a continuation of application Ser. No. 08/218,970, filed on Mar. 25, 1994, now abandoned, and is a reissue of U.S. Pat. No. 5,193,004.

BACKGROUND OF THE INVENTION

This invention relates to methods and systems for coding alternate fields of an interlaced video format and has particular applicability to arrangements wherein the other fields have already been coded.

Interlaced scanning is an efficient method of bandwidth compression for television transmission. Further bandwidth compression can be achieved by downsampling the interlaced video sequence by deleting either all the even or all the odd fields. This scheme is used, for example, in the current Motion Picture Experts Group (MPEG) proposal relating to coding and decoding protocols for the compression of video data. In that proposed format only the odd fields of an interlaced video sequence are encoded and transmitted. The present invention, utilizing the fact that even and odd fields are highly correlated, makes it possible to code the missing even fields very efficiently.

It is therefore the object of this invention to provide methods and systems for efficiently coding one field of an interlaced video.

It is a further object of this invention to provide methods and systems for coding interlaced video data so as to permit efficient and accurate decoding using methods and systems also in accordance with the invention.

SUMMARY OF THE INVENTION

In accordance with the present invention, a system, for multi-mode predictive interpolative coding of fields of video, includes input means for coupling current and later fields of interlaced data, such fields including even fields having pixel data for line positions at which pixel data is omitted in prior and later odd fields, separator means for separating even fields of data from odd fields of data and delayed coupling means for providing past odd field data. The system also includes storage means for storing data and for providing past even field data from storage and interpolation means, coupled to receive current even, future odd and past odd fields of data, for deriving and coupling to the storage means enhanced fields of data corresponding to each of such fields of data and having estimated pixel data at omitted line positions. Block matching means are included for comparing current even enhanced field data with each of the future odd and past odd enhanced fields and past even field data to develop motion vector signals indicative of location of best matched blocks of future odd, past odd and past even data, and for coupling motion-vector signals to the storage means. The system further includes comparator means for utilizing blocks of pixel data retrieved from storage in response to motion vector signals for performing a plurality of mode comparisons of a block of current even pixel data with different ones of the best matched blocks alone or on an averaged basis for deriving a best mode signal representative of a single best mode block having the least error and deriving pixel error signals representing pixel by pixel errors in the best mode block, and output means for providing pixel error signals, best matched block location signals based on motion vector signals corresponding to the best mode signal, and odd field pixel data signals for transmission for use by a decoder.

Also in accordance with the invention a system, for decoding coded fields of video, includes input means for coupling location signals providing location data for best matched blocks, pixel error signals representative of pixel value errors in a best mode block relative to a current even field of pixel data, and odd field pixel data signals, and storage means for storing fields of pixel data, including a future odd field and past odd and even fields. Address generator means are included for providing address signals for retrieving one or more blocks of pixel data from stored future odd and past odd and even fields, and block coupling means provide a single best mode data block regardless of the number of blocks of pixel data simultaneously retrieved, and includes means for averaging simultaneously retrieved blocks of pixel data. Also included are block adder means for combining pixel error signals with the single best mode data block to provide a block of current even field pixel data, and combiner means for providing video signals including alternating odd and even fields of data.

Further in accordance with the invention, a method, for coding multi-mode predictive interpolative coded fields of video, includes the steps of:

(a) providing a current field of interlaced pixel data, and past and future fields of such data;

(b) providing estimated pixel data at omitted line positions in the past and future fields of data to form enhanced fields of pixel data;

(c) comparing a block of pixel data from the current field with corresponding blocks of data from such past and future fields to derive motion vector signals indicative of best matched blocks of data;

(d) developing pixel error signals representing pixel by pixel errors based on utilization of best matched blocks in different modes for comparison with the block of pixel data from the current field and developing best mode signals indicative of which of such modes represents the least overall error; and

(e) providing the best mode signals, motion vector signals, pixel error signals, and the future odd field of data for transmission for use by a decoder.

Also in accordance with the invention a method, for decoding coded fields of video, includes the steps of:

(a) receiving location signals providing location data for best matched blocks of data, pixel error signals representative of pixel value errors in a best mode block relative to a current even field of data, and odd field pixel data signals;

(b) storing fields of pixel data which, relative to the current even field, include a future odd field and past odd and even fields;

(c) deriving, with use of location signals, address signals used in retrieving from storage one or more blocks of pixel data from stored future odd and past odd and even fields;

(d) providing an averaging function, responsive to blocks of pixel data retrieved in step (c), to provide a single best mode data block regardless of the number of blocks of pixel data simultaneously retrieved from storage;

(e) combining the best mode data block with such pixel error signals to derive a block of current even field pixel data; and

(f) assembling even fields of data for combination with the odd fields of data to provide video signals including alternating odd and even fields.

For a better understanding of the present invention, together with other and further objects, reference is made to the following description, taken in conjunction with the accompanying drawings, and its scope will be pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows the a system diagram of an encoder in accordance with the invention.

FIG. **2** shows a field splitter useful in the FIG. **1** encoder.

FIG. **3** shows a linear interpolator useful in the FIG. **1** encoder.

FIG. **4** shows a block data encoder useful in the FIG. **1** encoder.

FIG. **5** shows a uniform quantization table used for coding block data.

FIG. **6** shows a zig-zag scanning diagram of an 8×8 DCT block.

FIG. **7** shows a block data decoder useful in the FIG. **1** encoder and the FIG. **13** decoder.

FIG. **8** shows a best mode generator useful in the FIG. **1** encoder.

FIG. **9** shows an error generator useful in the FIG. **8** best mode generator.

FIG. **10** shows an average error generator useful in the FIG. **8** best mode generator.

FIG. **11** shows a comparator useful in the FIG. **8** best mode generator.

FIG. **12** shows a block selector useful in the FIG. **8** best mode generator.

FIG. **13** is a system diagram of a decoder according to the invention.

FIG. **14** is a block coupling unit useful in the FIG. **13** decoder.

FIG. **15**(a) shows an alternative arrangement of a best mode generator useful in the FIG. **1** encoder.

FIG. **15**(b) shows a coupling unit corresponding to the FIG. **15**(a) best mode generator.

DESCRIPTION OF THE INVENTION

Referring now to FIG. **1**, there is illustrated a system for coding alternate fields of an interlaced video sequence for transmission to a decoder. Thus, for frames of video made up of successive odd and even fields of video data, the FIG. **1** system is useable for coding the even fields for example.

As used herein:

"field" refers to an incomplete frame of data, for example, the alternate fields of an NTSC television signal;

"frame" refers to a complete frame of data, for example, the composite of two fields of NTSC data;

In FIG. **1** the encoder includes input means shown as terminal **20** for receiving an interlaced video sequence and separator means, shown as field splitter **22**, for separating odd fields of data O(t) from even fields of data E(t). FIG. **2** is an illustration of a suitable field splitter. A de-multiplexer, shown as DMUX unit **25** takes an interlaced video sequence and uses a counter as a control signal. When the output of the counter is even, the "Even" output port of the 2-to-1 DMUX is selected, otherwise the "Odd" output port is selected.

The odd field data is encoded by umit **21** and provided to modulator unit **68**. Encoded odd field data is decoded by unit **23**. In this way any errors introduced by coding and decoding will be taken into account during the block matching process. Decoded odd field data is designated Oc(t).

Delayed coupling means, including delay units **19** and **24** are arranged so that when an odd field of data, denoted as Oc(t) for reference timing purposes, is supplied to a point **26**, the previous odd field of data denoted as Oc(t−1) and the even field of data E(t) are simultaneously supplied to points **28** and **30**. Thus at any given iteration of the system's operation, the fields Oc(t), Oc(t−1) and E(t) are simultaneously available at **26**, **28** and **30** respectively.

The encoder also includes interpolation means, shown as linear interpolators (LI) **32**, **34**, and **36** which may be separate channels of a single interpolation unit, effective to fill in an approximation of the pixel data at missing lines of each individual field of data by interpolation of pixel data at corresponding positions in preceding and succeeding lines of the same individual field. This provides full frames of alternating lines of actual input pixel data and interleaved lines of interpolated data, at the frame rate. These interpolated fields will be referred to as enhanced fields. Non-linear interpolation is also possible. As shown, unit **32** receives the current odd field input data Oc(t) from the separator means, via encoder unit **21** and decoder unit **23**, and its output is an enhanced field version Oci(t). Similarly, unit **34** receives past odd field Oc(t−1) from delay unit **24** and its output is an enhanced field version Oci(t−1). Similarly, interpolation unit **36** receives the current even field of input data E(t) from the separator and its output is an enhanced field version Ei(t). The interpolation means provide Oci(t), Oci(t−1) and Ei(t) to memory bank **50** and to block matching means.

Referring to FIG. **3**, there is illustrated an embodiment of an interpolation circuit suitable for units **32**, **34** and **36**. In FIG. **3**, linear interpolations are performed between two scanning lines of one field to generate the missing intermediate line. This is done by a full adder means **31** and a shift register **29** for each missing pixel. As shown, the input field containing only even or odd lines of a frame is input to field buffer **35**. Under the control of values provided by counter means, two pixels are selected which are at the same horizontal position on two consecutive lines (i.e., the lines before and after the missing line position) and stored separately in the two registers **37** and **39**. The values of the two pixels are then added in means **31** and shifted to the right by one bit one bit in shift register **29**, which is the equivalent to dividing the sum of the two pixel values by a factor of two. The same process is applied for every missing pixel of the field, sequentially. In practice, this sequence of operations is performed in parallel through use of additional adder and register combinations. The output signal of units **32**, **34** and **36** are linearly interpolated enhanced fields. As indicated, inputing Oc(t) to unit **32** results in the interpolated output Oci(t) and similarly, interpolating of input OC(t−1) results in interpolated output Oci(t−1) and interpolating of E(t) results in interpolated output Ei(t).

Block matching means, shown as forward, backward and

cosited block matching (BM) units **40, 42** and **44**, may also be separate channels of a single unit. The block matching means receive as input the enhanced fields of data Ei(t), Oci(t), Oci(t–1) and Eci(t–1). Eci(t–1), the previous even field of data, is received from memory bank **50** where it has been stored after having been derived in the previous iteration of the encoder.

The block matching means finds for each given block of pixels in Ei(t), the corresponding blocks in Oci(t), Oci(t–1) and Eci(t–1) which match the given block in Ei(t) most closely. These can be referred to as the best matched forward, backward and cosited blocks. The block matching means then calculates an appropriate motion vector to each of the identified best matching blocks and outputs that data to memory bank **50**. Thus "fmv" is the appropriate motion vector indicating which block in Oci(t) best matches the appropriate block in Ei(t). Similarly "bmv" is the appropriate motion vector indicating which block in Oci(t–1) best matches the appropriate block in Ei(t). Finally, "cmv" represents the appropriate motion vector indicating which block in Eci(t–1) best matches the appropriate block in Ei(t). In the present embodiment, blocks of 16×16 pixels are used for motion compensated block matching. Block matching techniques are known and block matching units **40, 42**, and **44** may appropriately use block matching as shown in U.S. Pat. No. 4,897,720 by Wu and Yang.

The counter **52** and best-match selector **54** use the motion vector information to generate addresses for the best matched blocks in memory bank **50** corresponding to block in Ei(t) being matched.

Memory bank **50** can be composed of random access memory (RAM) chips which have to be big enough to hold five M×N images (M and N are the width and height in terms of pixels of one image) and three sets of N/16×M/16 motion vectors.

Best mode generator means **60** receives as input each block of Ei(t) and the best matched forward, backward and cosited blocks found by the block matching means. Concurrently, motion vector selector, shown as unit **62**, receives the motion vector values for each of the best matched blocks. The best mode generator determines which of the best matched blocks most closely matches the appropriate block in Ei(t). These different comparisons are known as modes. Thus there can be a forward mode, a backward mode and a cosited mode based on a comparison of a specific block of pixel data from Ei(t) with the best matched blocks of future odd, past odd and past even pixel data, respectively, The best mode generator can also create and compare blocks which are averages of two or more of the best matched blocks which are received from the block matching means. These averaged modes can be based on any averaged combination of the best matched blocks. In certain applications, the most useful averaged modes have been found to be combinations of the past even and future odd blocks and of the past and future odd blocks from their respective enhanced fields of pixel data. The best mode generator then picks from among those modes the overall best matched block, also known as the best mode block.

After selecting the best mode block, the best mode generator generates three different outputs; the best mode block, a difference block and a signal to motion vector selector unit **62** and modulator unit **68** indicating which mode has been selected. Motion vector selector unit **62** then sends the motion vector information regarding the appropriate block or blocks (in the case of an averaged mode) to motion vector encoder **64**. Unit **64** encodes the motion vector data and provides it to modulator **68**. The motion vector encoder uses variable length coding (VLC) which is based on a look-up table that stores the binary codes for all possible motion vectors. The look-up table is custom definable, however the present invention uses the same one which is used in the current MPEG proposal.

The difference block is the result of a pixel by pixel subtraction of the values of the overall best mode block from the block in Ei(t). The difference block is then coded by block data encoder **41** and provided to modulator unit **68**. Data encoder **41** is illustrated in more detail in FIG. **4**. Unit **48** converts the 16×16 blocks received from the best mode generator to four 8×8 blocks. A discrete cosine transform is applied to the difference block data by DCT unit **43**. The transform is performed on blocks of an 8×8 size The 8×8 discrete cosine transform is defined as:

$$X(u,v) = (x)C(u)C(v)\sum_{i=0}^{7}\sum_{j=0}^{7} x(i,j)\cos\left(\frac{(2i+1)u\pi}{16}\right)\cos\left(\frac{(2j+1)v\pi}{16}\right)$$

where x(i,j), i,j=0, . . . , 7, is the pixel value, X(u,v), u,v=0, . . . , 7, is the transformed coefficient,

$$C(0) = \frac{1}{\sqrt{2}}.$$

and C(u)= 1, u,v=1, . . . , 7. DCT is well known in the art, and there are IC chips available for this purpose.

To achieve higher coding efficiency, the DCT coefficients are quantized by a uniform quantizer, shown in FIG. **5**, with a fixed step S. The values of S, which are stored in a quantization table, typically vary from one coefficient to another. While FIG. **5** shows linear quantization, non-linear quantization is also possible. In the present instance the quantization table which is used is the current MPEG standard. Other quantization tables, however, are useable. After quantization, the DCT blocks contain a large amount of zero coefficients. Known techniques of zig-zag scanning may be applied to the DCT blocks in order to maximize the runs of zero coefficients and thereby effectuate higher data compression. The zig-zag scanning is implemented by a look-up table, shown in FIG. **6**, which maps coordinates of DCT coefficient blocks to values between 0 and 63. This represents the order of variable length coding. A known form of Huffman coding may then be applied to convert the quantized DCT coefficients to binary codes. In the present instance, the MPEG VLC table is used for these purposes although other tables are also useable.

The coded difference block data is also provided to block data decoder **58** shown in FIG. **7**. The block data decoder performs the reverse operations in the reverse order of the encoder. First the coded data is Huffman decoded and next unzig-zag scanning is applied. The data is then unquantized and an inverse discrete cosine transform is applied using known techniques. The decoder uses the same tables as the encoder. The output of block data decoder **58** is provided to block adder **56**. Block adder **56** also receives the best mode block from the best mode generator. It adds the difference block to the best mode block to create the same even field which will be recreated by the decoder. That even field is then provided to memory bank **50** where it will be used as the cosited past even field by cosited block matching unit **44** during the next iteration of the system.

Modulator unit **68** then combines the four sets of data it has received (odd field data, coded motion vector data, coded difference block data and best mode signal data) and provides an appropriate signal to terminal **70**. From there the data can be sent to an appropriate decoder.

FIG. **8** illustrates a suitable embodiment of the best mode generator **60**. The best mode generator includes four error generators shown as forward error generator (FEG) **92**, average error generator (FCEG) **94**, average error generator (BFEG) **96** and cosited error generator (CEG) **98**. The error generators receive as input a block from Ei(t) and the appropriate best matched blocks.

The forward error generator FEG compares the appropriate block in Ei(t) to the best matched forward block. The cosited error generator CEG compares the appropriate block in Ei(t) to the best matched cosited block.

The average error generators receive two or more best matched blocks which they average together to produce an average block. This average block is then compared to the appropriate block in Ei(t). Thus average error generator BFEG creates a block which is the average of the best matched backwards block and the best matched forward block. Similarly the average error generator FCEG creates a block which is the average of the best matched forward block and the best matched cosited block. Averaging can be done by adding pixel values from the two blocks on a pixel by pixel basis and reducing each resulting pixel value by a factor of two (i.e. dividing each value in half.

From these inputs the error generators produce three outputs; a prediction block, a difference block and an absolute error.

The prediction block is the block which the error generator compares to the appropriate block in Ei(t). Thus in the case of FEG or CEG, the prediction block is just the best matched block received from the block matching units. In the case of the average error generators, the prediction block is the average of two or more best matched blocks. The prediction blocks are outputted to the prediction block selector **93**.

The difference block is calculated by subtracting the value of a pixel in one block from the value of the corresponding pixel in the other block on a pixel by pixel basis. This value of this difference is then assigned to a corresponding pixel in the difference block. The sum of the absolute value of all of these pixels in the difference block is the absolute error.

The difference blocks are provided to the difference block selector unit **95**. The absolute errors are outputted to comparator unit **97**. Based on the absolute errors the comparator chooses the best mode. Typically this is the mode having the least absolute error, however, other selections are possible. This is referred to as the best mode. The comparator then supplies a signal indicating the best mode to the difference block selector unit **95**, modulator unit **68**, motion vector selector unit **62** and to the prediction block selector **93**. Upon receipt of the signal the difference block selector sends the appropriate difference block to block data encoder **41**, and the prediction block selector sends the appropriate prediction block (the best mode block) to block adder **56**.

Referring to FIG. **9**, there is illustrated an embodiment of the suitable error generator circuit for either the forward error generator FEG or the cosited error generator CEG, in FIG. **9** buffer block unit **67** and buffer block unit **69** receive a block from Ei(t) and the best matched block from either Oci(t) or Eci(t–1). Subtraction unit **51** calculates the difference in value of each set of corresponding pixels in the two blocks and assigns that value to a corresponding pixel value in block buffer **55**. This is known as the difference block.

Absolute value generator **53** converts the value of the difference for each set of pixels to an absolute value and provides that information to the adder unit **57**. The adder unit **57** sums all of the absolute values for the differences of the two blocks being compared to create an absolute error value.

Referring to FIG. **10**, an embodiment of a suitable average error generator circuit is shown. Block buffer **78** receives a block in Ei(t). Block buffers **79** and **83** receive the best matched blocks from the fields being averaged to create a block. In the case of error generator BFEG, the best matched blocks from Oci(t–1) and Oci(t) are used. In the case of average error generator FCEG, the best matched blocks from Oci(t) and Eci(t–1) are used. The values of each of the corresponding pixels in each of the best matched blocks is added and divided by two to create an average block. This is accomplished by unit **81**. This average block is then subtracted from the corresponding block in Ei(t) by subtraction unit **77**. In the same fashion as the other error generators, both a difference block and an absolute error value is created.

Referring to FIG. **11**, a suitable embodiment of the comparator unit **97** is shown. Minimum decision unit **74** picks the least value of the four absolute error inputs and outputs an appropriate best mode signal. While the current embodiment picks the mode with the least possible absolute error, other decision criterion are also available.

Referring to FIG. **12**, a suitable embodiment of a difference block selector is shown. Multiplexer unit **73** receives the four difference blocks as input. Responsive to the best mode signal, unit **73** outputs the appropriate difference block.

Decoder Description

Because the implemented coding scheme is very unsymmetrical, the decoder is simpler than the encoder. This is due largely to the fact that the decoder does not have to perform block matching or make a best mode determination.

In FIG. **13**, the decoder includes input means, shown as terminal **80**, for receiving encoded data. Demodulating means, shown as demodulator unit **82** separates the encoded data into four bit streams: location signals in the form of a motion vector bit stream, a best mode signal bit stream, pixel error signals in the form of a difference block bit stream and an odd field data signal bit stream.

The first bit stream, containing the motion vector data, is decoded by a motion vector decoder **84** which uses the same VLC table as used in the encoder. The motion vector decoder **84** segments the bit stream into portions which represent one or two different motion vectors. Using the VLC table, the decoder provides the corresponding motion vectors. The motion vectors represent the displacement of the best matched blocks from the original blocks in Ei(t). The motion vector decoder supplies the motion vectors to address generator unit **88**. The address generator also receives the best mode signal from demodulator unit **82**. The address generator uses the decoded motion vectors and the best mode signal to generate memory addresses of one or more of the best matched future odd, past odd and past even blocks, depending on the specific motion vector signals and the best mode signal. These blocks are sometimes referred to as the best matched forward, backward and cosited blocks, respectively.

In an alternative arrangement, only three bit streams need to be sent. In this arrangement the best mode signal and the motion vector would be combined in to an address bit stream

which would describe where in the receiver's memory the appropriate best matched blocks could be found.

Block coupling means, shown as prediction block generator unit **85**, receives the best matched forward, backward and cosited blocks from storage means shown as memory bank **86**. It also receives the best mode signal from demodulator **82**. Unit **85** then generates the same mode data block which was identified in the encoder. The mode data block is then provided to block adder unit **87**. Referring more specifically to FIG. **14**, a suitable embodiment of block generator **85** is shown. The best matched block or blocks representing the best mode data block are received from memory bank **86** into the appropriate block buffers. In this embodiment the two average modes are created by units **102** and **103**. The two other modes which merely use best matched blocks, are already available as received in the appropriate buffers. In operation, only the best matched block or blocks needed to provide the desired best mode block are supplied to block generator unit **85**. Thus, if either the future odd block or past even block represents the best mode block, only the respective desired block is received by unit **85** and it is coupled by unit **85** to block adder unit **87**. If, however, the best mode block is the block of data representing an average of the past even block and the future odd block, those blocks are provided from memory to buffers **100** & **101**, respectively, for averaging in unit **103** and coupling to block adder unit **87**. Operation is similar via buffers **99** and **100** and unit **102**, when the best mode block represents the average of the past and future odd field best matched blocks. As illustrated, unit **85** is responsive to the best mode signal in implementing the averaging function however, in other applications unit **85** need only be arranged to simply pass through any single input block and, in response to the input of two blocks simultaneously, to provide an averaged output to unit **87** whenever two blocks are received. In operation of unit **85** as illustrated, the appropriate mode is then loaded into MUX unit **106**, which outputs the appropriate prediction block to block adder unit **87**.

Block decoder unit **89** decodes the difference blocks and then provides the difference block to the block adder unit **87** where it is added to the single best mode data block from unit **85**. Referring more specifically to FIG. **7** there is an illustration of the decoder **89**. This decoder is of the same design as the decoder unit **58** in the FIG. **1** encoder. Units **59**, **61**, **63**, and **65** respectively perform the following functions in sequence: Huffman decode, unzig-zag scan, unquantize and inverse discrete cosine transform, upon the incoming coded difference block data. Unit **66** reassembles the four 8×8 blocks into one 16×16 block.

The combination by block adder unit **87** of the best mode block and the difference block creates the coded field Eci(t). This field is then provided to memory bank **86** where it can be used to recreate the next even field. It is also provided to combiner means shown as unit **90**.

The fourth bit stream outputted by demodulator unit **82** is the coded odd field data. This data is provided to decoder unit **91**, which may provide MPEG type coding compatible with prior encoding. The decoded odd field data is provided to linear interpolator **107** which operates in the same fashion as the linear interpolator units in the encoder. Thus enhanced field of data Oci(t) is created and sent to combiner unit **90** and memory bank **86**. Memory bank **86** uses Oci(t) and Oci(t−1) pixel field data which was created in the system's previous iteration, to generate the appropriate blocks for block coupling means **85**. As previously mentioned, Eci(t) and hence Eci(t−1) are available also from storage in memory bank **86**.

Combiner unit **90** drops half the lines out of both the even and odd enhanced fields of data it receives. Eci(t) and Oci(t) and sequentially combines them to provide reconstruction of the interlaced sequence of data that was originally inputed into terminal **20** of the encoder. As shown in FIG. **13**, the interlaced video data is supplied to delay unit **72** to permit viewing of the video sequence.

The term "best mode" as used herein is used to identify a selected mode. Normally the mode selection is made to minimize pixel error signals to be transmitted to a decoder, however, the term is used to include reference to any available mode selected for use in a particular application.

Combinations of modes, other than those described above are also available. FIG. **15**(a) shows an arrangement of a best mode generator which uses a different set of modes. The FIG. **15**(a) best mode generator compares the appropriate block in Ei(t) to the best matched future odd block, the best matched past odd block, the best matched past even block and to a block which is the average of the best matched future odd block and the best matched past even block. Error generator **110–113** carry out the appropriate comparisons. The other operations of the FIG. **15**(a) best mode generator block are similar to that of the FIG. **8** best mode generator block.

FIG. **15**(b) shows a suitable embodiment of a prediction block generator corresponding to the FIG. **15**(a) best mode generator. Unit **125** generates the average of the future odd and past even best matched blocks while units **121–123** couple as appropriate the best matched past odd, future odd and past even blocks to unit **127**. Unit **127** outputs the appropriate block responsive to the best mode signal.

Other arrangements are also possible. Original odd field data can be used for block matching purposes even if the odd field is being coded.

In another arrangement, the best mode generator could make comparisons based on only the past even field and the future odd field. Thus the best mode generator would require only 3 inputs.

In another alternative arrangement, the data received at terminal **20** can be interlaced data which has been compressed in to fall frames of data. In arrangements of this type, field delay unit **19** is not necessary.

In summary, methods and systems according to the invention contain various modes of operation. The following four modes were found to be most useful, but it is possible to have more, at the expense of increased complexity, including intrafield, backward, or even three-way averaging.

1. A "recursive", predictive, mode in which the past cosited even field is used for prediction. A motion vector must be sent, which often has zero values for stationary objects.

2. A "forward" mode, in which the future odd field is used for prediction. A motion vector must be sent.

3. An "averaged" mode, in which both past and future odd fields are used, by averaging the pixel values of the two optimum blocks. In that case, two motion vectors must be sent.

4. A "recursive averaged" mode, in which the previous even cosited field is combined as above, with the future odd field.

Methods and systems according to the invention, when combined with appropriate coding of the progressive sequence resulting from dropping the even fields of interlaced video, yields high quality compression with reasonable encoder complexity. This technique can be used for about 5 Mbits/s coding of standard-quality video coding, or

for high-compression distribution quality digital HDTV coding. Coding the quantized DCT coefficients must be optimized depending on their statistical nature, which, in turn, depends on the desired quality of the final reconstructed signal. If horizontal downsampling is avoided, then the resulting asymmetry between the horizontal and vertical frequencies must be considered when coding the DCT blocks, for optimum results. We have used 16×16 blocks for motion estimation and 8×8 blocks for DCT coding, but other configurations may be optimum, depending on the application, including, e.g., a quadtree-based segmented block matching approach using both 16×16 and 8×8 blocks. In our simulations, we have found that the even fields are coded with about 60% of the bit rate of the odd fields, with the same quality. The same concept can be used for HDTV coding at low bit rates (e.g. below 20 Mbits/s). There are various proposals for HDTV coding, using at least 70 Mbits/s. We also found that nonlinear edge preserving noise smoothing preprocessing greatly enhances coding performance, particularly in the case of coding noisy HDTV video signals.

While there have been described what are believed to be the preferred embodiments of the invention, those skilled in the art will recognize that other and further modifications may be made thereto without departing from the of the invention, and it is intended to claim all such embodiments as fall within the true scope of the invention.

We claim:

1. A system, for multi-mode predictive interpolative coding of fields of video, comprising:

input means for coupling current and later fields of interlaced data, such fields including even fields having pixel data for line positions at which pixel data is omitted in prior and later odd fields;

separator means, coupled to said input means, for separating said even fields of data from said odd fields of data;

delayed coupling means, coupled to said separation means to receive odd fields of data, for providing past odd field data;

storage means for storing data and for providing past even field data from storage;

interpolation means, coupled to said separation means and delayed coupling means to receive current even, future odd and past odd fields of data, for deriving and coupling to said storage means enhanced fields of data corresponding to each of said fields of data and having estimated pixel data at omitted line positions;

block matching means, coupled to said interpolation means and storage means, for comparing said current even enhanced field data with each of said future odd and past odd enhanced fields and said past even field data to develop motion vector signals indicative of location of best matched blocks of future odd, past odd and past even data, and for coupling said motion-vector signals to said storage means;

comparator means, coupled to said storage means, for utilizing blocks of pixel data retrieved from said storage means in response to said motion vector signals for performing a plurality of mode comparisons of a block of current even pixel data with different ones of said best matched blocks alone or on an averaged basis for deriving a best mode signal representative of a single best mode block having the least error and deriving pixel error signals representing pixel by pixel errors in said bets mode block; and

output means, coupled to said comparator means and separator means, for providing said pixel error signals, best matched block location signals based on motion vector signals corresponding to said best mode signal, and odd field pixel data signals for transmission for use by a decoder.

2. An encoding and decoding system, comprising:

(a) a system in accordance with claim 1, for coding fields of interlaced video to provide output signals; and

(b) a system, for decoding said output signals, comprising:

input means for coupling said output signals;

storage means, coupled to said input means, for

storing fields of pixel data, including a future odd field and past odd and even fields;

address generator means, responsive to said location signals, for providing address signals to said storage means for retrieving one or more blocks of pixel data from said stored future odd and past odd and even fields;

block coupling means, responsive to blocks of data retrieved from said storage means, for providing a single best mode data block regardless of the number of blocks of pixel data simultaneously retrieved, and including means for averaging simultaneously retrieved blocks of pixel data;

block adder means, coupled to said input means and block coupling means, for combining said pixel error signals with said single best mode data block to provide a block of current even field pixel data; and

combiner means, responsive to blocks of said current even field data and to said odd fields of pixel data, for providing video signals including alternating odd and even fields of data.

3. A coding system in accordance with claim 1, wherein said output means also provides said best mode signals for transmission for use by a decoder.

4. A coding system in accordance with claim 1, wherein said comparator means includes means for averaging blocks of pixel data from a past even field and a future odd field in deriving said best mode signal.

5. A system m accordance with claim 1, wherein said comparator means includes means for averaging blocks of pixel data from a past even field and a future odd field and averaging blocks of such data from past and future odd fields in denying said best mode signal.

6. A cooing system in accordance with claim 1, 4 or 5 wherein said comparator means includes means for averaging blocks of pixel data by adding two blocks of data on a pixel by pixel basis and reducing each resulting pixel value by a factor of two.

7. A coding system in accordance with claim 1, wherein said comparator means comprises:

first error generator means for deriving pixel error signals based on comparison of a block of current even field data with an average data block obtained by averaging a block of past even field data and a block of future odd field data.

8. A coding system in accordance with claim 7, wherein said comparator means additionally comprises:

second error generator means for deriving pixel error signals based on comparison of a block of current even field data with a block of past even field data.

9. A coding system in accordance with either of claims 7 or 8, wherein said comparator means additionally comprises:

third error generator means for denying pixel error signals based on comparison of a block of current even field data with an average data block obtained by averaging a block of past odd field data and a block of future odd field data.

10. A coding system in accordance with either of claims **7** or **8**, wherein said comparator means additionally comprises:

fourth error generator means for deriving pixel error signals based on a comparison of a block of current field data with a block of future odd field data; and

means for comparing the overall error represented by each of said pixel error signals to derive a best mode signal indicative of the pixel error signal representing the least overall error.

11. A system, for multi-mode predictive interpolative coding of fields of video, comprising:

input means for coupling current and later fields of interlaced data, such fields including current even fields having pixel data for line positions at which pixel data is omitted in past and future odd fields;

separator means, coupled to said input means, for separating said even fields of data from said odd fields of data;

delayed coupling means, coupled to said separation means to receive odd fields of data, for providing past odd field data;

storage means for storing data and for providing past even field data from storage;

block matching means, coupled to said separation means, delayed coupling means and storage means, for comparing current even field data with each of said future odd and past odd and even field data to develop motion vector signals indicative of locations of best matched blocks of future odd, past odd and past even data, and for coupling said motion-vector signals to said storage means;

comparator means, coupled to said storage means, for utilizing blocks of pixel data retrieved from said storage means in response to said motion vector signals for performing a plurality of mode comparisons of a block of current even pixel data with different ones of said best matched blocks alone or on an averaged basis for deriving a best mode signal representative of a single best mode block having the least error and deriving pixel error signals representing pixel by pixel errors in said best mode block; and

output means, coupled to said comparator means and separator means, for providing said pixel error signals, best matched block location signals based on motion vector signals corresponding to said best mode signal, and odd field pixel data signals for transmission for use by a decoder.

12. A coding system in accordance with claim **11**, wherein said comparator means includes means for averaging blocks of pixel data from a past even field and a future odd field in deriving said best mode signal.

13. A system, for decoding coded fields of video, comprising:

input means for coupling location signals providing location data for best matched blocks, pixel error signals representative of pixel value errors in a best mode block relative to a current even field of pixel data, and odd field pixel data signals;

storage means, coupled to said input means, for storing fields of pixel data, including a future odd field and past odd and even fields;

address generator means, responsive to said location signals, for providing address signals to said storage means for retrieving one or more blocks of pixel data from said stored future odd and past odd and even fields;

block coupling means, responsive to blocks of data retrieved from said storage means, for providing a single best mode data block regardless of the number of blocks of pixel data simultaneously retrieved, and including means for averaging simultaneously retrieved blocks of pixel data;

block adder means, coupled to said input means and block coupling means, for combining said pixel error signals with said single best mode data block to provide a block of current even field pixel data; and

combiner means, responsive to blocks of said current even field data and to said odd fields of pixel data, for providing video signals including alternating odd and even fields of data.

14. A decoding system in accordance with claim **13**, additionally comprising interpolation means, responsive to said odd fields of pixel data, for deriving and coupling to said storage means enhanced fields of data corresponding to said odd fields of data and having estimated pixel data inserted at omitted line positions.

15. A receiver, for decoding and displaying fields of video, comprising:

a decoder in accordance with claim **13**; and

display means for displaying said video signals.

16. A decoding system in accordance with claim **13**, wherein signals coupled by said input means also include best mode signals indicative of a block of data representing the least overall error and wherein said best mode signals are coupled to said address generator means for use in deriving address signals and to said block coupling means for controlling operation of said averaging means.

17. A decoding system in accordance with claim **16** wherein said input means couples location signals comprising motion vector signals.

18. A decoding system in accordance with claim **13**, wherein said block coupling means includes means for averaging blocks of pixel data from a past even field and a future odd field for deriving a best mode data block.

19. A decoding system in accordance with claim **13**, wherein said block coupling means includes means for averaging blocks of pixel data from a past even field and a future odd field, and means for averaging blocks of pixel data from a past odd field and a future odd field, for deriving a best mode data block.

20. A decoding system in accordance with claim **13**, wherein said block coupling means includes means for averaging blocks of pixel data when two blocks of such data are simultaneously retrieved, and for coupling to an output without modification singly retrieved blocks of such data.

21. A decoding system in accordance with claim **13**, **18**, **19** or **20** wherein said block coupling means includes means for averaging blocks of pixel data by adding two blocks of data on a pixel by pixel basis and reducing each resulting pixel value by a factor of two.

22. A method, for coding multi-mode predictive interpolative coded fields of video, comprising the steps of:

(a) providing a current field of interlaced pixel data, and past and future fields of such data;

(b) providing estimated pixel data at omitted line posi-

tions in said past and future fields of data to form enhanced fields of pixel data;

(c) comparing a block of pixel data from said current field with corresponding blocks of data from said past and future fields to derive motion vector signals indicative of best matched blocks of data;

(d) developing pixel error signals representing pixel by pixel errors based on utilization of said best matched blocks in different modes for comparison with said block of pixel data from said current field and developing best mode signals indicative of which of said modes represents the least overall error; and

(e) providing said best mode signals, motion vector signals, pixel error signals, and said future field of data for transmission for use by a decoder.

23. A decoding method comprising:

(a) receiving signals provided in accordance with claim **22**, including pixel error signals representative of pixel value errors in a best mode block relative to a current even field of data;

(b) storing fields of pixel data which, relative to said current even field, include a future odd field and past odd and even fields;

(c) deriving, with use of said location signals, address signals used in retrieving from storage one or more blocks of pixel data from said stored future odd and past odd and even fields;

(d) providing an averaging function, responsive to blocks of pixel data retrieved in step (c), to provide a single best mode data block regardless of the number of blocks of pixel data simultaneously retrieved from storage;

(e) combining said best mode data block with said pixel error signals to derive a block of current even field pixel data; and

(f) assembling even fields of data for combination with said odd fields of data to provide video signals including alternating odd and even fields.

24. A method in accordance with claim **22**, wherein the fields of pixel data provided in step (a) include a current even field, a future odd field and past odd and even fields of data and step (d) includes a comparison mode in which said block of pixel data from said current even field is compared with a block of data representing an average of corresponding blocks of data from said future odd and past even fields of data.

25. A method in accordance with claim **22**, wherein the fields of pixel data provided in step (a) include a current even field, a future odd field and past odd and even fields of data and step (d) includes a comparison mode in which said block of pixel data from said current even field is compared with a block of data representing an average of corresponding blocks of data from said future odd and past even fields of data and an additional comparison mode in which said current even field block is compared with a block of data representing an average of corresponding blocks of data from said past and future odd fields of data.

26. A method in accordance with claim **22**, **24** or **25** additionally comprising the step of receiving an interlaced video signal and separating said signal into odd and even fields of interlaced pixel data.

27. A method in accordance with claim **22**, **24** or **25** additionally comprising the steps of storing and retrieving fields of pixel data and motion vector signals.

28. A method in accordance with claim **22**, **24** or **25** additionally comprising the steps of compression coding

odd fields of pixel data and combining best mode signals, motion vector signals, pixel error signals and said coded odd fields into a combined signal for transmission for use by a decoder.

29. A method, for coding multi-mode predictive interpolative coded fields of video, comprising the steps of:

(a) providing a current field of interlaced pixel data, and past and future fields of such data;

(b) comparing a block of pixel data from said current field with corresponding blocks of data from said past and future fields to derive motion vector signals indicative of best matched blocks of data;

(c) developing pixel error signals representing pixel by pixel errors based on utilization of said best matched blocks in different modes for comparison with said block of pixel data from said current field and developing best mode signals indicative of which of said modes represents the least overall error; and

(d) providing said best mode signals, motion vector signals, pixel error signals, and said future field of data for transmission for use by a decoder.

30. A method, for decoding coded fields of video, comprising the steps of:

(a) receiving location signals providing location data for best matched blocks of data, pixel error signals representative of pixel value errors in a best mode block relative to a current even field of data, and odd field pixel data signals;

(b) storing fields of pixel data which, relative to said current even field, include a future odd field and past odd and even fields;

(c) deriving, with use of said location signals, address signals used in retrieving from storage one or more blocks of pixel data from said stored future odd and past odd and even fields;

(d) providing an averaging function, responsive to blocks of pixel data retrieved in step (c), to provide a single best mode data block regardless of the number of blocks of pixel data simultaneously retrieved from storage;

(e) combining said best mode data block with said pixel error signals to derive a block of current even field pixel data; and

(f) assembling even fields of data for combination with said odd fields of data to provide video signals including alternating odd and even fields.

31. A decoding method in accordance with claim **30**, additionally comprising the step of decoding said odd fields of pixel data in a manner compatible with data compression coding provided prior to data transmission.

32. A decoding method in accordance with claim **30**, wherein said signals received in step (a) also include best mode signals indicative of a block of data representing the least overall error, and wherein said best mode signals are made available for use in deriving address signals in step (e) and for controlling said averaging function in step (d).

33. A decoding method in accordance with claim **32**, wherein step (d) includes averaging on a pixel by pixel basis corresponding blocks of data from said future odd and past odd blocks of data, when said two blocks of data are simultaneously retrieved in step (c).

34. A decoding method in accordance with claim **30**, wherein step (d) includes averaging on a pixel by pixel basis corresponding blocks of data from said future odd and past even blocks of data, when said two blocks of data are

simultaneously retrieved in step (c).

35. A decoding method in accordance with claim **30, 34** or **33** wherein said step (d) includes averaging blocks of data, when two blocks are simultaneously retrieved in step (c), by adding said two blocks on a pixel by pixel basis and reducing each resulting pixel value by a factor of two.

36. A system, for multi-mode predictive interpolative coding of fields of video, comprising:

input means for coupling current and later fields of interlaced data, such fields including current even fields having pixel data for line positions at which pixel data is omitted in past and future odd fields;

separator means, coupled to said input means, for separating said even fields of data from said odd fields of data;

storage means for storing data and for providing the nearest in time past even field data then available, relative to said current even field of data;

block matching means, coupled to said separation means and storage means, for comparing current even field data with said future odd and past even field data to develop motion vector signals indicative of locations of best matched blocks of future odd and past even data, and for coupling said motion-vector signals to said storage means;

comparator means, coupled to said storage means, for utilizing blocks of pixel data retrieved from said storage means in response to said motion vector signals for performing a plurality of mode comparisons of a block of current even pixel data with different ones of said best matched blocks alone or on an averaged basis for deriving a best mode signal representative of a single best mode block having the least error and deriving pixel error signals representing pixel by pixel errors in said best mode block; and

output means, coupled to said comparator means and separator means, for providing said pixel error signals, best matched block location signals based on motion vector signals corresponding to said best mode signal, and odd field pixel data signals for transmission for use by a decoder.

37. A system, for multi-mode predictive interpolative coding of fields of video, comprising:

input means for coupling current and later fields of interlaced data, such fields including current even fields having pixel data for line positions at which pixel data is omitted in past and future odd fields;

separator means, coupled to said input means, for separating said even fields of data from said odd fields of data;

delayed coupling means, coupled to said separation means to receive odd fields of data, for providing the nearest in time past odd field data then available, relative to said current even field of data;

storage means for storing data and for providing the nearest in time past odd field data then available, relative to said current even field of data;

block matching means, coupled to said separation means and storage means, for comparing current even field data with said future odd and even past field data to develop motion vector signals indicative of locations of best matched blocks of future odd and past even data, and for coupling said motion-vector signals to said storage means;

comparator means, coupled to said storage means, for utilizing blocks of pixel data retrieved from said storage means in response to said motion vector signals for performing a plurality of mode comparisons of a block of current even pixel data with different ones of said best matched blocks alone or on an averaged basis for deriving a best mode signal representative of a single best mode block having the least error and deriving pixel error signals representing pixel by pixel errors in said best mode block; and

output means, coupled to said comparator means and separator means, for providing said pixel error signals, best matched block location signals based on motion vector signals corresponding to said best mode signal, and odd field pixel data signals for transmission for use by a decoder.

38. A coding system in accordance with claim **36** or **37**, wherein said comparator means includes means for averaging blocks of pixel data from a past even field and a future odd field in denying said best mode signal.

39. A coding system in accordance with claim **36** or **37**, additionally including interpolation means, coupled to said separation means, for deriving and coupling to said block matching means odd and even field data corresponding to odd and even fields of data having estimated pixel data at omitted line positions.

[40. A system, for decoding coded fields of video, comprising:

input means for coupling location signals providing location data for best matched blocks, pixel error signals representative of pixel value errors in a best mode block relative to a current even field of pixel data, and odd field pixel data signals;

storage means, coupled to said input means, for storing fields of pixel data, including a future odd field and a past even field;

address generator means, responsive to said location signals, for providing address signals to said storage means for retrieving one or more blocks of pixel data from said stored future odd and past even fields;

block coupling means, responsive to blocks of data retrieved from said storage means, for providing a single best mode data block regardless of the number of blocks of pixel data simultaneously retrieved, and including means for averaging simultaneously retrieved blocks of pixel data;

block adder means, coupled to said input means and block coupling means, for combining said pixel error signals with said single best mode data block to provide a block of current even field pixel data; and

combiner means, responsive to blocks of said current even field data and to said odd fields of pixel data, for providing video signals including alternating odd and even fields of data.**]**

[41. A decoding system in accordance with claim **40**, wherein said block coupling means includes means for averaging blocks of pixel data from a past even field and a future odd field for deriving a best mode data block.**]**

[42. A decoding system in accordance with claim **40**, wherein said block coupling means includes means for averaging blocks of pixel data when two blocks of such data are simultaneously retrieved, and for coupling to an output without modification singly retrieved blocks of such data.**]**

[43. A method, for decoding coded fields of video, comprising the steps of:

(a) receiving location signals providing location data for best matched blocks of data, pixel error signals repre-

sentative of pixel value errors in a best mode block relative to a current even field of data, and odd field pixel data signals;

(b) storing fields of pixel data which, relative to said current even field, include a future odd field and past even fields;

(c) deriving, with use of said location signals, address signals used in retrieving from storage one or more blocks of pixel data from said stored future odd and past even fields;

(d) providing an averaging function, responsive to blocks of pixel data retrieved in step (c), to provide a single best mode data block regardless of the number of blocks of pixel data simultaneously retrieved from storage;

(e) combining said best mode data block with said pixel error signals to derive a block of current even field pixel data; and

(f) assembling even fields of data for combination with said odd fields of data to provide video signals including alternating odd and even fields.]

[44. A decoding method in accordance with claim 43, wherein said signals received in step (a) also include best mode signals indicative of a block of data representing the least overall error, and wherein said best mode signals are made available for use in deriving address signals in step (c) and for controlling said averaging function in step (d).]

[45. A decoding method in accordance with claim 43, wherein step (d) includes averaging on a pixel by pixel basis corresponding blocks of data from said future odd and past even blocks of data, when said two blocks of data are simultaneously retrieved in step (c).]

46. A method, for decoding coded fields of video data, wherein frames of video data consist of first and second fields of video data, comprising the steps of:

(a) receiving location signals providing location data for best matched blocks of data, pixel error signals representative of pixel value errors in a best mode block relative to a first field of a current frame of data, and second field data signals;

(b) selecting, with use of said location signals, one or more blocks of pixel data from a second field of said current frame and a first field of a past frame of data;

(c) providing an averaging function, responsive to blocks of pixel data selected in step (b), to provide a single best mode data block regardless of the number of blocks of pixel data selected;

(d) combining said single best mode data block with said pixel error signals to derive a block of first field of a current frame pixel data; and

(e) assembling first fields of data for combination with said second fields of data to provide video signals including frames of first and second fields.

47. A decoding method in accordance with claim 46, further including the additional step of storing fields of pixel data which, relative to said first field of said current frame, include a second field of said current frame and a first field of a past frame of data, wherein said storing step is performed prior to step (b).

48. A decoding method in accordance with claim 47, wherein said blocks of pixel data selected from said second field of said current frame and said first field of said past frame of data are retrieved from storage.

49. A decoding method in accordance with claim 48, wherein step (b) includes using said location signals to derive address signals which are used in said retrieval.

50. A decoding method in accordance with claim 46, wherein step (b) includes using said location signals to derive address signals which are used in said selection.

51. A decoding method in accordance with claim 50, wherein said signals received in step (a) also include best mode signals indicative of a block of data representing the least overall error, and wherein said best mode signals are made available for use in deriving said address signals in step (b) and for controlling said averaging function in step (c).

52. A decoding method in accordance with claim 46, wherein said first fields of video data are even fields and said second fields of video data are odd fields.

53. A decoding method in accordance with claim 46, wherein step (c) includes averaging on a pixel by pixel basis corresponding blocks of data, when two blocks of data are simultaneously selected.

54. A system, for decoding coded fields of video data, wherein frames of video data consist of first and second fields of video data, comprising:

(a) input means for coupling location signals providing location data for best matched blocks of data, pixel error signals representative of pixel value errors in a best mode block relative to a first field of a current frame of data, and second field data signals;

(b) selection means, responsive to said location signals, for selecting one or more blocks of pixel data from a second field of said current frame and a first field of a past frame of data;

(c) block coupling means, responsive to blocks of data selected in step (b), for providing a single best mode data block regardless of the number of blocks of pixel data selected, and including means for averaging simultaneously selected blocks of pixel data;

(d) block adder means, coupled to said input means and block coupling means, for combining said single best mode data block with said pixel error signals to derive a block of first field of a current frame pixel data; and

(e) combiner means, responsive to said first fields of data and to said second fields of data, for providing video signals including frames of first and second fields.

55. A decoding system in accordance with claim 54, further including storage means, coupled to said input means, for storing fields of pixel data which, relative to said first field of said current frame, include a second field of said current frame and a first field of a past frame of data.

56. A decoding system in accordance with claim 55, wherein said blocks of pixel data selected from said second field of said current frame and said first fields of said past frame of data are retrieved from said storage means.

57. A decoding system in accordance with claim 56, wherein said selection means include address generator means, responsive to said storage means, for providing address signals for said retrieval to said storage means.

58. A decoding system in accordance with claim 57, wherein said signals received by said input means also include best mode signals indicative of a block of data representing the least overall error, and wherein said best mode signals are made available for use in deriving said address signals by said address generator means and for controlling said averaging means.

59. A decoding system in accordance with claim 54, wherein said first fields of video data are even fields and said second fields of video data are odd fields.

60. A decoding system in accordance with claim 54,

wherein said block coupling means includes means for averaging on a pixel by pixel basis corresponding blocks of data, when two blocks of data are simultaneously selected by said selection means.

61. A method, for coding multi-mode predictive interpolative coded fields of video, wherein frames of video data consist of first and second fields of video data, comprising the steps of:

(a) providing a first and a second field of a current frame of interlaced pixel data, and fields of past frames of such data;

(b) comparing a block of pixel data from said first field of said current frame with corresponding blocks of data from said second field of said current frame and fields from past frames to derive motion vector signals indicative of best matched blocks of data;

(c) developing pixel error signals representing pixel by pixel errors based on utilization of said best matched blocks in different modes for comparison with said block of pixel data from said first field of said current frame and developing best mode signals indicative of which of said modes represents the least overall error; and

(d) providing said best mode signals, motion vector signals, pixel error signals, and said second field of said current frame of data for transmission for use by a decoder.

62. A system, for coding multi-mode predictive interpolative coded fields of video, wherein frames of video data consist of first and second fields of video data, comprising:

(a) input means for coupling a first and a second field of a current frame of interlaced pixel data, and fields of past frames of such data;

(b) storage means, coupled to said input means, for storing data and for providing data;

(c) block matching means, coupled to said storage means, for comparing a block of pixel data from said first field of said current frame with corresponding blocks of data from said second field of said current frame and fields from past frames to develop motion vector signals indicative of best matched blocks of data, and for coupling said motion vector signals to said storage means;

(d) comparator means, coupled to said storage means, for utilizing blocks of pixel data retrieved from said storage means in response to said motion vector signals for performing a plurality of mode comparisons of a block of pixel data from said first field of said current frame with different ones of said best matched blocks alone or on an averaged basis for deriving a best mode block having the least error and deriving pixel error signals representing pixel by pixel errors in said best mode block; and

(e) output means, coupled to said comparator means, for providing said best mode signals, motion vector signals, pixel error signals, and said second field of said current frame of data for transmission for use by a decoder.

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : RE. 35,093 Page 1 of 3

DATED : November 21, 1995

INVENTOR(S) : Feng M. Wang et al.

It is certified that error appears in the above-indentified patent and that said Letters Patent is hereby corrected as shown below:

Title page, item [56]: OTHER PUBLICATIONS

Puri, A. et al. Video Coding with Motion-Compensated Interpolation for CD-ROM Applications, Image Communication, vol. 2, No. 2 pp. 127-144 Aug. 1990.

Burt, P. J. et al., The Laplacian Pyramid as a Compact Image Code, IEEE Transactions on Communications, vol. COM-31, No. 4 Apr. 1983.

Uz, K. M. et al., A Multiresolution Approach to Motion Estimation and Interpolation with Application to Coding of Digital HDTV, Proceedings, 1990 International Symposium on Circuits and Systems, p. 1298.

Barbero, M. et al., A System for the Transmission of HDTV Signals Based on the Discrete Cosine Transform, Proceedings, 1990 IEEE International Symposium on Circuits and Systems, pp. 1887-1890.

Yashima, Y. et al. HDTV/Standard-TV Compatible Coding Based on DCT, Proceedings, 1990 International Symposium on Circuits and Systems, pp. 1894-1898.

Fleischler, P.E. et al., Coding of Advanced TV for BISDN Using Multiple Subbands, Proceedings, 1990 International Symposium on Circuits and Systems, pp. 1314-1317.

Anastassiou, Dimitris et al., Gray-Scale Image Coding for Freeze-Frame Videoconferencing, IEEE Transactions or Communications, vol. 34, No. 4 Apr. 1986.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : RE. 35,093

DATED : November 21, 1995

INVENTOR(S) : Feng M. Wang et al.

It is certified that error appears in the above-indentified patent and that said Letters Patent is hereby corrected as shown below:

International Organization for Standardization Simulation Model Editorial Group, MPEG Video Simulation Mode Three, Jul. 25, 1990.

Anastassiou, D., Generalized Three-Dimensional Pyramid Coding for HDTV Using Nonlinear Interpolation, Columbia University.

Anastassiou, D., Generalized Pyramid Coding Using Nonlinear Interpolation for HDTV Coding, Proceedings, 1990 Picture Coding Symposium.

Wang, F. and Anastassiou, D., Time Recursive Deinterlacing for HDTV and Pyramid Coding, Image Communication, Vol. 2, No. 3, Oct. 1990.

Netravali, A. N. and Haskell, B.G. "Digital Pictures: Representation and Compression", Plenum Press, 1988.

Col. 4, line 64, "OC(t-1)" should read --Oc(t-1).

Col. 6, line 22, at the beginning of the equation, "(x)" should read --1/4--.

Col. 7, line 28, "half." should read --half).--.

Col. 7, line 61, "CEG, in" should read --CEG. In--.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : RE. 35,093 Page 3 of 3

DATED : November 21, 1995

INVENTOR(S) : Feng M. Wang et al.

It is certified that error appears in the above-indentified patent and that said Letters Patent is hereby corrected as shown below:

Col. 12, line 48, "cooing" should read --coding--.
Col. 16, line 57, "step (e)" should read --step (c)--.
Col. 18, line 19, "denying" should read --deriving--.
Col. 20, line 51, "first fields" should read --first field--.

Signed and Sealed this

Twenty-ninth Day of October 1996

Attest:

BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : RE 35,093
DATED : November 21, 1995
INVENTOR(S) : Wang et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page,
Item [56], before "Preliminary Examiner" insert

-- OTHER PUBLICATIONS

Puri, A. et al., "Video Coding with Motion-Compensated Interpolation for CD-ROM Applications", Image Communications, Vol. 2, No. 2, pp. 127-144, August 1990.

Burt, P.J. et al., "The Laplacian Pyramid as a Compact Image Code", IEEE Transaction on Communications, Vol. COM-31, No. 4, April 1983.

Uz, K.M. et al., "A Multiresolution Approach to Motion Estimation and Interpolation with Application to Coding of Digital HDTV", Proceedings, 1990 International Symposium on Circuits and Systems, p. 1298.

Barbero, M. et al., "A System for the Transmission of HDTV Signals Based on the Discrete Cosine Transform", Proceedings, 1990 IEEE International Symposium on Circuits and Systems, pp. 1887-1890.

Yashima, Y. et al., "HDT/Standard-TV Compatible Coding Based on DCT", Proceedings, 1990 International Symposium on Circuits and Systems, pp. 1894-1898

Fleischer, P.E. et al., "Coding of Advanced TV for BISDN using Multiple Subbands", Proceedings, 1990 International Syposium on Circuits and Systems, pp. 1314-1317.

Anastassiou, D. et al., "Gray-Scale Image Coding for Freeze-Frame Videoconferencing", IEEE Transactions or Communications, Vol. 34, No. 4, April 1986.

International Organization for Standardization Simulation Model Editorial Group, MPEG Video Simulation Model Three, July 25, 1990.

Anastassiou, D., "Generalized Three-Dimensional Pyramid Coding for HDTV Using Nonlinear Interpolation", Columbia University.

Anastassiou, D., "Generalized Pyramid Coding Using Nonlinear Interpolation for HDTV Coding", Proceedings, 1990 Picture Coding Symposium.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : RE 35,093
DATED : November 21, 1995
INVENTOR(S) : Wang et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Wang, F. et al., "Time Recursive Deinterlacing for IDTV and Pyramid Coding", Image Communications, Vol. 2, No. 3, October 1990

Netravali, A.N. and Haskell, B.G. Digital Pictures: Representation and Compression, Plenum Press, 1988. --

Signed and Sealed this

Twelfth Day of February, 2002

Attest:

Attesting Officer

JAMES E. ROGAN
Director of the United States Patent and Trademark Office

Exhibit 13

US005844867A

United States Patent [19]

De Haan et al.

[11] Patent Number: 5,844,867

[45] Date of Patent: *Dec. 1, 1998

[54] **METHODS AND APPARATUS FOR ENCODING AND DECODING AN AUDIO AND/OR VIDEO SIGNAL, AND A RECORD CARRIER USED THEREWITH OR PRODUCED THEREFROM**

[75] Inventors: **Wiebe De Haan; Jan Van Der Meer,** both of Eindhoven, Netherlands

[73] Assignee: **U.S. Philips Corporation,** New York, N.Y.

[*] Notice: The term of this patent shall not extend beyond the expiration date of Pat. No. 5,606,539.

[21] Appl. No.: **707,845**

[22] Filed: **Sep. 9, 1996**

Related U.S. Application Data

[63] Continuation of Ser. No. 299,027, Aug. 31, 1994, Pat. No. 5,606,539, which is a continuation of Ser. No. 86,402, Jun. 30, 1993, abandoned, which is a continuation of Ser. No. 711,186, Jun. 5, 1991, abandoned.

[30] **Foreign Application Priority Data**

Jun. 5, 1990 [GB] United Kingdom 9012538

[51] **Int. Cl.**[6] **G11B 7/00**; H04N 5/76

[52] **U.S. Cl.** **369/59**; 369/48; 369/60; 386/104; 386/109; 386/95

[58] **Field of Search** 369/59, 47, 48, 369/49, 60, 124, 275.3; 370/110.1; 348/432, 384, 390, 461, 419, 387, 474; 386/95, 104, 109, 111, 112, 33

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,215,369	7/1980	Iijima	358/146
4,382,299	5/1983	Dieterich	371/8
4,472,803	9/1984	Iijima	370/110.1
4,512,006	4/1985	Murakami et al.	369/50
4,680,647	7/1987	Moriyama	358/343
4,816,928	3/1989	Sasaki et al.	360/35.1
4,985,784	1/1991	Tsuboi et al.	358/342
5,130,816	7/1992	Yoshio	358/341
5,606,539	2/1997	De Haan et al.	369/59
5,608,697	3/1997	De Haan et al.	369/48

OTHER PUBLICATIONS

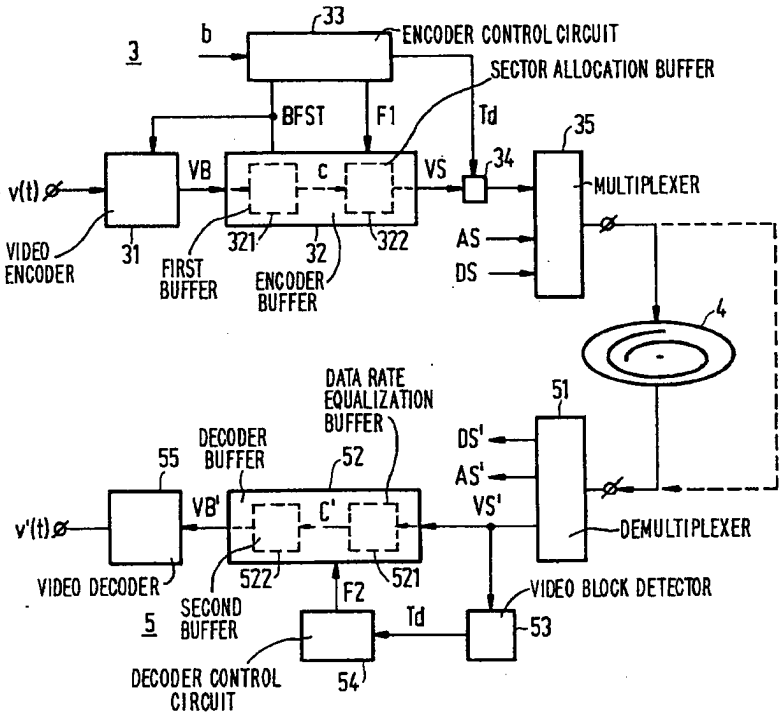
Takahashi et al., Interframe CODEC for NTSC Color Television Signals, Fujitsu Scientific & Technical Journal, vol. 13, No. 4, 1977, pp. 21–52.

Primary Examiner—Thang V. Tran

[57] **ABSTRACT**

Methods and apparatus for encoding and decoding an audio and/or video signal, and a record carrier for use with such apparatus. One or more audio and/or full motion video signals, e.g., a video signal, and possibly computer data) are recorded on an interactive compact disc. The video signal is encoded into code blocks of variable lengths, each corresponding to a picture or picture pair. A decoder delay time parameter is associated with one or more of the code blocks, which parameter represents a length of time (i.e., a delay time) with which the corresponding picture of a code block is to be displayed after that code block has been received by a decoding apparatus.

37 Claims, 4 Drawing Sheets



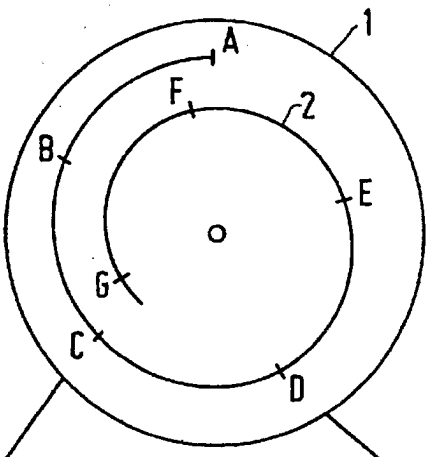


FIG.1A

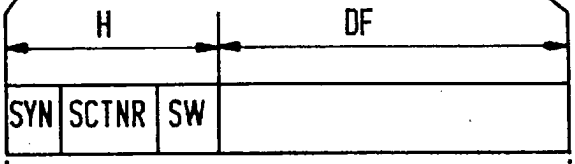


FIG.1B

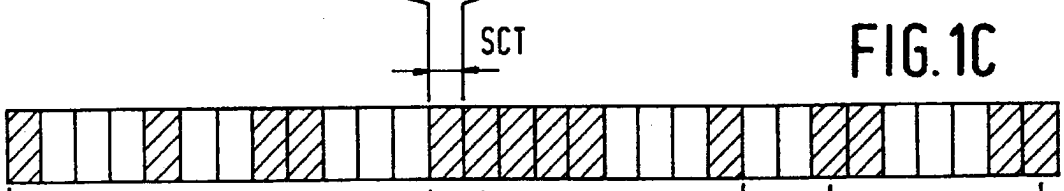


FIG.1C

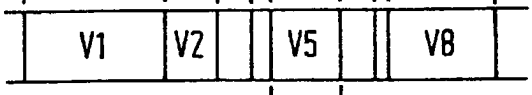


FIG.1D

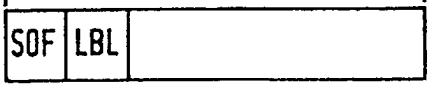


FIG.1E

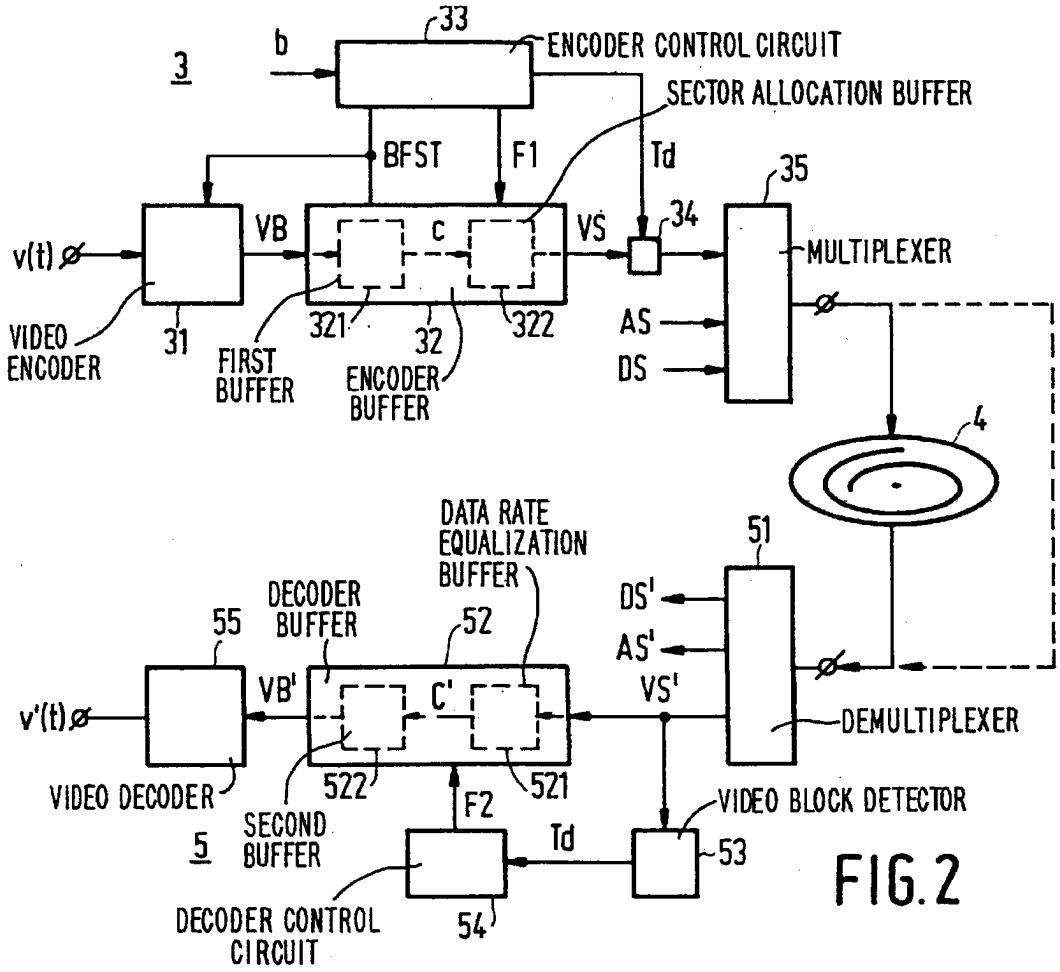

3
b
33
ENCODER CONTROL CIRCUIT
SECTOR ALLOCATION BUFFER
BFST
F1
Td
35
v(t)
VB
C
VS
34
MULTIPLEXER
AS
DS
VIDEO ENCODER
31
FIRST BUFFER
321
32
ENCODER BUFFER
322
4
DATA RATE EQUALIZATION BUFFER
51
DS'
AS'
VS'
DECODER BUFFER
55
52
v'(t)
VB'
C'
DEMULTIPLEXER
VIDEO DECODER
522
521
F2
VIDEO BLOCK DETECTOR
5
SECOND BUFFER
Td
53
DECODER CONTROL CIRCUIT
54

FIG.2

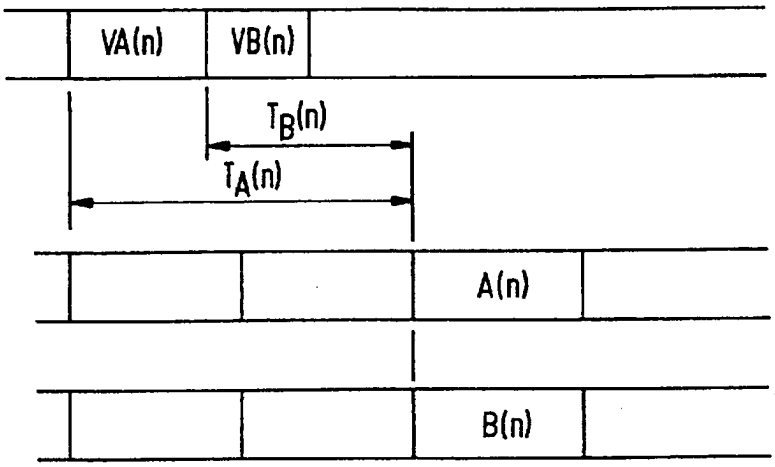

VA(n)
VB(n)
$T_B(n)$
$T_A(n)$
A(n)
B(n)

FIG.5

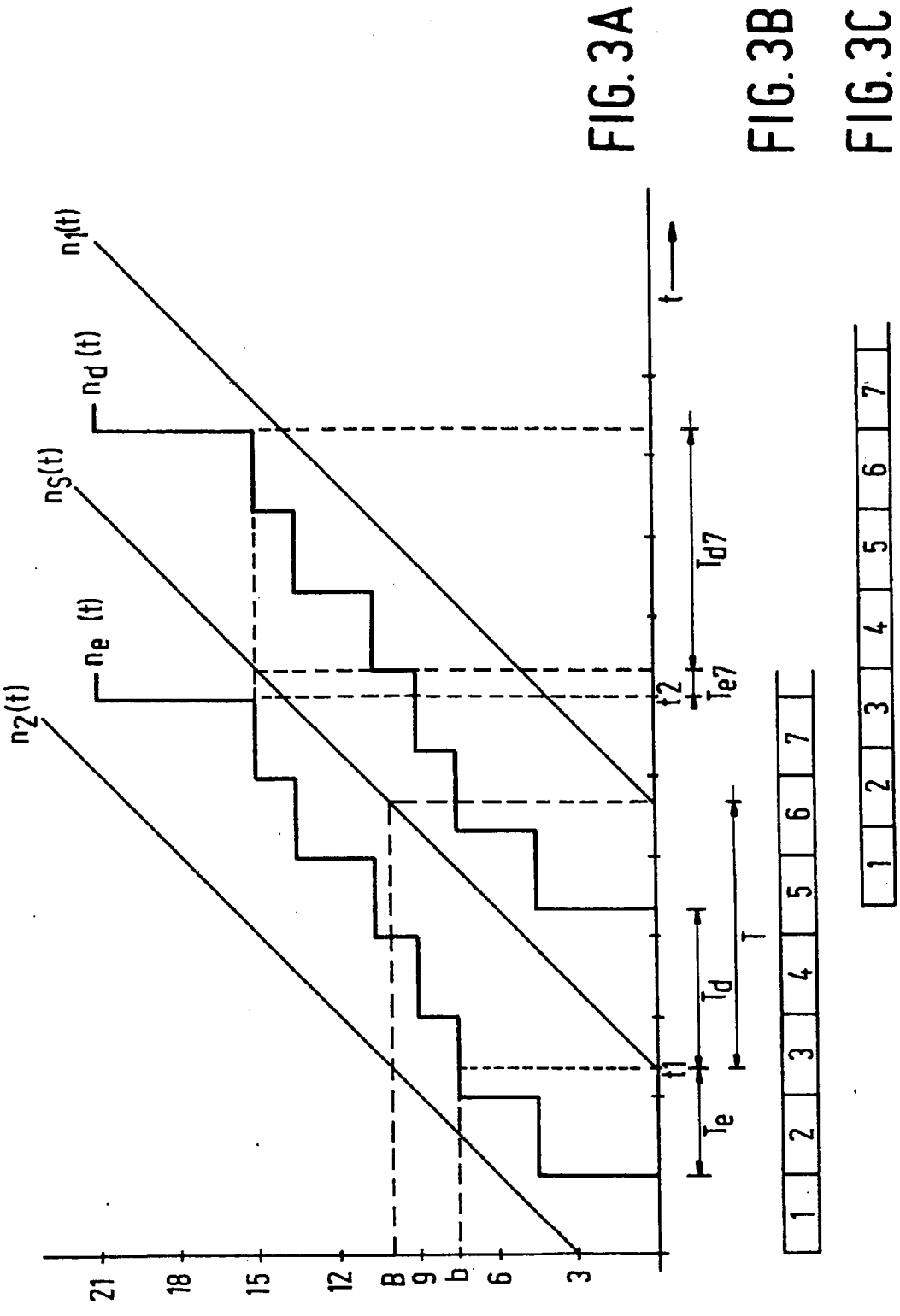


FIG.3A
FIG.3B
FIG.3C
n1(t)
nd (t)
nS(t)
ne (t)
n2(t)
t
t2
t1
Td7
Te7
Td
Te
T
21
18
15
12
B
9
b
6
3
1
2
3
4
5
6
7

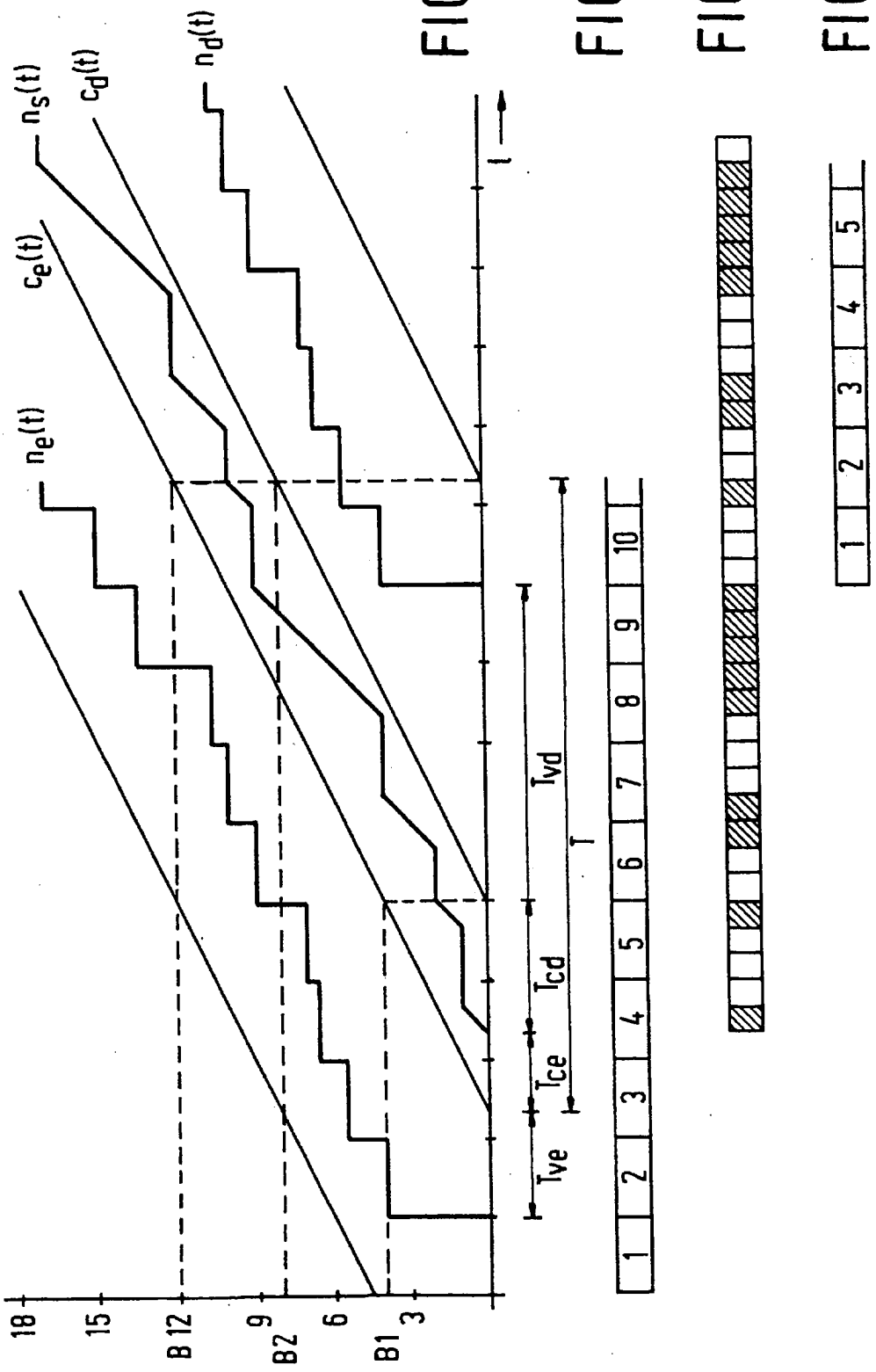


FIG.4A
FIG.4B
FIG.4C
FIG.4D
$n_S(t)$
$c_d(t)$
$n_d(t)$
$c_e(t)$
$n_e(t)$
t
18
15
B 12
9
B2
6
B1
3
T_{ve}
T_{ce}
T_{cd}
T_{vd}
T
1 2 3 4 5 6 7 8 9 10
1 2 3 4 5

METHODS AND APPARATUS FOR ENCODING AND DECODING AN AUDIO AND/OR VIDEO SIGNAL, AND A RECORD CARRIER USED THEREWITH OR PRODUCED THEREFROM

CROSS REFERENCE TO RELATED APPLICATIONS

This is a continuation of application Ser. No. 08/299,027, filed on Aug. 31, 1994, now U.S. Pat. No. 5,606,539, which is a continuation of application Ser. No. 08/086,402, filed Jun. 30, 1993 and now abandoned, which was a continuation of application Ser. No. 07/711,186, filed Jun. 5, 1991 and now abandoned.

BACKGROUND OF THE INVENTION

The invention relates to a method of encoding audio and/or video signals for transmissions via a transmission medium. More particularly, the transmission medium is preferably an optically readable disc. Nevertheless, the transmission medium may also be a magnetic tape or disc, or a direct connection between a transmitter and a receiver. The invention also relates to a transmission medium on which audio and/or video signals are recorded, to an encoding apparatus for encoding and transmitting the audio and/or video signals, and to a decoding apparatus for receiving those signals after unloading and transmission.

The interactive compact disc (CDI) on which data for text and graphic images and digital audio is stored has been developed in the last few years. The presentation possibilities of CDI are considerably enhanced if full motion video pictures are also recorded on it. The known analog recording of a video signal on compact disc video (CDV) is not suitable for this purpose. For this reason, a video signal on CDI is digitized.

A full-motion video scene is considered as a sequence of pictures (of that video scene) of which there are, for example, 25 or 30 per second. Each picture comprises, for example, 256 picture lines and 352 pixels per picture line. The sequence of pictures is converted by means of a suitably chosen encoding method into a series of video blocks, each comprising so much digital information that each picture can be reconstructed without any noticeable loss of quality. Together with the audio signal and further data, the encoded video signal is recorded optically. A CDI may comprise various video scenes.

The most efficient encoding methods convert successive signal portions into successive code blocks of variable lengths. In the case of a video signal, these signal portions are formed, for example, by the pictures or picture pairs of which the signal is composed. Some pictures may be subjected to intraframe coding and are then converted into code blocks from which the picture can be reconstructed completely. Other pictures may be subjected to interframe coding, which means that the pictures can only be reconstructed with the aid of previous pictures. The code blocks a video signal will hereinafter be referred to as video blocks. Due to their variable length, the successive video blocks are read at irregular instants when a disc in which they are stored is being played. Moreover, the video blocks on the disc may alternate with (or may even by interrupted by) other data signals, for example, a lip-synchronous digital audio signal corresponding to the video scene.

The pictures corresponding to the video blocks should be displayed at a constant frequency of, for example, 25 frames per second. However, the instant when a video block of the

disc is being read hardly ever corresponds exactly to the instant when the corresponding picture from the video scene is to be displayed. In a player, the video blocks are, therefore, applied to a memory buffer at a frequency which is entirely determined by the way in which they are "packed" on the disc. Subsequently, the video block are read from the buffer at the picture frequency required for display. On an average, the number of video blocks applied per second from the disc to the buffer equals the number of pictures displayed per second. The video block corresponding to the next picture to be displayed will always have to be stored completely in the buffer. Moreover, the buffer will already comprise a subsequent video block, a portion thereof or even a number of subsequent video blocks. As soon as a picture has been decoded, the corresponding video block may be removed from the buffer. The buffer space then released is written by one or more subsequent video blocks or a portion thereof. The number of video blocks stored in the buffer for later display is thus variable, and is greatly dependent on the encoding efficiency and the presence of signals other than the relevant video signal on the disc.

It would seem that the display of a video scene can start as soon as the first video block has been received completely and is stored in the buffer. However, this is not the case. It is possible that a subsequent video block is too large to be scanned (and stored in the buffer) within the required time (1/25 sec) to (decode and) display the picture corresponding to the first video blank. As a result, the corresponding picture of the subsequent video block cannot be displayed in time. The absence of a complete video block in the buffer at the instant when the corresponding picture has to be decoded and displayed is sometimes referred to as underflow of the buffer.

Underflow of the buffer also occurs if a large quantity of other (non-video) data has been packed together with the video blocks of a scene causing the buffer to be temporarily not filled with video blocks. Because of that other data the buffer empties, and at a given instant the video block for the corresponding next picture to be displayed is not yet present. The display of the video scene then stalls, and the pictures are not smooth moving.

If the display of a picture of a video scene starts too late after the corresponding video block has been received, it is probable that the buffer will fill so that the display of the video scene also stalls. This is referred to as overflow of the buffer.

The same problems occur with audio signals which may also be recorded on the disc in a non-contiguous manner.

SUMMARY OF THE INVENTION

It is an object of the invention to provide a method of encoding audio and/or video signals (for transmission) in which the occurrence of overflow and underflow of a decoder buffer is prevented so that the display of pictures can proceed in an undisturbed manner.

According to the invention, a parameter is associated with at least one selected code block, which parameter indicates the quantity of delay with which that code block must be decoded after it has been received. If the corresponding picture is decoded with this delay, it can be displayed without the risk of overflow or underflow of the buffer. This ensures an undisturbed display. The transmission of the parameter, sometimes referred to as a decoder delay parameter (or decoder delay for short), also enables synchronous display of two signals, for example, a video signal with a time-division multiplexed associated audio signal, or two video signals jointly representing a threedimensional video scene.

In principle, it is sufficient to associate the parameter with one video block. This will preferably be the first block of the video scene. All further pictures can then be read at a constant picture frequency without a further risk of overflow or underflow of the buffer.

In a further embodiment of the method, the decoder delay parameter is regularly associated with video blocks. The constant picture frequency can then be obtained in a favorable manner. Moreover, this provides the possibility of a so-called "random-access" display. This means the display of a fragment of a video scene from the video block with which the decoder delay is associated.

The decoder delay parameter may assume various formats, but it preferably indicates the state of a counter which is regularly loaded with a reference value which is also transmitted and which counter further receives a predetermined clock signal.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A–E show diagrammatically an optically readable disc with an audio and/or video signal recorded thereon and the format of that disc.

FIG. 2 shows the general structure of a transmission circuit suitable for performing the method according to the invention.

FIGS. 3A–C show some time diagrams which help explain the circuit of FIG. 2.

FIG. 4 shows some further time diagrams to explain the circuit of FIG. 2.

FIG. 5 shows some time diagrams to explain the transmission of two simultaneously transmitted signals.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

FIG. 1A shows diagrammatically an optically readable disc 1 with an information track 2 recorded thereon. A so-called sector, of which there may be about 300,000, is present between every two successive points A, B, C, D, etc. The structure of such a sector is shown diagrammatically in FIG. 1B. It is divided into a sector header H or 24 bytes and a data field DF of 2324 bytes. The sector head H comprises a synchronization word SYN of 12 bytes, a sector number SCTNR of 4 bytes and a service word SW of 8 bytes. The synchronization word SYN marks the start of a sector. The sector number SCTNR indicates the ordinal number of the sector on the disc 1. The service word SW indicates whether the data field DF of the sector comprises video data, audio data or computer data. In conformity with that data, a sector is sometimes referred to as a video sector, an audio sector or a data sector.

The conventional rate of revolution of the disc 1 is such that 75 sectors per second are scanned. This corresponds to a bit rate, hereinafter referred to as channel bit rate, of approximately 1.4 Mbit/sec. If a disc comprises video sectors only, the video bit rate is equal to the channel bit rate. If a disc also comprises audio and data sectors, the video bit rate decreases accordingly.

FIG. 1C shows a part of the track 2 in which the sectors are denoted by SCT. More particularly the video sectors therein are shaded. The video sectors alternate with other sectors.

There are many encoding methods for reducing the number of bits per picture without deteriorating picture quality. The most efficient encoding methods convert successive pictures of a video scene into video blocks of distinct number of bits. In FIG. 1D, this is shown in the form of video blocks V1, V2, etc., each having a distinct length. For example, video block V1 has a length of 4 sectors on the disc 1, video block V2 has a length of 1½ sector, etc.

FIG. 1E shows the data format of a video block. The start of a video block is marked by the presence of a unique start-of-frame word SOF. The video block also comprises a label LBL in which specific control information is stored for the corresponding video block.

FIG. 2 shows the general structure of a circuit for transmitting audio and video signals. The circuit comprises an encoding apparatus 3, a compact disc 4 and a decoding apparatus 5.

The encoding apparatus 3 of FIG. 2 comprises a video encoder 31 to which a video signal v(t) is applied. The video encoder 31 encodes successive pictures of the video signal, of which there are 25 per second, into video blocks VB of variable lengths. These pictures are applied video block by video block to an encoder buffer 32. To prevent overflow and underflow of the encoder buffer 32, a buffer status signal BFST is fed back to the video encoder 31 so that the video encoder 31 can adapt the encoding efficiency to the contents of the encoder buffer 32. If the encoder buffer 32 tends to get filled and there is a risk of overflow, the video signal is temporarily quantized in a coarser manner. If the encoder buffer 32 tends to get empty, the video signal is quantized more accurately, or pseudo-video data is possibly temporarily applied to the encoder buffer 32. The buffer status signal BFST is also applied to an encoder control circuit 33. The encoder control circuit 33 of FIG. 2 is adapted to generate, at a predetermined degree of occupation of the encoder buffer 32, a clock signal F1 with which the encoder buffer 32 is read. The encoder control circuit 33 also determines the value of a parameter T_d for each video block in a manner to be described hereinafter. This parameter (T_d) is associated with a video block by means of an inserter 34 and transmitted in the label LBL of that block (see FIG. 1E).

As is shown in FIG. 2, the encoder buffer 32 may be considered to be divided into a first buffer 321 to which the video blocks VB are applied and which is read at a constant video bit rate C, and a sector allocation buffer 322 which converts this constant bit stream into video sectors VS. The video sectors VS are applied from the encoder buffer 32 to a first input of a multiplexer 35 which receives audio sectors AS at a second input and data sectors DS at a third input. The resultant bit stream is recorded on the compact disc 4.

When the compact disc 4 is played at a later stage, the sectors are scanned and applied to a demultiplexer 51 in which the video sectors VS' are separated from audio sectors AS' and data sectors DS' by reference to each sectors service word SW (see FIG. 1B). The video sectors VS' are applied to a decoder buffer 52 and a video block detector 53. The video block detector 53 detects the occurrence of a start-of-frame code SOF (see FIG. 1E) and reads from the subsequent label LBL the parameter T_d transmitted therein. The parameter T_d is applied to a decoder control circuit 54 which is adapted to read the decoder buffer 52 with a clock signal F2. In a manner to be described hereinafter, the parameter T_d determines the instant when each video block is read from the decoder buffer 52.

As is shown in the FIG. 2, the decoder buffer 52 may be considered to be divided into a data rate equalization buffer 521 to which the video sectors VS' are applied and which is read at a constant video bit rate C', and a second buffer 522 which converts this constant bit stream into successive video blocks VB'. Finally, each video block is applied to a video

decoder **55** for conversion into a picture. The successive pictures which are obtained are applied as a video signal v'(t) to a display device (now shown).

In practice the actual instant when a disc is being played does not play any role at all. Therefore, it will be assumed hereinafter that the output of the encoding apparatus **3** is directly connected to the input of the decoding apparatus **5**. This is indicated by means of a broken line in FIG. **2**.

It will be assumed for the time being that only video signals are transmitted. This means that the encoder buffer **32** can apply an uninterrupted bit stream to the disc **4** at the full channel bit rate of 1.4 Mbit/sec (75 sectors per second). This means that the sector allocation buffer **322** and the multiplexer **35**, on the one hand, and the demultiplexer **51** and the data rate equalization buffer **521**, on the other hand, of FIG. **2** do not play a role in the following discussion.

The operation of the circuit shown in FIG. **2** will be explained with reference to some time diagrams which are shown in FIGS. 3A–C. More particularly, FIG. 3B shows a number of successive pictures enumerated **1, 2, 3**, etc. These pictures occur at a picture frequency of 25 frames per second and are applied to the video encoder **31** of FIG. **2**. As soon as each picture has been encoded, the corresponding video block is written into the encoder buffer **32** of FIG. **2**. For the sake of simplicity, it is assumed that this is effected timelessly. The quantity of video data cumulatively applied to the encoder buffer **32** and expressed in disc sectors increases step-wise for each video block. This is denoted by means of the curve $n_e(t)$ in FIG. 3A.

Reading of the encoder buffer **32** of FIG. **2** and applying data to the output of the encoding apparatus **3** of FIG. **2** starts from instant **t1**. This instant **t1** is determined, for example, by reaching a predetermined degree b of occupation of the encoder buffer **32** and may be different for each video scene. Reading is effected at a constant rate of 75 sectors per second, i.e., 1.4 Mbit/sec. The quantity of video data cumulatively withdrawn from the encoder buffer **32** increases lineraly. This is denoted by means of the curve $n_s(t)$ in FIG. 3A. The curves $n_e(t)$ and $n_s(t)$ must not intersect each other because this would mean that a video block is read from the encoder buffer **32** before it is written into it (underflow of the encoder buffer **32**). As already previously stated, underflow of the encoder buffer **32** is prevented by adapting the quantization of the video scene to the contents of the encoder buffer **32**.

Based on the assumption that the output of the encoding apparatus **3** of FIG. **2** is directly connected to the input of the decoding apparatus **5** of FIG. **2**, the curve $n_s(t)$ shown in FIG. 3A also indicates the cumulative quantity of video data applied to the decoder buffer **52** of FIG. **2**. The decoder buffer **52** must be read in such a manner that the curve $n_s(t)$ is not exceeded, because underflow of the decoder buffer **52** could then occur. Overflow of the decoder buffer **52** should not occur either. In FIG. 3A line $n_1(t)$ at a distance B (the buffer size) from the line $n_s(t)$ indicates the threshold of overflow of the encoder buffer **52**. The **52** line $n_1(t)$ should not be exceeded by the curve $n_s(t)$.

The decoder buffer **52** of FIG. **2** is read video block by video block. For the sake of simplicity, it is assumed that a video block is read timelessly. The quantity of video data cumulatively withdrawn from the decoder buffer **52** and expressed in disc sectors increases step-wise for each video block. This is denoted by means of the curve $n_d(t)$ in FIG. 3A. As soon as a video block has been read and decoded, the corresponding picture is displayed in 1/25 sec. FIG. 3C shows the display of the decoded pictures **1, 2, 3**, etc.

The curve $n_d(t)$ is a replica of the curve $n_e(t)$ shifted over a time interval T_e+T_d. Here T_e, also referred to as an encoder delay, is the delay time between the instant when the first video block of the video scene is written into the encoder buffer **32** of FIG. **2** and the instant **t1** when the transmission of this video block begins. In a corresponding manner T_d, also referred to as a decoder delay, is the delay time between the instant when the reception of the first video block in the decoder buffer **52** of FIG. **2** begins and the instant when this video block is, read from the decoder buffer **52**. The time interval T_e+T_d represents the delay time occurring between writing a video block into the encoder buffer **32** and reading the same video block from the decoder buffer **52**. This delay time is constant. As previously noted, **t1**, and consequently T_e, may be different for each video scene. In addition (and in conformity therewith), the decoder delay T_d may be different for each video scene as well.

The instant when the decoding apparatus of FIG. **2** starts reading the decoder buffer **52** of FIG. **2** is of great importance. In fact, if the decoder **5** should start reading too early, there may be underflow of the decoder buffer **52** because the curve $n_d(t)$ will intersect the boundary line $n_s(t)$. If the decoder **5** starts reading too late, there may be overflow of the decoder buffer **52** because the curve $n_d(t)$ will intersect the boundary line $n_1(t)$. Both underflow and overflow may become manifest in the video scene at a possibly later stage.

Overflow and underflow of the decoder buffer **52** of FIG. **2** do not occur if the curve $n_d(t)$ is always as far remote from the boundaries lines $n_s(t)$ and $n_1(t)$as the curve $n_e(t)$ is from boundaries lines $n_2(t)$ and $n_s(t)$. Line $n_2(t)$ is a line at a distance B (the decoder buffer size) from the line $n_e(t)$. This is realized by choosing a suitable value for the decoder delay T_d, as well as by the previously mentioned mechanism of adaptive quantization in the encoding apparatus **3** of FIG. **2**, which ensures that the curve $n_e(t)$ remains completely between the two boundaries lines $n_2(t)$ and $n_s(t)$.

A suitable value for decoder delay T_d can be obtained by considering the fact that the previously mentioned delay time T_e+T_d is equal to a time interval T shown in FIG. 3A. The time interval T corresponds to the time required to fully read a completely filled encoder buffer or to completely fill a still empty decoder buffer, and is entirely determined by the buffer size B and the video bit rate at which that buffer is read or written. Accordingly, the value of T_d can be derived from the computation of the different $T-T_e$. Here both T_e and T are known to the encoding apparatus.

The encoding apparatus **3** of FIG. **2** associates the decoder delay T_d as a parameter with the first video block of the scene so as to enable the decoding apparatus **5** of FIG. **2** to determine the instant when reading of the decoder buffer **52** of FIG. **2** should start. After the decoding apparatus **5** has read the video block with the delay T_d from the encoder buffer **52**, the reading process can be continued at the picture frequency in an autonomic manner without the risk of underflow or overflow of the decoder buffer **52**. The picture frequency of 25 Hz can be obtained by dividing the channel bit rate (75 sectors/sec*2324 bytes/sector*8 bits/byte) by 55776. The coupling of the picture frequency to the channel bit rate which is necessary for this purpose is, however, superfluous if the decoder delay parameter has regularly been associated with video blocks. In such a case, the decoder delay will generally be different for each video block.

If the difference between the actual instant when a video block is read and the instant determined by the corresponding decoder delay parameter occurs at a given picture

frequency, the picture frequency or the rate of revolution of the disc can be corrected in response to this difference. FIG. 3A shows by way of example a decoder delay T_{d7} for picture 7. At the instant denoted by t2 the video block corresponding to picture 7 is written into the encoder buffer 32 of FIG. 2. After encoder delay T_{e7}, transmission of the video block corresponding to picture 7 from the encoder buffer 32 to the encoder buffer 52 of FIG. 2 starts, and after a subsequent decoder delay T_{d7}, that video block must be decoded. The encoding apparatus 3 of FIG. 2 associates the decoder delay $T_{d7}=T-T_{e7}$ for picture 7 with video block 7 and transmits it in the label LBL of this block (see FIG. 1E).

The regular transmission of the decoder delay also provides the possibility of a so-called "random-access" playback mode. This means playing a fragment of the video scene from a picture other than the first picture. For example, the decoder delay T_{d7} shown in FIG. 3A can be used to play the fragment of the video scene from picture 7. Picture 7 is preferably an intraframe-encoded picture and can therefore be reconstructed without the aid of previous pictures. In principle, it is possible to compute the decoder delay T_{d7} for picture 7 from the previous signal. However, such computations are complicated and also require the availability of previous information. In the case of random-access display, the previous signal is, however, not available.

The situation described above will be more complicated if not all disc sectors are allocated to video data. If the disc also comprises sectors with audio and computer data, they will alternate with video sectors on the disc. The average video bit rate for a video scene will now be lower than 75 sectors per second. The average video bit rate will hereinafter be expressed in a number S indicating which part of the channel bit rate is suitable for video transmission. For example, S=½ means that on an average 1 out of 2 sectors is a video sector. This corresponds to a video bit rate of ½*75=37.5 sectors per second, i.e., 0.7 Mbit/sec.

For the purpose of illustration, FIG. 4 shows some time diagrams of the encoding and decoding process if S=½. FIG. 4B shows diagrammatically the successive pictures 1, 2, etc. of a video scene applied to the encoding apparatus 3 of FIG. 2. The curve $n_3(t)$ in FIG. 4A indicates the quantity of video data applied for each picture to the encoder buffer 32 of FIG. 2 and expressed in the number of disc sectors. In comparison with the curve $n_e(t)$ in FIG. 3A, the encoding is now such that on average each picture is encoded in 1.5 sectors instead of in 3 sectors. The contents of the encoder buffer 32 are applied to selected sectors of the disc. This is effected in accordance with a given pattern, an example of which is shown in FIG. 4C. In the pattern shown in FIG. 4C, the shaded sectors represent video sectors and, the other sectors are audio sectors or data sectors. FIG. 4C also shows the signal controlling the multiplexer 35 of FIG. 2. The average bit rate is reached in this example by writing video information on 8 out of each 16 sectors on the disc. The quantity of video data cumulatively applied to the disc is indicated in FIG. 4A by means of the curve $n_s(t)$.

When the disc is being played, the reverse operations take place. The curve $n_s(t)$ now represents the number of video sectors cumulatively read from the disc. These sectors are applied to the decoder buffer 52 of FIG. 2, from which they are subsequently read video block by video block in accordance with the curve $n_d(t)$.

In FIG. 4A, $n_e(t)-n_s(t)$ indicates the actual contents of the encoder buffer 32 of FIG. 2. To prevent underflow of the encoder buffer 32, the curves $n_e(t)$ and $n_s(t)$ should not intersect each other. This condition is certainly met if, as already shown in FIG. 2, the encoder buffer 32 is considered to be divided into a first buffer 321 to which the video blocks are applied and which is read at a constant video bit rate, and a sector allocation buffer 322 which converts this constant bit stream into the sector-sequential supply of sectors to the disc. That constant bit stream is denoted by the straigth line $c_e(t)$ in FIG. 4A. The slope of the line $C_e(t)$ is the average bit rate, 0.7 Mbit/sec in this example. As long as the two curves $n_e(t)$ and $n_s(t)$ do not intersect the line $c_e(t)$, there is no encoder buffer underflow.

In a corresponding manner, $n_s(t)-n_d(t)$ represents the actual contents of the decoder buffer 52 of FIG. 2. To prevent underflow of the decoder buffer 52, the curve $n_e(t)$ should not intersect the curve $n_s(t)$. This condition is certainly met if, as already shown in FIG. 2, the decoder buffer 52 is considered to be divided into a data rate equalization buffer 521 having a size of B1 to which the video sectors of the disc are applied and which is read at the constant bit rate, and a second buffer 522 of the size B2 which converts this constant bit stream into video blocks. That constant bit stream is denoted by the straight line $c_d(t)$ in FIG. 4A. The slope of the line $c_d(t)$ corresponds to the average video bit rate of 0.7 Mbit/sec. As long as the two curves $n_s(t)$ and $n_d(t)$ do not intersect the line $c_d(t)$,there is no decoder buffer underflow.

The previously mentioned decoder delay parameter (T_d) which indicates when the decoding apparatus 5 of FIG. 2 can read a video block from the decoder buffer 52 of FIG. 2 after the first bit of the video scene has been scanned (i.e. read from the disc), is now equal to $T_{cd}+T_{vd}$ shown in FIG. 4A. Its value is completely determined by the encoding apparatus 3 of FIG. 2 and transmitted in the label LBL (see FIG. 1E) of a corresponding video block.

The decoder delay parameter is determined as follows. The value of $T_{cd}+T_{vd}$ follows from the consideration that $T_{ve}+T_{ce}+T_{cd}+T_{vd}$ corresponds to the delay of the video signal (from being read into the encoder buffer 32 of FIG. 2 to being read out of decoder buffer 52 of FIG. 2) if the output of the encoding apparatus 3 of FIG. 2 is directly coupled to the input of the decoding apparatus 5 of FIG. 2. This delay is equal to the interval T shown in FIG. 4A and is dependent on the average video bit rate which is S*75 sectors per second and the size B (=B1+B2) of the decoder buffer 52 of FIG. 2. More particularly, it can be derived from FIG. 4A that

$$T=\frac{B}{S*75}$$

and

$$T_{cd}+T_{vd}=T-(T_{ve}+T_{ce}).$$

Here, S is fixed when writing the disc. As for the decoder buffer size B, it holds that it may be a predetermined fixed value which is fixed in the encoding apparatus 3 of FIG. 2 as well as in the decoding apparatus 5 of FIG. 2. The encoding apparatus 3 may also be adapted to transmit the buffer size B to be reserved in the decoding apparatus 5 as a further parameter. It is notably sensible to render the decoder buffer size B dependent on S. The (encoder) delay ($T_{ve}+T_{ce}$), being the time between the encoding of a video picture and its transmission, is determined by the encoding apparatus 3 itself. As already previously stated, the insant when the first video block is transmitted may be determined by reaching a predetermined degree of occupation of the encoder buffer 32.

The form of the transmitted decoder delay parameter may assume several formats. For example, it is possible to

transmit a value indicating at which degree of occupation of the decoder buffer **52** of FIG. **2** the decoder **5** of FIG. **2** should start reading. This degree of occupation may be expressed in an absolute value (number of bits) or in a relative value (fraction of the buffer size B). The decoder delay parameter may also indicate the time delay in suitably chosen units with respect to the instant when EL video block is written into the decoder buffer **52**. Suitable units are, for example, (m)sec or the number of clock periods of a predetermined clock signal. It has been found useful to have the decoder delay parameter indicate the state of a counter at which the decoding of a video block should start The counter is then regularly loaded with a reference value which is also transmitted. The counter is further clocked by a predetermined clock signal. The transmitted reference value may form part of the service word SW (see FIG. 1B). A suitable frequency of the clock signal is 90 kHz. This value is an integral multiple of the picture frequencies 24 Hz, 25 Hz, 30 Hz and 29.97 Hz which are suitable for display.

Finally, it is to be noted that in the foregoing the decoder delay parameter is only described for one signal, in this case a video signal. However, the decoder delay parameter also enables the synchronous display of a plurality of signals. These may be, for example, a video signal and an associated lipsynchronous audio signal. However, they may also be two vide signals multiplexed on the compact disc, which signals may not only be displayed separately but, also if desired, simultaneously. This is shown diagrammatically in FIG. **5** for two video signals A and B.

FIG. **5** shows a video block VA(n) and VB(n) of the two signals, in which n is the ordinal number of the corresponding picture to be displayed. As is apparent from FIG. **5**, the decoder delay parameters $T_A(n)$ and $T_B(n)$ transmitted in the video block have such a value that the corresponding pictures A(n) and B(n) are displayed simultaneously.

We claim:

1. A method for encoding an audio and/or video signal, the method comprising:

encoding successive portions of the audio and/or video signal into corresponding successive code blocks;

determining a delay time parameter for at least one code block of the code blocks, which delay time parameter indicates how long after the code block has been received by a decoding device it is to be decoded; and

inserting the delay time parameter into the code block.

2. The method as claimed in claim **1**, wherein the delay time parameter is inserted into a predetermined position of the code block.

3. The method as claimed in claim **2**, wherein the code block is a first code block of the code blocks.

4. The method as claimed in claim **2**, wherein the delay time parameter indicates how long before decoding the code block the code block is to be stored within a decoder buffer, which receives the code blocks before decoding.

5. The method as claimed in claim **4**, wherein the delay time parameter indicates how long each code block of the code blocks is to be stored in the decoder buffer before being decoded.

6. The method as claimed in claim **4**, wherein the delay time parameter is the degree of occupation the decoder buffer must be at before the code block, after being stored therein, is to be decoded.

7. The method as claimed in claim **2**, wherein the delay time parameter is a time indication.

8. The method as claimed in claim **2**, wherein the delay time parameter is a number of clock period of a predetermined clock signal.

9. The method as claimed in claim **2**, wherein the delay time parameter is the state of a counter.

10. The method as claimed in claim **2**, further comprising recording the code blocks after insertion of the delay time parameter on an optically readable or magnetic record carrier.

11. A record carrier produced by the method claimed in claim **10**.

12. The method as claimed in claim **2**, further comprising transmitting the code blocks after insertion of the delay time parameter to a decoding device.

13. The method as claimed in claim **1**, wherein a respective delay time parameter is determined for a plurality of the code blocks, and each respective delay time parameter is inserted into a same predetermined position of the code block for which that respective delay time parameter is determined.

14. The method as claimed in claim **13**, wherein the code blocks have variable lengths.

15. An apparatus for encoding an audio and/or video signal, the apparatus comprising:

an encoder which encodes successive portions of the audio and/or video signal into corresponding successive code blocks;

a paramater determining unit which determines a delay time parameter for at least one code block of the code blocks, which delay time parameter indicates how long after the code block has been received by a decoding device it is to be decoded; and

an inserting unit which inserts the delay time parameter into the code block.

16. The apparatus as claimed in claim **15**, wherein the inserting unit inserts the delay time parameter into a predetermined position of the code block.

17. The apparatus as claimed in claim **16**, further comprising means for recording the encoded signal after insertion of the delay time parameter on an optically readable or magnetic record carrier.

18. A transmitting device, comprising the apparatus as claimed in claim **16**, for transmitting the code blocks after insertion of the delay time parameter.

19. A record carrier, including:

successive code blocks representing successive portions of an audio and/or video signal; and

a delay time parameter for at least one code block of the code blocks indicating how long after that code block is obtained by a decoder it is to be decoded.

20. The record carrier as claimed in claim **19**, wherein the delay time paramater is located at a predetermined position within the code block.

21. The record carrier as claimed in claim **20**, wherein the code block is a first code block of the code blocks.

22. The record carrier as claimed in claim **20**, wherein the delay time parameter indicates how long before decoding the code block the code block is to be stored within a decoder buffer, which receives the code blocks before decoding.

23. The record carrier as claimed in claim **22**, wherein the delay time parameter indicates how long each code block of the code blocks is to be stored in the decoder buffer before being decoded.

24. The record carrier as claimed in claim **22**, wherein the delay time parameter is the degree of occupation the decoder buffer must be at before the code block, after being stored therein, is to be decoded.

25. The record carrier as claimed in claim **20**, wherein the delay time parameter is a time indication.

26. The record carrier as claimed in claim 20, wherein the delay time parameter is a number of clock period of a predetermined clock signal.

27. The record carrier as claimed in claim 20, wherein the delay time parameter is the state of a counter.

28. The record carrier as claimed in claim 20, further comprising a plurality of delay time parameters which are each associated with and included in a different one of the code blocks at a same respective predetermined position therein.

29. A method for decoding an audio and/or video signal which has been encoded into corresponding successive code blocks, the method comprising:

obtaining the code blocks and a delay time parameter for at least one code block of the code blocks, which delay time parameter indicates how long after the code block has been obtained it is to be decoded; and

decoding the code blocks in a manner whereby the decoding of the code block is delayed with respect to when it is obtained for a period of time indicated by the delay time paramater.

30. The method as claimed in claim 29, wherein the delay time parameter is obtained from a predetermined position of the code block.

31. The method as claimed in claim 30, wherein the code blocks and the delay time parameter are obtained from a record carrier.

32. The method as claimed in claim 30, wherein the code blocks and the delay time parameter are obtained from a transmission medium.

33. The method as claimed in claim 30, wherein the code blocks are decoded in a manner whereby the decoding of each code block is delayed with respect to when it is obtained for the period of time indicated by the delay time parameter.

34. The method as claimed in claim 29, wherein a respective delay time parameter is obtained for a plurality of the code blocks from a same predetermined position in the code block to which that respective delay time parameter relates; and the code blocks are decoded in a manner whereby the decoding of each code block of the plurality of code blocks is delayed with respect to when it is obtained for a period of time indicated by the delay time paramater obtained from that code block.

35. An apparatus for decoding an audio and/or video signal which has been encoded into corresponding successive code blocks, the apparatus comprising:

receiving means for receiving the code blocks;

parameter obtaining means for obtaining a delay time parameter for at least one code block of the code blocks, which delay time parameter indicates how long after the code block has been received it is to be decoded; and

means for decoding the code blocks in a manner whereby the decoding of the code block is delayed with respect to when it is obtained for a period of time indicated by the delay time paramater.

36. The apparatus as claimed in claim 35, wherein the parameter obtaining means obtains the delay time parameter from a predetermined position of the code block.

37. The apparatus as claimed in claim 36, wherein the decoding means comprises

a decoder buffer for receiving the code blocks prior to decoding; and

a decoder, coupled to the decoder buffer, for receiving the code blocks from the decoder buffer and decoding them;

wherein the decoder buffer stores the block code for a period of time indicated by the delay time paramater.

* * * * *

Exhibit 14

United States Patent [19]

De Haan et al.

[11] **Patent Number: 5,606,539**

[45] **Date of Patent: Feb. 25, 1997**

[54] **METHOD AND APPARATUS FOR ENCODING AND DECODING AN AUDIO AND/OR VIDEO SIGNAL, AND A RECORD CARRIER FOR USE WITH SUCH APPARATUS**

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[73] Assignee: **U.S. Philips Corporation,** New York, N.Y.

[21] Appl. No.: **299,027**

[22] Filed: **Aug. 31, 1994**

Related U.S. Application Data

[63] Continuation of Ser. No. 86,402, Jun. 30, 1993, abandoned, which is a continuation of Ser. No. 711,186, Jun. 5, 1991, abandoned.

[30] **Foreign Application Priority Data**

Jun. 5, 1990 [GB] United Kingdom 9012538

[51] **Int. Cl.**^{6} **H04N 5/76**

[52] **U.S. Cl.** **369/59**; 369/48; 348/461; 348/419; 386/104

[58] **Field of Search** 369/48, 99, 54, 369/59, 60; 360/19.1, 40, 48, 35.1, 8, 15; 358/342, 343, 335, 133, 146, 135, 136; 370/110.1; 348/384, 390, 461, 419, 387, 474

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,215,369	7/1980	Iijima	358/146
4,382,299	5/1983	Dieterich	369/48 X
4,472,803	9/1984	Iijima	370/110.1
4,512,006	4/1985	Murakami et al.	369/59 X
4,680,647	7/1987	Moriyama	360/19.1 X
4,816,928	3/1989	Sasaki et al.	360/35.1
4,985,784	1/1991	Tsuboi et al.	369/59 X
5,130,816	7/1992	Yoshio	369/49 X

OTHER PUBLICATIONS

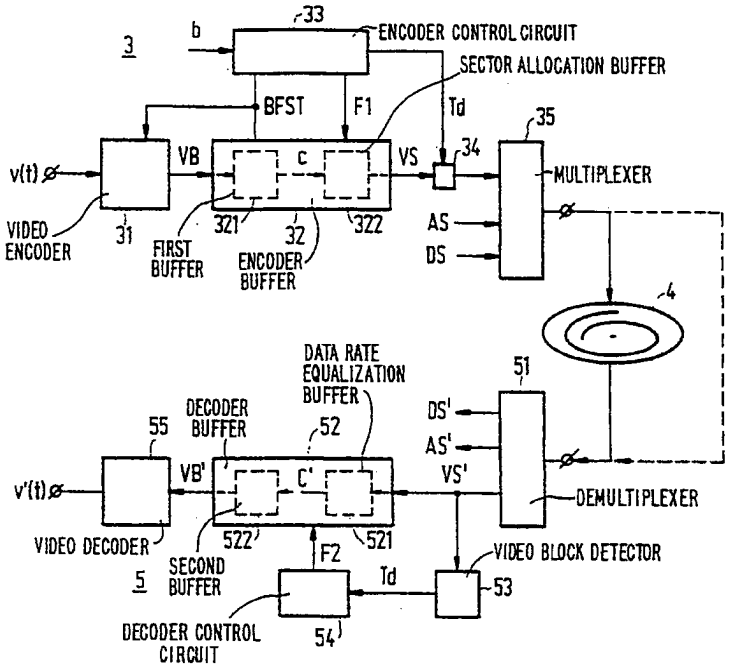
Takahashi et al., "Interframe CODEC for NTSC Color Television Signals", Fujitsu Scientific & Technical Journal, vol. 13, No. 4, 1977, pp. 21–52.

Primary Examiner—Thang V. Tran
Attorney, Agent, or Firm—Richard A. Weiss

[57] **ABSTRACT**

Methods and apparatus for encoding and decoding an audio and/or video signal, and a record carrier for use with such apparatus. One or more audio and/or full motion video signals, e.g., a video signal (and possibly computer data), are recorded on an interactive compact disc. The video signal prior to being recorded is encoded into code blocks of variable lengths, each corresponding to a picture or picture pair. A decoder delay time parameter associated with one or more of the code blocks, which parameter represents a length of time (i.e., a delay time) with which the corresponding picture of a code block is to be displayed after that code block has been received by a decoding apparatus is determined and included in the video signal prior to being recorded.

29 Claims, 4 Drawing Sheets



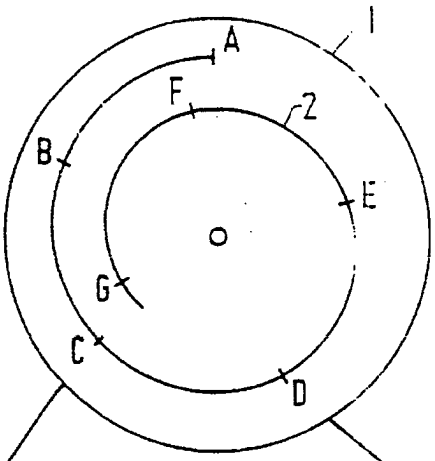


FIG.1A

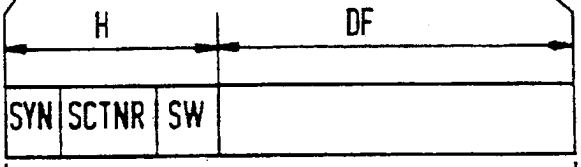


FIG.1B

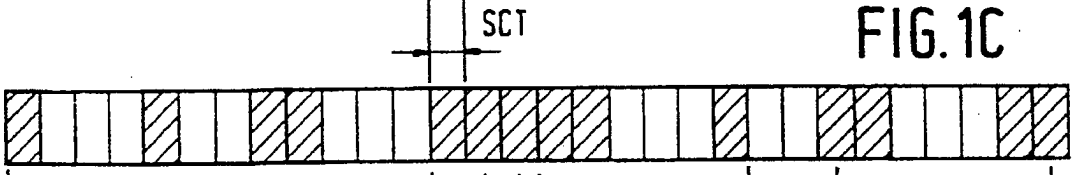


FIG.1C

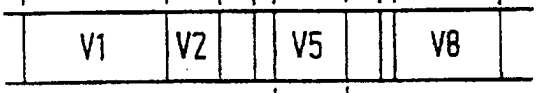


FIG.1D

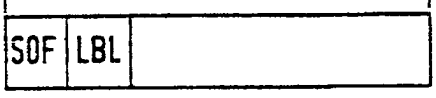
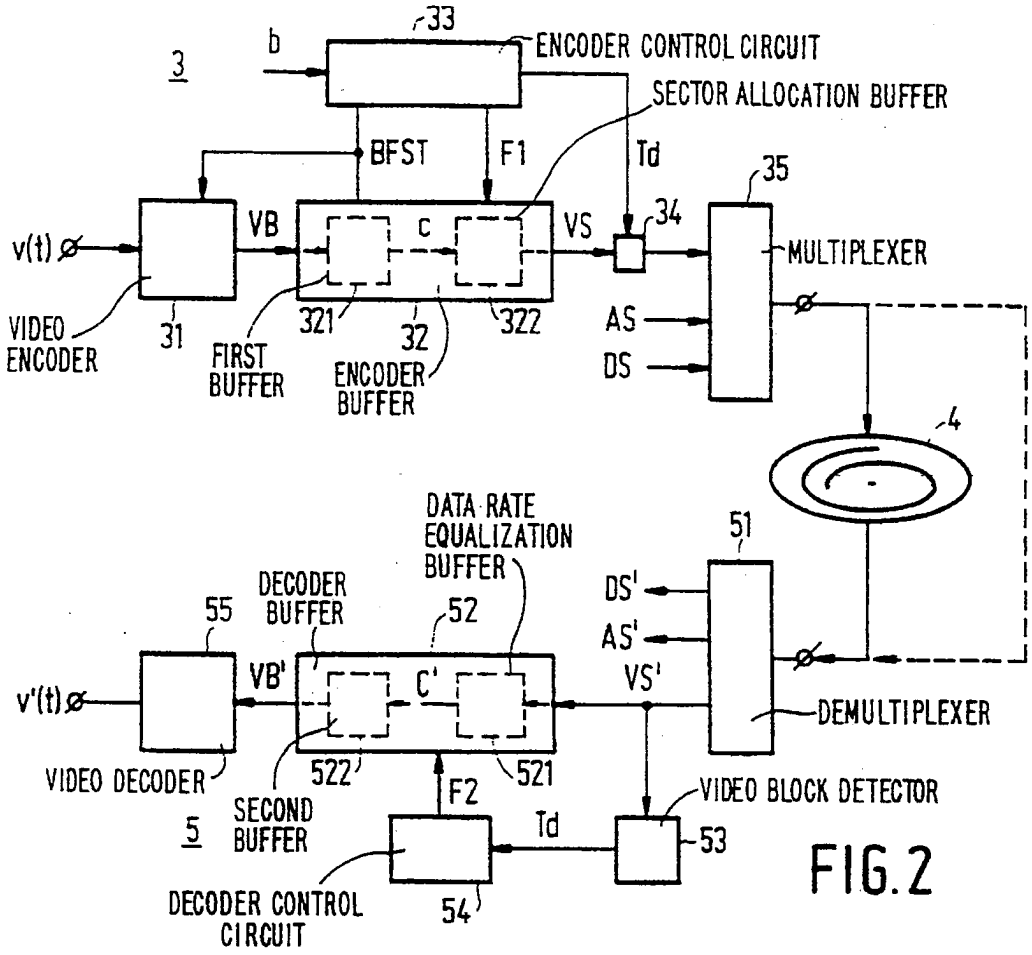


FIG.1E


3
b
33
ENCODER CONTROL CIRCUIT
SECTOR ALLOCATION BUFFER
BFST
F1
Td
35
v(t)
VB
c
VS
34
MULTIPLEXER
AS
DS
VIDEO ENCODER
31
FIRST BUFFER
321
32
ENCODER BUFFER
322
4
DATA RATE EQUALIZATION BUFFER
51
DS'
AS'
VS'
55
DECODER BUFFER
52
v'(t)
VB'
C'
DEMULTIPLEXER
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F2
VIDEO BLOCK DETECTOR
5
SECOND BUFFER
Td
53
DECODER CONTROL CIRCUIT
54

FIG.2

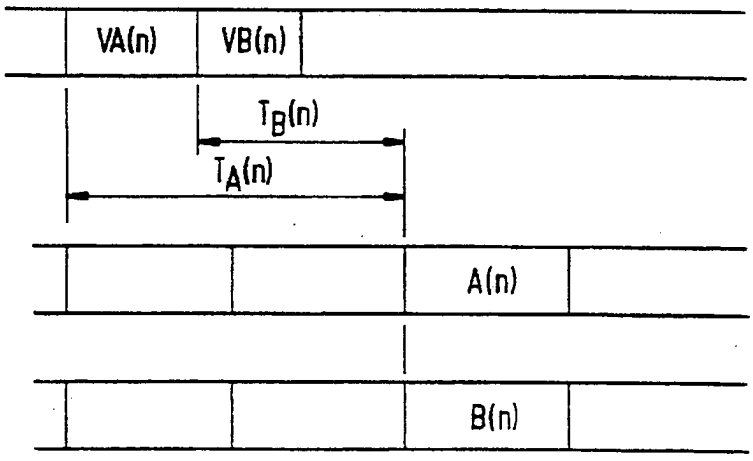
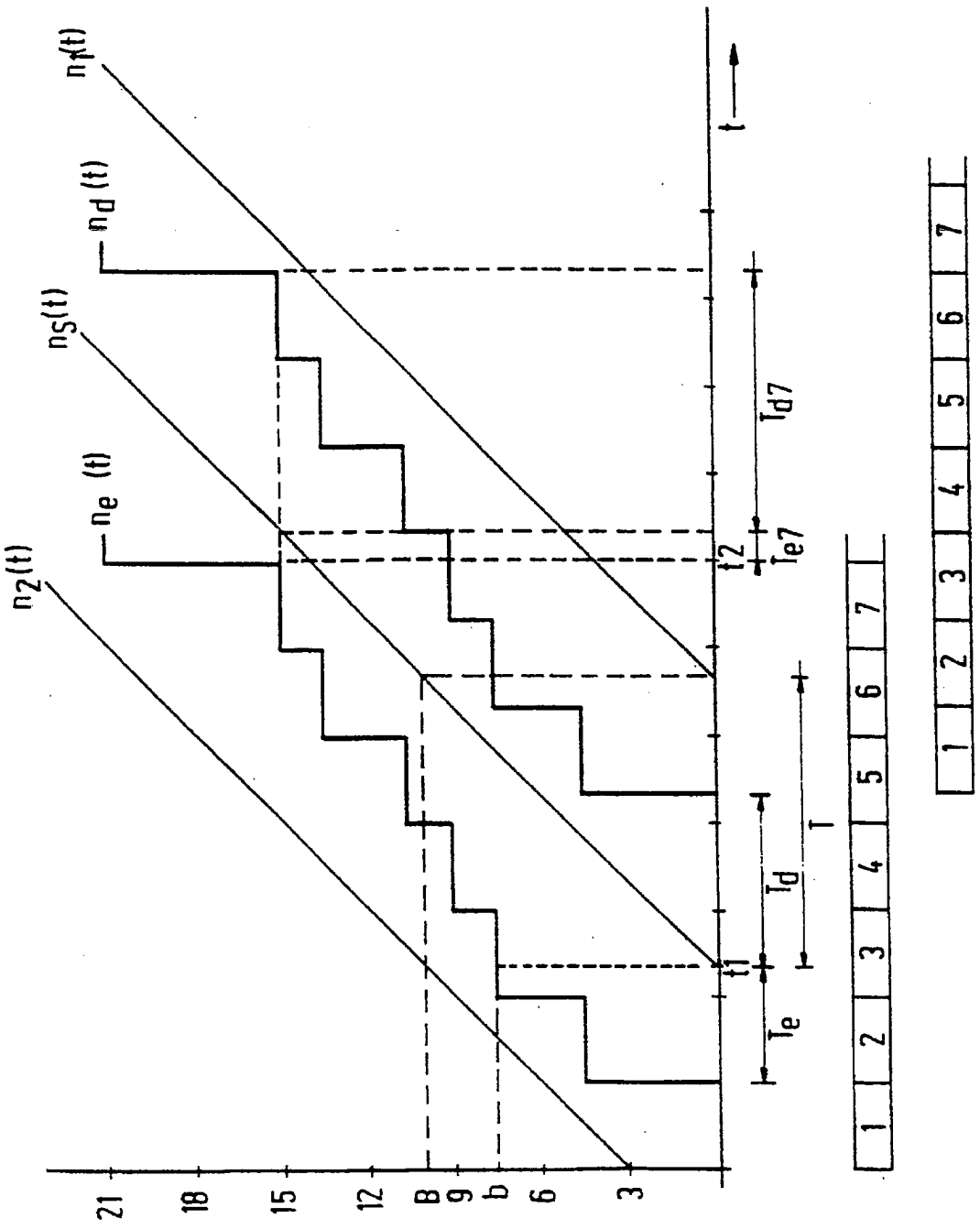

VA(n)
VB(n)
$T_B(n)$
$T_A(n)$
A(n)
B(n)

FIG.5

FIG. 3A

FIG. 3B

FIG. 3C



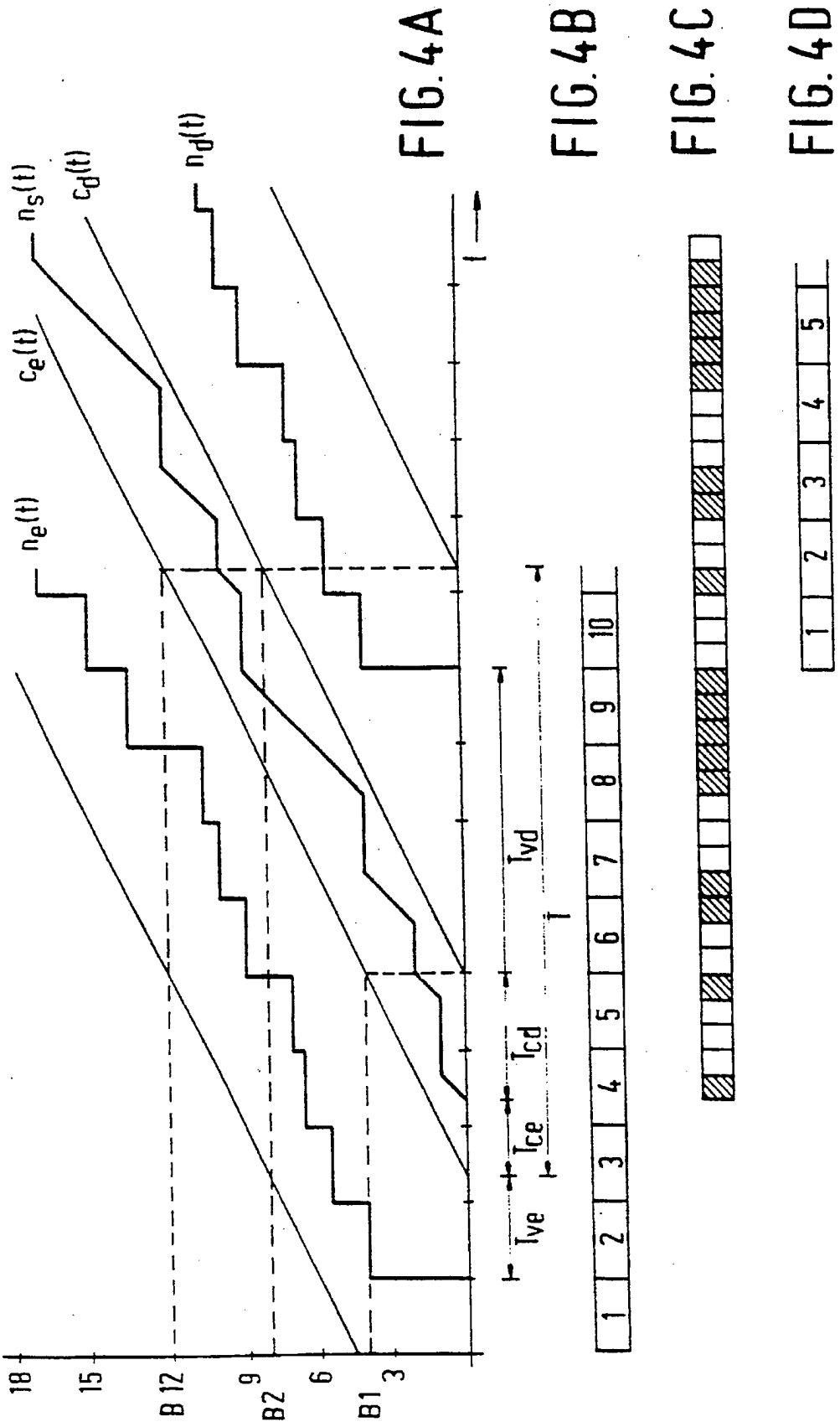


FIG.4A
FIG.4B
FIG.4C
FIG.4D
$n_s(t)$
$c_d(t)$
$n_d(t)$
$c_e(t)$
$n_e(t)$
t
T_{vd}
T_{ve}
T_{ce}
T_{cd}
T
18
15
B 12
9
B2
6
B1
3
1 2 3 4 5 6 7 8 9 10
1 2 3 4 5

METHOD AND APPARATUS FOR ENCODING AND DECODING AN AUDIO AND/OR VIDEO SIGNAL, AND A RECORD CARRIER FOR USE WITH SUCH APPARATUS

CROSS REFERENCE TO RELATED APPLICATIONS

This is a continuation of Application Ser. No. 08/086,402, filed Jun. 30, 1993 and now abandoned, which was a continuation of Application Ser. No. 07/711,186, filed Jun. 5, 1991 and now abandoned.

BACKGROUND OF THE INVENTION

The invention relates to a method of encoding audio and/or video signals for transmissions via a transmission medium More particularly, the transmission medium is preferably an optically readable disc. Nevertheless, the transmission medium may also be a magnetic tape or disc, or a direct connection between a transmitter and a receiver. The invention also relates to a transmission medium on which audio and/or video signals are recorded, to an encoding apparatus for encoding and transmitting the audio and/or video signals, and to a decoding apparatus for receiving those signals after unloading and transmission.

The interactive compact disc (CDI) on which data for text and graphic images and digital audio is stored has been developed in the last few years. The presentation possibilities of CDI are considerably enhanced if full motion video pictures are also recorded on it. The known analog recording of a video signal on compact disc video (CDV) is not suitable for this purpose. For this reason, a video signal on CDI is digitized.

A full-motion video scene is considered as a sequence of pictures (of that video scene) of which there are, for example, 25 or 30 per second. Each picture comprises, for example, 256 picture lines and 352 pixels per picture line. The sequence of pictures is converted by means of a suitably chosen encoding method into a series of video blocks, each comprising so much digital information that each picture can be reconstructed without any noticeable loss of quality. Together with the audio signal and further data, the encoded video signal is recorded optically. A CDI may comprise various video scenes.

The most efficient encoding methods convert successive signal portions into successive code blocks of variable lengths. In the case of a video signal, these signal portions are formed, for example, by the pictures or picture pairs of which the signal is composed. Some pictures may be subjected to intraframe coding and are then converted into code blocks from which the picture can be reconstructed completely. Other pictures may be subjected to interframe coding, which means that the pictures can only be reconstructed with the aid of previous pictures. The code blocks of a video signal will hereinafter be referred to as video blocks. Due to their variable length, the successive video blocks are read at irregular instants when a disc in which they are stored is being played. Moreover, the video blocks on the disc may alternate with (or may even by interrupted by) other data signals, for example, a lip-synchronous digital audio signal corresponding to the video scene.

The pictures corresponding to the video blocks should be displayed at a constant frequency of, for example, 25 frames per second. However, the instant when a video block of the disc is being read hardly ever corresponds exactly to the instant when the corresponding picture from the video scene is to be displayed. In a player, the video blocks are, therefore, applied to a memory buffer at a frequency which is entirely determined by the way in which they are "packed" on the disc. Subsequently, the video block are read from the buffer at the picture frequency required for display. On an average, the number of video blocks applied per second from the disc to the buffer equals the number of pictures displayed per second. The video block corresponding to the next picture to be displayed will always have to be stored completely in the buffer. Moreover, the buffer will already comprise a subsequent video block, a portion thereof or even a number of subsequent video blocks. As soon as a picture has been decoded, the corresponding video block may be removed from the buffer. The buffer space then released is written by one or more subsequent video blocks or a portion thereof. The number of video blocks stored in the buffer for later display is thus variable, and is greatly dependent on the encoding efficiency and the presence of signals other than the relevant video signal on the disc.

It would seem that the display of a video scene can start as soon as the first video block has been received completely and is stored in the buffer. However, this is not the case. It is possible that a subsequent video block is too large to be scanned (and stored in the buffer) within the required time (1/25 sec) to (decode and) display the picture corresponding to the first video blank. As a result, the corresponding picture of the subsequent video block cannot be displayed in time. The absence of a complete video block in the buffer at the instant when the corresponding picture has to be decoded and displayed is sometimes referred to as underflow of the buffer.

Underflow of the buffer also occurs if a large quantity of other (non-video) data has been packed together with the video blocks of a scene causing the buffer to be temporarily not filled with video blocks. Because of that other data the buffer empties, and at a given instant the video block for the corresponding next picture to be displayed is not yet present. The display of the video scene then stalls, and the pictures are not smooth moving.

If the display of a picture of a video scene starts too late after the corresponding video block has been received, it is probable that the buffer will fill so that the display of the video scene also stalls. This is referred to as overflow of the buffer.

The same problems occur with audio signals which may also be recorded on the disc in a non-contiguous manner,

SUMMARY OF THE INVENTION

It is an object of the invention to provide a method of encoding audio and/or video signals (for transmission) in which the occurrence of overflow and underflow of a decoder buffer is prevented so that the display of pictures can proceed in an undisturbed manner.

According to the invention, a parameter is associated with at least one selected code block, which parameter indicates the quantity of delay with which that code block must be decoded after it has been received. If the corresponding picture is decoded with this delay, it can be displayed without the risk of overflow or underflow of the buffer. This ensures an undisturbed display. The transmission of the parameter, sometimes referred to as a decoder delay parameter (or decoder delay for short), also enables synchronous display of two signals, for example, a video signal with a time-division multiplexed associated audio signal, or two

video signals jointly representing a three-dimensional video scene.

In principle, it is sufficient to associate the parameter with one video block. This will preferably be the first block of the video scene. All further pictures can then be read at a constant picture frequency without a further risk of overflow or underflow of the buffer.

In a further embodiment of the method, the decoder delay parameter is regularly associated with video blocks. The constant picture frequency can then be obtained in a favorable manner. Moreover, this provides the possibility of a so-called "random-access" display. This means the display of a fragment of a video scene from the video block with which the decoder delay is associated.

The decoder delay parameter may assume various formats, but it preferably indicates the state of a counter which is regularly loaded with a reference value which is also transmitted and which counter further receives a predetermined clock signal.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1**A–E show diagrammatically an optically readable disc with an audio and/or video signal recorded thereon and the format of that disc.

FIG. **2** shows the general structure of a transmission circuit suitable for performing the method according to the invention.

FIGS. **3**A–C show some time diagrams which help explain the circuit of FIG. **2**.

FIG. **4** shows some further time diagrams to explain the circuit of FIG. **2**.

FIG. **5** shows some time diagrams to explain the transmission of two simultaneously transmitted signals.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

FIG. **1**A shows diagrammatically an optically readable disc **1** with an information track **2** recorded thereon. A so-called sector, of which there may be about 300,000, is present between every two successive points A, B, C, D, etc. The structure of such a sector is shown diagrammatically in FIG. **1**B. It is divided into a sector header H or 24 bytes and a data field DF of 2324 bytes. The sector head H comprises a synchronization word SYN of 12 bytes, a sector number SCTNR of 4 bytes and a service word SW of 8 bytes. The synchronization word SYN marks the start of a sector. The sector number SCTNR indicates the ordinal number of the sector on the disc **1**. The service word SW indicates whether the data field DF of the sector comprises video data, audio data or computer data. In conformity with that data, a sector is sometimes referred to as a video sector, an audio sector or a data sector.

The conventional rate of revolution of the disc **1** is such that 75 sectors per second are scanned. This corresponds to a bit rate, hereinafter referred to as channel bit rate, of approximately 1.4 Mbit/sec. If a disc comprises video sectors only, the video bit rate is equal to the channel bit rate. If a disc also comprises audio and data sectors, the video bit rate decreases accordingly.

FIG. **1**C shows a part of the track **2** in which the sectors are denoted by SCT. More particularly the video sectors therein are shaded. The video sectors alternate with other sectors.

There are many encoding methods for reducing the number of bits per picture without deteriorating picture quality. The most efficient encoding methods convert successive pictures of a video scene into video blocks of distinct number of bits. In FIG. **1**D, this is shown in the form of video blocks **V1**, **V2**, etc., each having a distinct length. For example, video block **V1** has a length of 4 sectors on the disc **1**, video block **V2** has a length of 1¼ sector, etc.

FIG. **1**E shows the data format of a video block. The start of a video block is marked by the presence of a unique start-of-frame word SOF. The video block also comprises a label LBL in which specific control information is stored for the corresponding video block.

FIG. **2** shows the general structure of a circuit for transmitting audio and video signals. The circuit comprises an encoding apparatus **3**, a compact disc **4** and a decoding apparatus **5**.

The encoding apparatus **3** of FIG. **2** comprises a video encoder **31** to which a video signal v(t) is applied. The video encoder **31** encodes successive pictures of the video signal, of which there are 25 per second, into video blocks VB of variable lengths. These pictures are applied video block by video block to an encoder buffer **32**. To prevent overflow and underflow of the encoder buffer **32**, a buffer status signal BFST is fed back to the video encoder **31** so that the video encoder **31** can adapt the encoding efficiency to the contents of the encoder buffer **32**. If the encoder buffer **32** tends to get filled and there is a risk of overflow, the video signal is temporarily quantized in a coarser manner. If the encoder buffer **32** tends to get empty, the video signal is quantized more accurately, or pseudo-video data is possibly temporarily applied to the encoder buffer **32**. The buffer status signal BFST is also applied to an encoder control circuit **33**. The encoder control circuit **33** of FIG. **2** is adapted to generate, at a predetermined degree of occupation of the encoder buffer **32**, a clock signal F1 with which the encoder buffer **32** is read. The encoder control circuit **33** also determines the value of a parameter T_d for each video block in a manner to be described hereinafter. This parameter (T_d) is associated with a video block by means of an inserter **34** and transmitted in the label LBL of that block (see FIG. **1**E).

As is shown in FIG. **2**, the encoder buffer **32** may be considered to be divided into a first buffer **321** to which the video blocks VB are applied and which is read at a constant video bit rate C, and a sector allocation buffer **322** which converts this constant bit stream into video sectors VS. The video sectors VS are applied from the encoder buffer **32** to a first input of a multiplexer **35** which receives audio sectors AS at a second input and data sectors DS at a third input. The resultant bit stream is recorded on the compact disc **4**.

When the compact disc **4** is played at a later stage, the sectors are scanned and applied to a demultiplexer **51** in which the video sectors VS' are separated from audio sectors AS' and data sectors DS' by reference to each sectors service word SW (see FIG. **1**B). The video sectors VS' are applied to a decoder buffer **52** and a video block detector **53**. The video block detector **53** detects the occurrence of a start-of-frame code SOF (see FIG. **1**E) and reads from the subsequent label LBL the parameter T_d transmitted therein. The parameter T_d is applied to a decoder control circuit **54** which is adapted to read the decoder buffer **52** with a clock signal F2. In a manner to be described hereinafter, the parameter T_d determines the instant when each video block is read from the decoder buffer **52**.

As is shown in the FIG. **2**, the decoder buffer **52** may be considered to be divided into a data rate equalization buffer

521 to which the video sectors VS' are applied and which is read at a constant video bit rate C', and a second buffer 522 which converts this constant bit stream into successive video blocks VB' Finally, each video block is applied to a video decoder 55 for conversion into a picture. The successive pictures which are obtained are applied as a video signal v' (t) to a display device (now shown).

In practice the actual instant when a disc is being played does not play any role at all. Therefore, it will be assumed hereinafter that the output of the encoding apparatus 3 is directly connected to the input of the decoding apparatus 5. This is indicated by means of a broken line in FIG. 2.

It will be assumed for the time being that only video signals are transmitted. This means that the encoder buffer 32 can apply an uninterrupted bit stream to the disc 4 at the full channel bit rate of 1.4 Mbit/sec (75 sectors per second). This means that the sector allocation buffer 322 and the multiplexer 35, on the one hand, and the demultiplexer 51 and the data rate equalization buffer 521, on the other hand, of FIG. 2 do not play a role in the following discussion.

The operation of the circuit shown in FIG. 2 will be explained with reference to some time diagrams which are shown in FIGS. 3A–C. More particularly, FIG. 3B shows a number of successive pictures enumerated 1, 2, 3, etc. These pictures occur at a picture frequency of 25 frames per second and are applied to the video encoder 31 of FIG. 2. As soon as each picture has been encoded, the corresponding video block is written into the encoder buffer 32 of FIG. 2. For the sake of simplicity, it is assumed that this is effected timelessly. The quantity of video data cumulatively applied to the encoder buffer 32 and expressed in disc sectors increases step-wise for each video block. This is denoted by means of the curve $n_e(t)$ in FIG. 3A.

Reading of the encoder buffer 32 of FIG. 2 and applying data to the output of the encoding apparatus 3 of FIG. 2 starts from instant t1. This instant t1 is determined, for example, by reaching a predetermined degree b of occupation of the encoder buffer 32 and may be different for each video scene. Reading is effected at a constant rate of 75 sectors per second, i.e., 1.4 Mbit/sec. The quantity of video data cumulatively withdrawn from the encoder buffer 32 increases linearly. This is denoted by means of the curve $n_s(t)$ in FIG. 3A. The curves $n_e(t)$ and $n_s(t)$ must not intersect each other because this would mean that a video block is read from the encoder buffer 32 before it is written into it (underflow of the encoder buffer 32). As already previously stated, underflow of the encoder buffer 32 is prevented by adapting the quantization of the video scene to the contents of the encoder buffer 32.

Based on the assumption that the output of the encoding apparatus 3 of FIG. 2 is directly connected to the input of the decoding apparatus 5 of FIG. 2, the curve $n_s(t)$ shown in FIG. 3A also indicates the cumulative quantity of video data applied to the decoder buffer 52 of FIG. 2. The decoder buffer 52 must be read in such a manner that the curve $n_s(t)$ is not exceeded, because underflow of the decoder buffer 52 could then occur. Overflow of the decoder buffer 52 should not occur either. In FIG. 3A line $n_1(t)$ at a distance B (the buffer size) from the line $n_s(t)$ indicates the threshold of overflow of the encoder buffer 52. The 52 line $n_1(t)$ should not be exceeded by the curve $n_s(t)$.

The decoder buffer 52 of FIG. 2 is read video block by video block. For the sake of simplicity, it is assumed that a video block is read timelessly. The quantity of video data cumulatively withdrawn from the decoder buffer 52 and expressed in disc sectors increases step-wise for each video block. This is denoted by means of the curve $n_d(t)$ in FIG. 3A. As soon as a video block has been read and decoded, the corresponding picture is displayed in 1/25 sec. FIG. 3C shows the display of the decoded pictures 1, 2, 3, etc.

The curve $n_d(t)$ is a replica of the curve $n_e(t)$ shifted over a time interval T_e+T_d. Here T_e, also referred to as an encoder delay, is the delay time between the instant when the first video block of the video scene is written into the encoder buffer 32 of FIG. 2 and the instant t1 when the transmission of this video block begins. In a corresponding manner T_d, also referred to as a decoder delay, is the delay time between the instant when the reception of the first video block in the decoder buffer 52 of FIG. 2 begins and the instant when this video block is read from the decoder buffer 52. The time interval T_e+T_d represents the delay time occurring between writing a video block into the encoder buffer 32 and reading the same video block from the decoder buffer 52. This delay time is constant. As previously noted, t1, and consequently T_e, may be different for each video scene. In addition (and in conformity therewith), the decoder delay T_d may be different for each video scene as well.

The instant when the decoding apparatus of FIG. 2 starts reading the decoder buffer 52 of FIG. 2 is of great importance. In fact, if the decoder 5 should start reading too early, there may be underflow of the decoder buffer 52 because the curve rid $n_d(t)$ will intersect the boundary line $n_s(t)$. If the decoder 5 starts reading too late, there may be overflow of the decoder buffer 52 because the curve rid n_d (t) will intersect the boundary line $n_1(t)$. Both underflow and overflow may become manifest in the video scene at a possibly later stage.

Overflow and underflow of the decoder buffer 52 of FIG. 2 do not occur if the curve rid $n_d(t)$ iS always as far remote from the boundaries lines $n_s(t)$ and $n_1(t)$ as the curve $n_e(t)$ is from boundaries lines $n_2(t)$ and $n_s(t)$. Line $n_2(t)$ is a line at a distance B (the decoder buffer size) from the line $n_e(t)$. This is realized by choosing a suitable value for the decoder delay T_d, as well as by the previously mentioned mechanism of adaptive quantization in the encoding apparatus 3 of FIG. 2, which ensures that the curve $n_e(t)$ remains completely between the two boundaries lines $n_2(t)$ and $n_s(t)$.

A suitable value for decoder delay T_d can be obtained by considering the fact that the previously mentioned delay time T_e+T_d iS equal to a time interval T shown in FIG. 3A. The time interval T corresponds to the time required to fully read a completely filled encoder buffer or to completely fill a still empty decoder buffer, and is entirely determined by the buffer size B and the video bit rate at which that buffer is read or written. Accordingly, the value of T_d can be derived from the computation of the different $T-T_e$. Here both T_e and T are known to the encoding apparatus.

The encoding apparatus 3 of FIG. 2 associates the decoder delay T_d as a parameter with the first video block of the scene so as to enable the decoding apparatus 5 of FIG. 2 to determine the instant when reading of the decoder buffer 52 of FIG. 2 should start. After the decoding apparatus 5 has read the video block with the delay T_d from the encoder buffer 52, the reading process can be continued at the picture frequency in an autonomic manner without the risk of underflow or overflow of the decoder buffer 52. The picture frequency of 25 Hz can be obtained by dividing the channel bit rate (75 sectors/sec*2324 bytes/sector*8 bits/byte) by 55776. The coupling of the picture frequency to the channel bit rate which is necessary for this purpose is, however, superfluous if the decoder delay parameter has regularly been associated with video blocks. In such a case, the

decoder delay will generally be different for each video block.

If the difference between the actual instant when a video block is read and the instant determined by the corresponding decoder delay parameter occurs at a given picture frequency, the picture frequency or the rate of revolution of the disc can be corrected in response to this difference. FIG. 3A shows by way of example a decoder delay T_{d7} for picture 7. At the instant denoted by t2 the video block corresponding to picture 7 is written into the encoder buffer 32 of FIG. 2. After encoder delay T_{e7}, transmission of the video block corresponding to picture 7 from the encoder buffer 32 to the encoder buffer 52 of FIG. 2 starts, and after a subsequent decoder delay T_{d7}, that video block must be decoded. The encoding apparatus 3 of FIG. 2 associates the decoder delay $T_{d7}=T-T_{e7}$ for picture 7 with video block 7 and transmits it in the label LBL of this block (see FIG. 1E).

The regular transmission of the decoder delay also provides the possibility of a so-called "random-access" playback mode. This means playing a fragment of the video scene from a picture other than the first picture. For example, the decoder delay T_{d7} shown in FIG. 3A can be used to play the fragment of the video scene from picture 7. Picture 7 is preferably an intraframe-encoded picture and can therefore be reconstructed without the aid of previous pictures. In principle, it is possible to compute the decoder delay T_{d7} for picture 7 from the previous signal. However, such computations are complicated and also require the availability of previous information. In the case of random-access display, the previous signal is, however, not available.

The situation described above will be more complicated if not all disc sectors are allocated to video data. If the disc also comprises sectors with audio and computer data, they will alternate with video sectors on the disc. The average video bit rate for a video scene will now be lower than 75 sectors per second. The average video bit rate will hereinafter be expressed in a number S indicating which part of the channel bit rate is suitable for video transmission. For example, S=½ means that on an average 1 out of 2 sectors is a video sector. This corresponds to a video bit rate of ½*75=37.5 sectors per second, i.e., 0.7 Mbit/sec.

For the purpose of illustration, FIG. 4 shows some time diagrams of the encoding and decoding process if S=½. FIG. 4B shows diagrammatically the successive pictures 1, 2, etc. of a video scene applied to the encoding apparatus 3 of FIG. 2. The curve $n_3(t)$ in FIG. 4A indicates the quantity of video data applied for each picture to the encoder buffer 32 of FIG. 2 and expressed in the number of disc sectors. In comparison with the curve $n_e(t)$ in FIG. 3A, the encoding is now such that on average each picture is encoded in 1.5 sectors instead of in 3 sectors. The contents of the encoder buffer 32 are applied to selected sectors of the disc. This is effected in accordance with a given pattern, an example of which is shown in FIG. 4C. In the pattern shown in FIG. 4C, the shaded sectors represent video sectors and the other sectors are audio sectors or data sectors. FIG. 4C also shows the signal controlling the multiplexer 35 of FIG. 2. The average bit rate is reached in this example by writing video information on 8 out of each 16 sectors on the disc. The quantity of video data cumulatively applied to the disc is indicated in FIG. 4A by means of the curve $n_s(t)$.

When the disc is being played, the reverse operations take place. The curve $n_s(t)$ now represents the number of video sectors cumulatively read from the disc. These sectors are applied to the decoder buffer 52 of FIG. 2, from which they are subsequently read video block by video block in accordance with the curve rid $n_d(t)$.

In FIG. 4A, $n_e(t)-n_s(t)$ indicates the actual contents of the encoder buffer 32 of FIG. 2. To prevent underflow of the encoder buffer 32, the curves $n_e(t)$ and $n_s(t)$ should not intersect each other. This condition is certainly met if, as already shown in FIG. 2, the encoder buffer 32 is considered to be divided into a first buffer 321 to which the video blocks are applied and which is read at a constant video bit rate, and a sector allocation buffer 322 which converts this constant bit stream into the sector-sequential supply of sectors to the disc. That constant bit stream is denoted by the straight line $c_e(t)$ in FIG. 4A. The slope of the line $C_e(t)$ iS the average bit rate, 0.7 Mbit/sec in this example. As long as the two curves $n_e(t)$ and $n_s(t)$ do not intersect the line $c_e(t)$, there is no encoder buffer underflow.

In a corresponding manner, $n_s(t)-n_d(t)$ represents the actual contents of the decoder buffer 52 of FIG. 2. To prevent underflow of the decoder buffer 52, the curve $n_e(t)$ should not intersect the curve $n_s(t)$. This condition is certainly met if, as already shown in FIG. 2, the decoder buffer 52 is considered to be divided into a data rate equalization buffer 521 having a size of B1 to which the video sectors of the disc are applied and which is read at the constant bit rate, and a second buffer 522 of the size B2 which converts this constant bit stream into video blocks. That constant bit stream is denoted by the straight line $C_d(t)$ in FIG. 4A. The slope of the line $C_d(t)$ corresponds to the average video bit rate of 0.7 Mbit/sec. As long as the two curves $n_s(t)$ and $n_d(t)$ do not intersect the line $C_d(t)$,there is no decoder buffer underflow.

The previously mentioned decoder delay parameter (T_d) which indicates when the decoding apparatus 5 of FIG. 2 can read a video block from the decoder buffer 52 of FIG. 2 after the first bit of the video scene has been scanned (i.e. read from the disc), is now equal to $T_{cd}+T_{vd}$ shown in FIG. 4A. Its value is completely determined by the encoding apparatus 3 of FIG. 2 and transmitted in the label LBL (see FIG. 1E) of a corresponding video block.

The decoder delay parameter is determined as follows. The value of $T_{cd}+T_{vd}$ follows from the consideration that $T_{ve}+T_{ce}+T_{cd}+T_{vd}$ corresponds to the delay of the video signal (from being read into the encoder buffer 32 of FIG. 2 to being read out of decoder buffer 52 of FIG. 2) if the output of the encoding apparatus 3 of FIG. 2 is directly coupled to the input of the decoding apparatus 5 of FIG. 2. This delay is equal to the interval T shown in FIG. 4A and is dependent on the average video bit rate which is S*75 sectors per second and the size B (=B1 +B2) of the decoder buffer 52 of FIG. 2. More particularly, it can be derived from FIG. 4A that

$$T=B/S*75$$

and

$$T_{cd}+T_{vd}=T-(T_{ve}+T_{ce}).$$

Here. S is fixed when writing the disc. As for the decoder buffer size B, it holds that it may be a predetermined fixed value which is fixed in the encoding apparatus 3 of FIG. 2 as well as in the decoding apparatus 5 of FIG. 2. The encoding apparatus 3 may also be adapted to transmit the buffer size B to be reserved in the decoding apparatus 5 as a further parameter. It is notably sensible to render the decoder buffer size B dependent on S. The (encoder) delay ($T_{ve}+T_{ce}$), being the time between the encoding of a video picture and its transmission, is determined by the encoding apparatus 3 itself. As already previously stated, the instant when the first video block is transmitted may be determined

by reaching a predetermined degree of occupation of the encoder buffer 32.

The form of the transmitted decoder delay parameter may assume several formats. For example, it is possible to transmit a value indicating at which degree of occupation of the decoder buffer 52 of FIG. 2 the decoder 5 of FIG. 2 should start reading. This degree of occupation may be expressed in an absolute value (number of bits) or in a relative value (fraction of the buffer size B). The decoder delay parameter may also indicate the time delay in suitably chosen units with respect to the instant when a video block is written into the decoder buffer 52. Suitable units are, for example, (m) sec or the number of clock periods of a predetermined clock signal. It has been found useful to have the decoder delay parameter indicate the state of a counter at which the decoding of a video block should start The counter is then regularly loaded with a reference value which is also transmitted. The counter is further clocked by a predetermined clock signal. The transmitted reference value may form part of the service word SW (see FIG. 1B). A suitable frequency of the clock signal is 90 kHz. This value is an integral multiple of the picture frequencies 24 Hz, 25 Hz, 30 Hz and 29.97 Hz which are suitable for display.

Finally, it is to be noted that in the foregoing the decoder delay parameter is only described for one signal, in this case a video signal. However, the decoder delay parameter also enables the synchronous display of a plurality of signals. These may be, for example, a video signal and an associated lipsynchronous audio signal. However, they may also be two vide signals multiplexed on the compact disc, which signals may not only be displayed separately but, also if desired, simultaneously. This is shown diagrammatically in FIG. 5 for two video signals A and B.

FIG. 5 shows a video block VA(n) and VB(n) of the two signals, in which n is the ordinal number of the corresponding picture to be displayed. As is apparent from FIG. 5, the decoder delay parameters $T_A(n)$ and $T_B(n)$ transmitted in the video block have such a value that the corresponding pictures A(n) and B(n) are displayed simultaneously.

We claim:

1. A method for encoding an audio and/or video signal into an encoded signal which can be decoded by a decoding device including a decoder buffer for receiving the encoded signal and a decoder for decoding the encoded signal, the method comprising:

encoding successive portions of the audio and/or video signal into corresponding successive code blocks making up the encoded signal;

determining a delay time parameter for a code block of the code blocks, which delay time parameter represents a length of time during which the code block is to be stored within the decoder buffer before decoding by the decoder in order to ensure that the decoder buffer will not experience overflow or underflow of the code blocks; and

inserting the delay time parameter into the encoded signal.

2. The method as claimed in claim 1, wherein the method is used to encode at least two audio and/or video signals into at least two respective encoded signals which each includes a respective delay time parameter therein, and further comprises combining the at least two respective encoded signals.

3. The method as claimed in claim 1, wherein the audio and/or video signal is a video signal, and the method further comprises combining an encoded audio and/or data signal with the encoded signal after insertion of the delay time parameter to obtain in a combination signal.

4. The method as claimed in claim 3, further comprising recording the combination signal on an optically readable or magnetic record carrier.

5. The method as claimed in claim 3, further comprising recording the combination signal produced on a record carrier.

6. A recorded record carrier having the combination signal produced by the method claimed in claim 5.

7. The method as claimed in claim 1, further comprising recording the encoded signal after insertion of the delay time parameter on an optically readable or magnetic record carrier.

8. The method as claimed in claim 1, further comprising recording the encoded signal on a record after insertion of the delay time parameter carrier.

9. A recorded record carrier having the encoded signal produced by the method claimed in claim 8.

10. The method as claimed in claim 1, wherein the delay time parameter is included in the code block.

11. The method as claimed in claim 1, wherein the code block is a first code block of the code blocks.

12. The method as claimed in claim 1, wherein the delay time parameter represents the length of time during which each of the code blocks is to be stored within the decoder buffer before decoding by the decoder in order to ensure that the decoder buffer will not experience overflow or underflow of the code blocks.

13. The method as claimed in claim 1, wherein a respective delay time parameter is determined for a plurality of the code blocks, and each respective delay time parameter is inserted into the code block for which that respective delay time parameter is determined.

14. The method as claimed in claim 1, wherein the delay time parameter is a time indication.

15. The method as claimed in claim 1, wherein the delay time parameter is a number of clock period of a predetermined clock signal.

16. The method as claimed in claim 1, wherein the delay time parameter is the state of a counter.

17. The method as claimed in claim 1, wherein the delay time parameter is the degree of occupation the decoder buffer must be at before the code block, after being stored therein, is to be decoded.

18. An encoding apparatus for use with a system for encoding and decoding an audio and/or video for signal, which system includes the encoding apparatus for encoding the audio and/or video signal into an encoded signal, and a decoding apparatus having a decoder buffer for receiving the encoded signal and a decoder for decoding the encoded signal, the encoding apparatus comprising:

means for encoding successive portions of the audio and/or video signal into corresponding successive code blocks making up the encoded signal;

means for determining a delay time parameter for a code block of the code blocks, which delay time parameter represents a length of time during which the code block is to be stored within the decoder buffer before decoding by the decoder in order to ensure that the decoder buffer will not experience overflow or underflow of the code blocks; and

means for inserting the delay time parameter into the encoded signal.

19. The encoding apparatus as claimed in claim 18, wherein the means for inserting the delay time parameter into the encoded signal inserts the delay time parameter into the code block.

20. The encoding apparatus as claimed in claim 19, wherein the audio and/or video signal is a video signal, and

the encoding device further comprises means for combining an encoded audio and/or data signal with the encoded signal after insertion of the delay time parameter to obtain a combination signal.

21. The encoding apparatus as claimed in claim **20**, further comprising means for recording the combination signal on an optically readable or magnetic record carrier.

22. The encoding apparatus as claimed in claim **18**, further comprising means for recording the encoded signal after insertion of the delay time parameter on an optically readable or magnetic record carrier.

23. A decoding apparatus for use with a system for encoding and decoding an audio and/or video signal, which system includes an encoding apparatus for encoding the audio and/or video signal into code blocks making up an encoded signal, determining a delay time parameter for a code block of the code blocks and inserting the delay time parameter into the encoded signal, and the decoding device for decoding the encoded signal, the decoding device comprising:

a) means for obtaining the delay time parameter from the encoded signal;

b) a decoder buffer for receiving the code blocks from the encoded signal; and

c) a decoder for decoding the code blocks after receipt by the decoder buffer, which decoder decodes the code block when the code block has been stored in the decoder buffer for a length of time represented by the delay time parameter which ensures that the decoder buffer will not experience overflow or underflow of the code blocks.

24. The decoding apparatus as claimed in claim **23**, further comprising control means for controlling the decoder buffer and the decoder so that the code block is stored in the decoder buffer for the length of time represented by the delay time parameter before the decoder decodes that code block.

25. The decoding apparatus as claimed in claim **23**, wherein the audio and/or video signal is a video signal, and the encoded signal after insertion of the delay time parameter has been combined with an encoded audio and/or data signal in a combination signal; and said decoder apparatus further comprises means for separating the encoded signal from the encoded audio and/or data signal.

26. The decoding apparatus as claimed in claim **25**, further comprising means for receiving the combination signal from an optically readable or magnetic record carrier.

27. The decoding apparatus as claimed in claim **25**, further comprising means for receiving the encoded signal, including the delay time parameter, from an optically readable or magnetic record carrier.

28. The decoding apparatus as claimed in claim **23**, wherein the decoder decodes each of the code blocks when that code block has been stored in the decoder buffer for a length of time represented by the delay time parameter in order to ensure that the decoder buffer will not experience overflow or underflow of the code blocks.

29. A method for decoding an audio and/or video signal encoded in successive code blocks making up an encoded signal, which encoded signal further includes a delay,time parameter, the method comprising:

a) obtaining the delay time parameter from the encoded signal;

b) supplying the code blocks of the encoded signal to a decoder buffer; and

c) decoding the code blocks after receipt by the decoder buffer in a manner whereby at least one of the code blocks is decoded when that code block has been stored in the decoder buffer for a length of time represented by the delay time parameter which ensures that the decoder buffer will not experience overflow or underflow of the code blocks.

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